

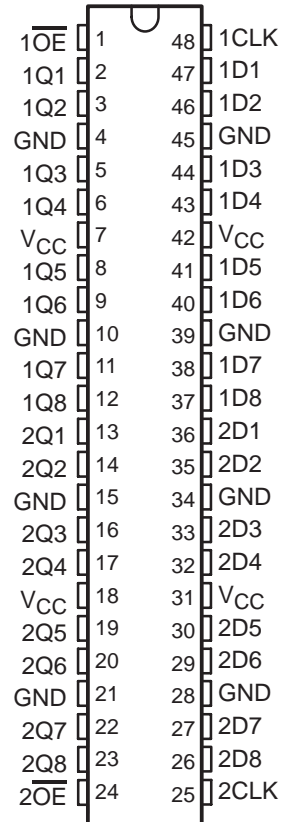
SN74LVTH16374-EP

3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

SCBS779A – NOVEMBER 2003 – OCTOBER 2004

- **Controlled Baseline**
 - One Assembly/Test Site, One Fabrication Site
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree†**
- **Member of the Texas Instruments Widebus™ Family**
- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static-Power Dissipation**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **I_{off} and Power-Up 3-State Support Hot Insertion**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Latch-Up Performance Exceeds 500 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

DGG OR DL PACKAGE
(TOP VIEW)



† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

description/ordering information

The SN74LVTH16374 is a 16-bit edge-triggered D-type flip-flop with 3-state outputs designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. This device is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

This device can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK), the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.



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description/ordering information (continued)

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

\overline{OE} does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

ORDERING INFORMATION

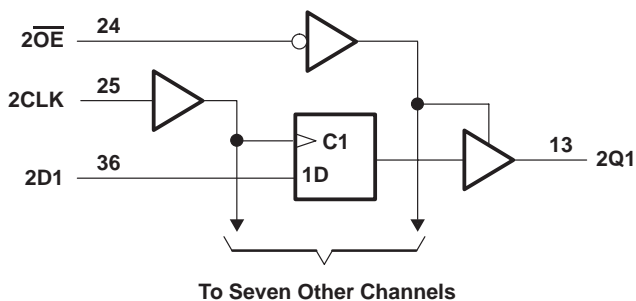
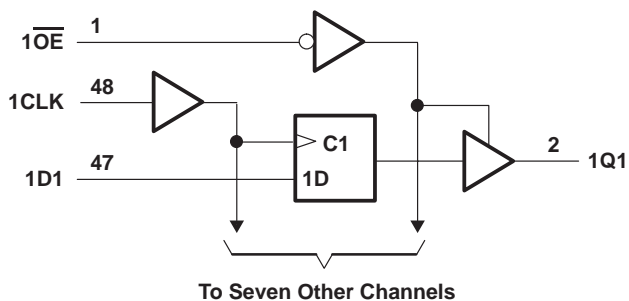
| T_A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|-------------|---------------|-----------------------|------------------|
| -40°C to 85°C | TSSOP – DGG | Tape and reel | CLVTH16374IDGGREP | LH16374EP |
| | SSOP – DL | Tape and reel | CLVTH16374IDLREP | LH16374EP |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each flip-flop)

| INPUTS | | | OUTPUT |
|-----------------|--------|---|--------|
| \overline{OE} | CLK | D | Q |
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | H or L | X | Q_0 |
| H | X | X | Z |

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|----------------------------|
| Supply voltage range, V_{CC} | –0.5 V to 4.6 V |
| Input voltage range, V_I (see Note 1) | –0.5 V to 7 V |
| Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1) | –0.5 V to 7 V |
| Voltage range applied to any output in the high state, V_O (see Note 1) | –0.5 V to $V_{CC} + 0.5$ V |
| Current into any output in the low state, I_O | 128 mA |
| Current into any output in the high state, I_O (see Note 2) | 64 mA |
| Input clamp current, I_{IK} ($V_I < 0$) | –50 mA |
| Output clamp current, I_{OK} ($V_O < 0$) | –50 mA |
| Package thermal impedance, θ_{JA} (see Note 3): DGG package | 70°C/W |
| DL package | 63°C/W |
| Storage temperature range, T_{stg} | –65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

| | | MIN | MAX | UNIT |
|--------------------------|------------------------------------|-----|-----|-----------------|
| V_{CC} | Supply voltage | 2.7 | 3.6 | V |
| V_{IH} | High-level input voltage | 2 | | V |
| V_{IL} | Low-level input voltage | | 0.8 | V |
| V_I | Input voltage | | 5.5 | V |
| I_{OH} | High-level output current | | –32 | mA |
| I_{OL} | Low-level output current | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 10 | ns/V |
| | | | | Outputs enabled |
| $\Delta t/\Delta V_{CC}$ | Power-up ramp rate | 200 | | μ s/V |
| T_A | Operating free-air temperature | –40 | 85 | °C |

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|----------------------|--|---|--|-----------------------------------|------|-----------|---------------|
| V_{IK} | | $V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$ | | | | -1.2 | V |
| V_{OH} | | $V_{CC} = 2.7\text{ V to }3.6\text{ V}$, $I_{OH} = -100\text{ }\mu\text{A}$ | | $V_{CC} - 0.2$ | | | V |
| | | $V_{CC} = 2.7\text{ V}$, $I_{OH} = -8\text{ mA}$ | | 2.4 | | | |
| | | $V_{CC} = 3\text{ V}$, $I_{OH} = -32\text{ mA}$ | | 2 | | | |
| V_{OL} | | $V_{CC} = 2.7\text{ V}$ | | $I_{OL} = 100\text{ }\mu\text{A}$ | | 0.2 | V |
| | | | | $I_{OL} = 24\text{ mA}$ | | 0.5 | |
| | | $V_{CC} = 3\text{ V}$ | | $I_{OL} = 16\text{ mA}$ | | 0.4 | |
| | | | | $I_{OL} = 32\text{ mA}$ | | 0.5 | |
| | | | | $I_{OL} = 64\text{ mA}$ | | 0.55 | |
| I_I | | $V_{CC} = 0\text{ or }3.6\text{ V}$, Control inputs | | $V_I = 5.5\text{ V}$ | | 10 | μA |
| | | $V_{CC} = 3.6\text{ V}$, Data inputs | | $V_I = V_{CC}\text{ or GND}$ | | ± 1 | |
| | | $V_{CC} = 3.6\text{ V}$ | | $V_I = V_{CC}$ | | 1 | |
| | | | | $V_I = 0$ | | -5 | |
| I_{off} | | $V_{CC} = 0$, $V_I\text{ or }V_O = 0\text{ to }4.5\text{ V}$ | | | | ± 100 | μA |
| $I_{I(\text{hold})}$ | | $V_{CC} = 3\text{ V}$, Data inputs | | $V_I = 0.8\text{ V}$ | | 75 | μA |
| | | | | $V_I = 2\text{ V}$ | | -75 | |
| | | $V_{CC} = 3.6\text{ V}^\ddagger$, Data inputs | | $V_I = 0\text{ to }3.6\text{ V}$ | | ± 500 | |
| I_{OZH} | | $V_{CC} = 3.6\text{ V}$, $V_O = 3\text{ V}$ | | | | 5 | μA |
| I_{OZL} | | $V_{CC} = 3.6\text{ V}$, $V_O = 0.5\text{ V}$ | | | | -5 | μA |
| I_{OZPU} | | $V_{CC} = 0\text{ to }1.5\text{ V}$, $V_O = 0.5\text{ V to }3\text{ V}$, $\overline{OE} = \text{don't care}$ | | | | ± 100 | μA |
| I_{OZPD} | | $V_{CC} = 1.5\text{ V to }0$, $V_O = 0.5\text{ V to }3\text{ V}$, $\overline{OE} = \text{don't care}$ | | | | ± 100 | μA |
| I_{CC} | | $V_{CC} = 3.6\text{ V}$, $I_O = 0$, $V_I = V_{CC}\text{ or GND}$ | | Outputs high | | 0.19 | mA |
| | | | | Outputs low | | 5 | |
| | | | | Outputs disabled | | 0.19 | |
| ΔI_{CC}^\S | | $V_{CC} = 3\text{ V to }3.6\text{ V}$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at $V_{CC}\text{ or GND}$ | | | | 0.2 | mA |
| C_i | | $V_I = 3\text{ V or }0$ | | | | 3 | pF |
| C_o | | $V_O = 3\text{ V or }0$ | | | | 9 | pF |

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

| | | $V_{CC} = 3.3 \pm 0.3\text{ V}$ | | $V_{CC} = 2.7\text{ V}$ | | UNIT |
|--------------------|--|---------------------------------|-----|-------------------------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| f_{clock} | Clock frequency | 160 | | 160 | | MHz |
| t_w | Pulse duration, CLK high or low | 3 | | 3 | | ns |
| t_{su} | Setup time, data before CLK \uparrow | High or low | | 2 | | ns |
| t_h | Hold time, data after CLK \uparrow | High or low | | 0.1 | | ns |



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switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

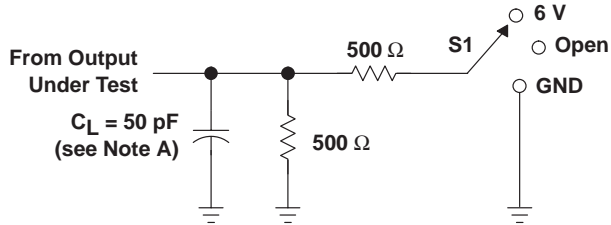
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | | | $V_{CC} = 2.7\text{ V}$ | | UNIT |
|-------------|-----------------|-------------|--|------|-----|-------------------------|-----|------|
| | | | MIN | TYP† | MAX | MIN | MAX | |
| f_{max} | | | 160 | | | 160 | | MHz |
| t_{PLH} | CLK | Q | 1.9 | 3 | 4.5 | | 5.2 | ns |
| t_{PHL} | | | 2.1 | 2.9 | 4 | | 4.2 | |
| t_{PZH} | \overline{OE} | Q | 1.5 | 2.8 | 4.5 | | 5.4 | ns |
| t_{PZL} | | | 1.5 | 2.8 | 4.4 | | 5 | |
| t_{PHZ} | \overline{OE} | Q | 2.4 | 3.5 | 5 | | 5.4 | ns |
| t_{PLZ} | | | 2 | 3.2 | 4.6 | | 4.8 | |
| $t_{sk(o)}$ | | | | | 0.5 | | | ns |

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

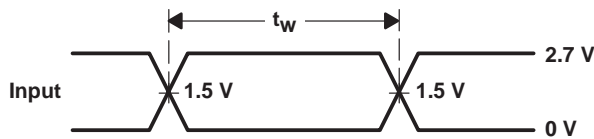
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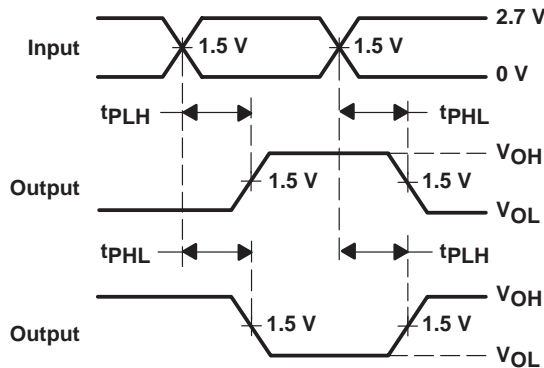
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

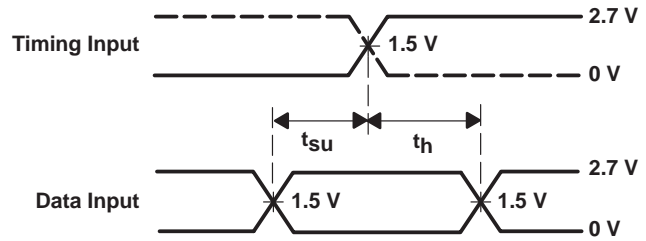


VOLTAGE WAVEFORMS
PULSE DURATION

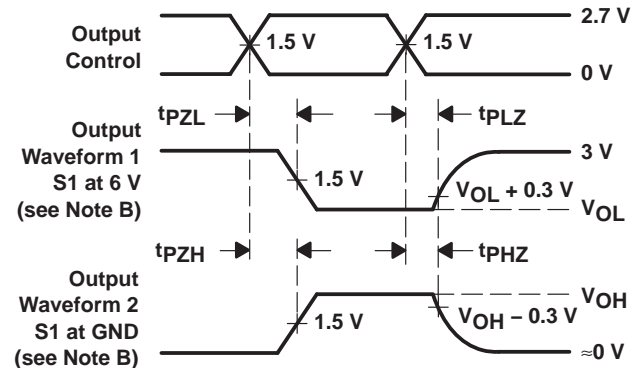


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

| TEST | S1 |
|-------------------|------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | 6 V |
| t_{PHZ}/t_{PZH} | GND |



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|-------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| CLVTH16374IDGGREP | ACTIVE | TSSOP | DGG | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CLVTH16374IDLREP | ACTIVE | SSOP | DL | 48 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| V62/04711-01XE | ACTIVE | TSSOP | DGG | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| V62/04711-01YE | ACTIVE | SSOP | DL | 48 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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- Catalog: [SN74LVTH16374](#)
- Military: [SN54LVTH16374](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CLVTH16374IDGGREP | TSSOP | DGG | 48 | 2000 | 330.0 | 24.4 | 8.6 | 15.8 | 1.8 | 12.0 | 24.0 | Q1 |
| CLVTH16374IDLREP | SSOP | DL | 48 | 1000 | 330.0 | 32.4 | 11.35 | 16.2 | 3.1 | 16.0 | 32.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CLVTH16374IDGGREP | TSSOP | DGG | 48 | 2000 | 346.0 | 346.0 | 41.0 |
| CLVTH16374IDLREP | SSOP | DL | 48 | 1000 | 346.0 | 346.0 | 49.0 |

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