NCP1370

Product Preview

Dimmable Quasi-Resonant Primary Side Current-Mode Controller for LED TV Backlight

The NCP1370 is a PWM current mode controller targeting isolated flyback and non−isolated constant current topologies. The controller operates in a quasi−resonant mode to provide high efficiency. Thanks to a novel control method, the device is able to precisely regulate a constant LED current from the primary side. This removes the need for secondary side feedback circuitry, biasing and an opto−coupler.

The device is highly integrated with a minimum number of external components. A robust suite of safety protection is built in to simplify the design. This device supports analog/digital dimming and both modes can be combined to enhance dimming precision. The NCP1370 has a programmable peak current limit to optimize design compatibility over a wide range of applications. The controller features a standby mode with reduced current consumption.

Features

- Quasi−resonant Peak Current−mode Control Operation
- Primary Side Sensing (no opto−coupler needed)
- Wide V_{CC} Range
- Source 300 mA / Sink 500 mA Totem Pole Driver with 12 V Gate Clamp
- Precise LED Constant Current Regulation ±1% Typical
- Line Feed−forward for Enhanced Regulation Accuracy
- Low LED Current Ripple
- 500 mV ±1.2% Guaranteed Voltage Reference for Current Regulation
- Programmable Cycle−by−Cycle Peak Current Limit
- Low $V_{CC(on)}$ Allowing to use a Standby Power Supply to Power the Device
- Analog or Digital Dimming
- Wide Temperature Range of −40 to + 125°C
- Robust Protection Features
  - LED Open Circuit Protection
  - V_{CC} Over Voltage Protection
  - Secondary Diode Short Protection
  - Output Short Circuit Protection
  - Shorted Current Sense Pin Fault Detection
  - Brown−out
  - V_{CC} Under Voltage Lockout
  - Thermal Shutdown
- Pb−free, Halide−free MSL1 Product

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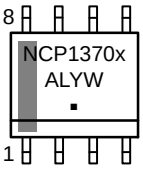
QUASI−RESONANT PWM CONTROLLER FOR LED DRIVERS

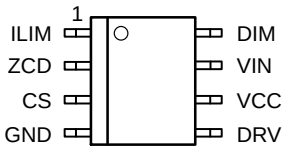
SOIC−8
D SUFFIX
CASE 751

MARKING DIAGRAM



NCP1370 = Specific Device Code
x = Device Option (A or B)
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 18 of this data sheet.

Typical Applications

- TV Backlight
- Lighting with Auxiliary Power Supply

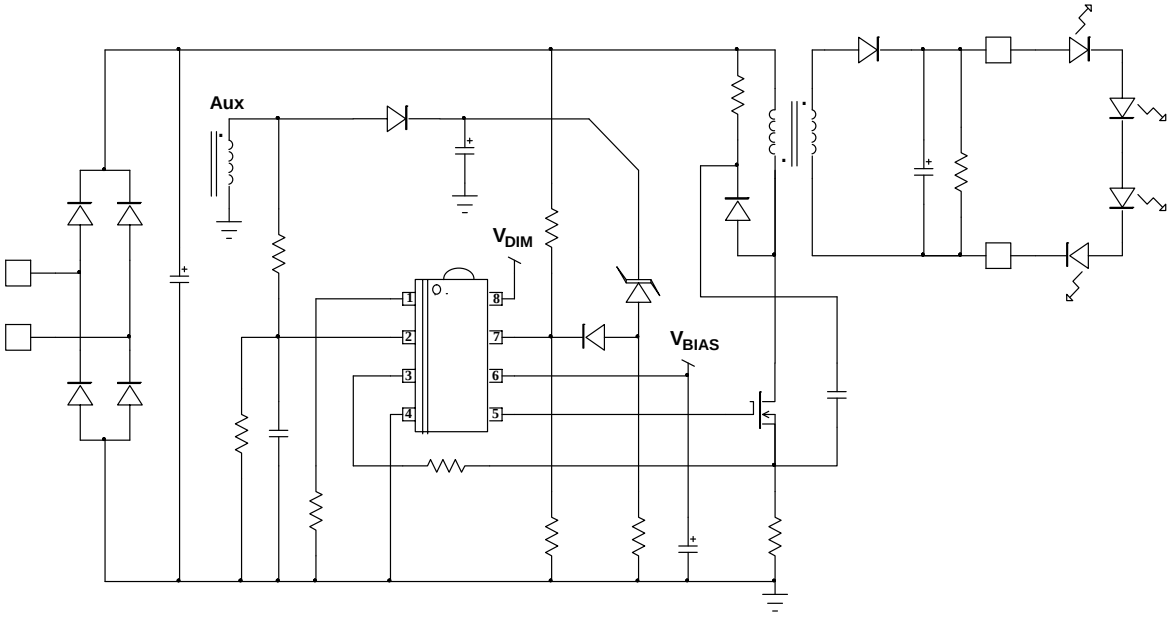


Figure 1. Typical Application Schematic for NCP1370

Table 1. PRODUCTS TABLE

Block or Electrical Parameter	NCP1370B	NCP1370A
Brown−out blanking time $t_{BO(blank)}$	100 μs	2 ms
Blanking circuit for leakage inductance reset detection	ON	ON
V_{CC} OVP	Auto−recovery	Latched
Switching cycles count before activating the output diode short circuit protection: $V_{CS} > V_{CS(stop)}$	4 cycles	4 cycles
Output Diode Short Circuit protection	Auto−recovery	Latched
Adjustable OVP Auto−recovery timer	1 second	4 seconds
CS short circuit protection (impedance measurement before startup)	ON	OFF
High mains valley switching	3rd (all HL valleys incremented by 1)	2nd
Propagation delay from ZCD to DRV high state $t_{ZCD(DEM)}$	ON	ON

Table 2. PIN FUNCTION DESCRIPTION

Pin N°	Pin Name	Function	Pin Description
1	ILIM	Peak current limit and 2nd over current protection	This pin sets the cycle−by−cycle peak current limit threshold and the threshold for secondary diode short detection
2	ZCD	Zero Crossing Detection	Connected to the auxiliary winding, this pin detects the core reset event.
3	CS	Current sense	This pin monitors the primary peak current.
4	GND	−	The controller ground
5	DRV	Driver output	The driver's output to an external MOSFET
6	VCC	Supplies the controller	This pin is connected to an external power supply.
7	VIN	Brown−Out Input voltage sensing Over Voltage Protection	This pin observes the HV rail and protects the circuit in case of low main conditions. This pin also sense the line voltage for the valley selection and the line feed−forward A Zener diode can also be used to pull−up the pin and stop the controller for adjustable OVP protection
8	DIM	Analog / PWM dimming	This pin is used for analog or PWM dimming control. An analog signal than can be varied between $V_{DIM(EN)}$ and V_{DIM100} can be used to vary the current, or a PWM signal with an amplitude greater than V_{DIM100}. This pin is also used for the OFF mode

Internal Circuit Architecture

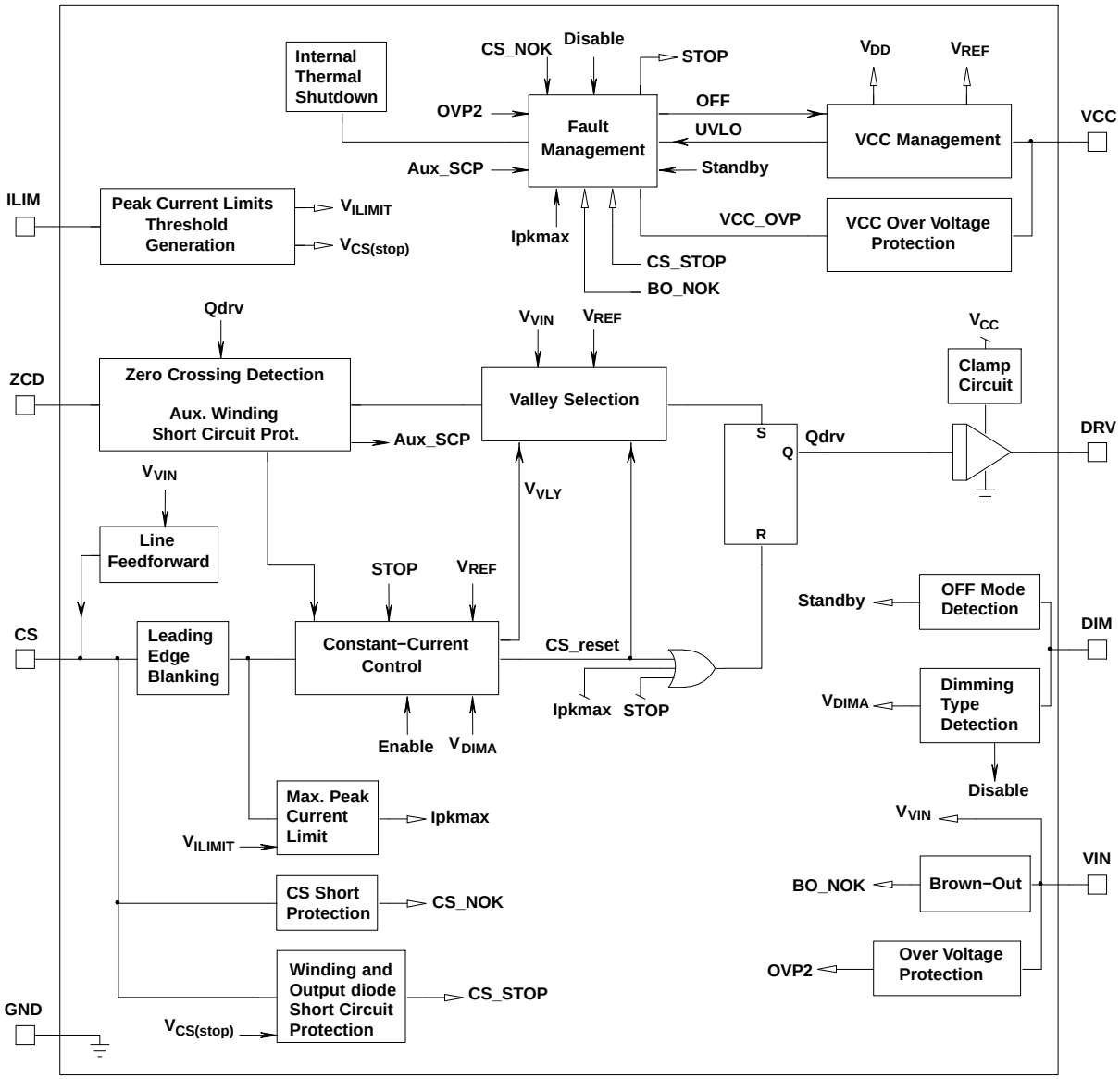


Figure 2. Internal Circuit Architecture

Table 3. MAXIMUM RATINGS TABLE

Symbol	Rating	Value	Unit
$V_{CC(MAX)}$ $I_{CC(MAX)}$	Maximum Power Supply voltage, VCC pin, continuous voltage Maximum current for VCC pin	−0.3, +35 Internally limited	V mA
$V_{DRV(MAX)}$ $I_{DRV(MAX)}$	Maximum driver pin voltage, DRV pin, continuous voltage Maximum current for DRV pin	−0.3, V_{DRV} (Note 1) −500, +800	V mA
V_{MAX} I_{MAX}	Maximum voltage on low power pins (except pins DIM, DRV and VCC) Current range for low power pins (except pins DRV and VCC)	−0.3, +5.5 −2, +5	V mA
$V_{DIM(MAX)}$	Maximum voltage for DIM pin	−0.3, +7	V
$R_{\theta J-A}$	Thermal Resistance Junction−to−Air	289	°C/W
$T_{J(MAX)}$	Maximum Junction Temperature	150	°C
	Operating Temperature Range	−40 to +125	°C
	Storage Temperature Range	−60 to +150	°C
	ESD Capability, HBM model (Note 2)	4	kV
	ESD Capability, MM model (Note 2)	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. V_{DRV} is the DRV clamp voltage $V_{DRV(high)}$ when V_{CC} is higher than $V_{DRV(high)}$. V_{DRV} is V_{CC} unless otherwise noted.
2. This device series contains ESD protection and exceeds the following tests: Human Body Model 4000 V per Mil−Std−883, Method 3015.
3. This device contains latch−up protection and exceeds 100 mA per JEDEC Standard JESD78

Table 4. ELECTRICAL CHARACTERISTICS (Unless otherwise noted: For typical values T_J = 25°C, V_{CC} = 12 V)
For min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{CC} = 12 V)

Description	Test Condition	Symbol	Min	Typ	Max	Unit
STARTUP AND SUPPLY CIRCUITS						
Supply Voltage Startup Threshold Minimum Operating Voltage Hysteresis $V_{CC(on)}$ − $V_{CC(off)}$ Internal logic reset equal to $V_{CC(off)}$	 V_{CC} increasing V_{CC} decreasing V_{CC} decreasing	 $V_{CC(on)}$ $V_{CC(off)}$ $V_{CC(HYS)}$ $V_{CC(reset)}$	 11 9 1.8 9	 12 9.5 − 9.5	 13 10 − 10	V
Over Voltage Protection VCC OVP threshold		$V_{CC(OVP)}$	26	28	30	V
$V_{CC(off)}$ noise filter $V_{CC(reset)}$ noise filter		$t_{VCC(off)}$ $t_{VCC(reset)}$	− −	5 20	− −	μs
Startup current		$I_{CC(start)}$	−	−	100	μA
Starting time from exiting OFF Mode to 1st DRV pulse		$t_{CC(start)}$		−	250	μs
Supply Current Device Disabled/Fault Device Enabled/No output load on pin 5 Device Switching (F_{sw} = 65 kHz)	 V_{CC} > $V_{CC(off)}$ F_{sw} = 65 kHz C_{DRV} = 470 pF, F_{sw} = 65 kHz	 I_{CC1} I_{CC2} I_{CC3}	 0.8 − −	 1.2 2.3 2.7	 1.4 4.0 5.0	mA
Supply Current in OFF mode		$I_{CC(off)}$			50	μA
CURRENT SENSE AND ILIM PIN						
Reference current for maximum peak current limit threshold		$I_{LIM(REF)}$	190	200	210	μA
Minimum value for internal V_{ILIMIT}	$V_{pinILIM}$ < 0.5 V	$V_{ILIMIT(MIN)}$		0.5		V
Maximum value for internal V_{ILIMIT}	Pin ILIM open	$V_{ILIMIT(MAX)}$	2.34	2.6	2.86	V
Difference between internal V_{ILIMIT} and ILIM pin voltage	$V_{pinILIM}$ = 1.5 V	$V_{ILIMIT(offset)}$	−30		30	mV
$V_{CS(stop)}$ at $V_{pinILIM}$ = 1.5 V	$V_{pinILIM}$ = 1.5 V	$V_{CS(stop)1}$	2.037	2.1	2.163	V
Leading Edge Blanking Duration for V_{ILIM} (T_j = −40°C to 125°C)		t_{LEB}	280	330	380	ns
Minimum on−time (equal to t_{LEB})		$t_{on(MIN)}$	280	330	380	ns
Propagation delay from current detection to gate off−state		t_{ILIM}	−	50	150	ns
Maximum on−time		$t_{on(MAX)}$	37.5	50	62.5	μs

4. Guaranteed by design

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For min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{CC} = 12 V)

Description	Test Condition	Symbol	Min	Typ	Max	Unit
CURRENT SENSE AND ILIM PIN						
Minimum threshold value for immediate fault protection activation	$V_{pinILIM}$ < 0.5 V	$V_{CS(stop)MIN}$		0.7		V
Minimum threshold value for immediate fault protection activation	Pin ILIM open	$V_{CS(stop)MAX}$		3.64		V
Ratio between internal $V_{CS(stop)}$ and internal V_{ILIMIT}		$K_{STOP/ILIMIT}$		140		%
Leading Edge Blanking Duration for $V_{CS(stop)}$		t_{BCS}	–	200	–	ns
Current source for CS to GND short detection		$I_{CS(short)}$	400	500	600	μA
Timer for measuring CS to GND short		$t_{CS(short)}$	12	17	22	μs
GATE DRIVE						
Drive Resistance DRV Sink DRV Source		 R_{SNK} R_{SRC}	 – –	 13 30	 – –	Ω
Drive current capability DRV Sink (Note 4) DRV Source (Note 4)		 I_{SNK} I_{SRC}	 – –	 500 300	 – –	mA
Rise Time (10 % to 90 %)	C_{DRV} = 470 pF	t_r	–	40	–	ns
Fall Time (90 % to 10 %)	C_{DRV} = 470 pF	t_f	–	30	–	ns
DRV Low Voltage	V_{CC} = $V_{CC(off)}$+0.2 V C_{DRV} = 470 pF, R_{DRV}=33 kΩ	$V_{DRV(low)}$	8	–	–	V
DRV High Voltage	V_{CC} = 30 V C_{DRV} = 470 pF, R_{DRV}=33 kΩ	$V_{DRV(high)}$	10	12	14	V
ZERO VOLTAGE DETECTION CIRCUIT						
ZCD threshold voltage	V_{ZCD} increasing	$V_{ZCD(THI)}$	30	50	70	mV
ZCD threshold voltage (Note 4)	V_{ZCD} decreasing	$V_{ZCD(THD)}$	20	40	60	mV
ZCD hysteresis (Note 4)	V_{ZCD} increasing	$V_{ZCD(HYS)}$	8	–	–	mV
Threshold voltage for output short circuit or aux. winding short circuit detection		$V_{ZCD(short)}$	0.8	1	1.2	V
Short circuit detection Timer	V_{ZCD} < $V_{ZCD(short)}$	t_{OVLD}	70	90	110	ms
Auto−recovery timer duration		$t_{recovery}$	3	4	5	s
Input clamp voltage High state Low state	 I_{pin1} = 3.0 mA I_{pin1} = −2.0 mA	 $V_{ZCD(CH)}$ $V_{ZCD(CL)}$	 – −0.9	 8 −0.6	 – −0.3	V
Propagation Delay from valley detection to DRV high	V_{ZCD} decreasing	$t_{ZCD(DEM)}$	−	−	480	ns
Delay from valley lockout output to DRV latch set	V_{ZCD} decreasing	t_{LEB4}	125	250	375	ns
Blanking delay after on−time	V_{REF} > 100 mV	$t_{ZCD(BLANK1)}$	1.2	1.6	2	μs
Blanking delay after on−time at light load	V_{REF} < 75 mV	$t_{ZCD(BLANK2)}$	0.6	0.8	1	μs
Timeout after last demag transition		t_{TIMO}	5	6.5	8	μs
LINE FEED−FORWARD						
V_{VIN} to $I_{CS(offset)}$ conversion ratio		K_{LFF}	15	17	19	μA/V
Offset current maximum value	V_{pinVIN} = 4.5 V	$I_{offset(MAX)}$	67.5	76.5	85.5	μA
CONSTANT CURRENT CONTROL						
Reference Voltage (after division by 2) (T_j = 25°C)		V_{REF}	495	500	505	mV
Reference Voltage (after division by 2) (T_j = 0°C to 85°C)		V_{REF}	492	500	508	mV
Reference Voltage (after division by 2) (T_j =−40°C to 125°C)		V_{REF}	488	500	512	mV

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For min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{CC} = 12 V)

Description	Test Condition	Symbol	Min	Typ	Max	Unit
CONSTANT CURRENT CONTROL						
Current sense lower threshold for detection of the leakage inductance reset time		$V_{CS(low)}$	25	55	85	mV
Blanking time for leakage inductance reset detection		$t_{CS(low)}$		130		ns
V_{REF} value below which the ZCD blanking time is divided by 2 (light load)	V_{REF} decreases	$V_{REF(off)}$		75		mV
V_{REF} value above which ZCD blanking time is $t_{ZCD(blank1)}$	V_{REF} increases	$V_{REF(on)}$		100		mV
VALLEY SELECTION						
Threshold for line range detection V_{in} increasing (1st to 2nd valley or 1st to 3rd transition for V_{REF} > 0.375 V)	V_{VIN} increases	V_{HL}	2.28	2.4	2.52	V
Threshold for line range detection V_{in} decreasing (2nd to 1st valley or 1st to 3rd transition for V_{REF} > 0.375 V)	V_{VIN} decreases	V_{LL}	2.18	2.3	2.42	V
Blanking time for line range detection		$t_{HL(blank)}$	15	25	35	ms
Valley thresholds (V_{REF} = 500 mV)						mV
1st to 2nd valley transition at LL and 2nd to 3rd valley HL (3rd to 4th valley HL for version B) V_{REF} decreases	V_{REF} decreases	$V_{VLY1-2/2-3}$	350	373	396	
2nd to 1st valley transition at LL and 3rd to 2nd valley HL (4th to 3rd valley HL for version B), V_{REF} incr.	V_{REF} increases	$V_{VLY2-1/3-2}$	366	390	414	
2nd to 4th valley transition at LL and 3rd to 5th valley HL (4th to 6th valley HL for version B), V_{REF} decr.	V_{REF} decreases	$V_{VLY2-4/3-5}$	231	248	265	
4th to 2nd valley transition at LL and 5th to 3rd valley HL (6th to 4th valley HL for version B), V_{REF} incr.	V_{REF} increases	$V_{VLY4-2/5-3}$	249	267	285	
4th to 7th valley transition at LL and 5th to 8th valley HL (6th to 9th valley HL for version B), V_{REF} decr.	V_{REF} decreases	$V_{VLY4-7/5-8}$	–	150	–	
7th to 4th valley transition at LL and 8th to 5th valley HL (9th to 6th valley HL for version B), V_{REF} incr.	V_{REF} increases	$V_{VLY7-4/8-5}$	–	165	–	
7th to 11th valley transition at LL and 8th to 12th valley HL (9th to 13th valley HL for version B), V_{REF} decr.	V_{REF} decreases	$V_{VLY7-11/8-12}$	–	75	–	
11th to 7th valley transition at LL and 12th to 8th valley HL (13th to 9th valley HL for version B), V_{REF} incr.	V_{REF} increases	$V_{VLY11-7/12-8}$	–	100	–	
11th to 13th valley transition at LL and 12th to 15th valley HL (13th to 16th valley HL for version B), V_{REF} decr.	V_{REF} decreases	$V_{VLY11-13/12-15}$	–	30	–	
13th to 11th valley transition at LL and 15th to 12th valley HL (16th to 13th valley HL for version B), V_{REF} incr.	V_{REF} increases	$V_{VLY13-11/15-12}$	–	40	–	
Valley thresholds in percentage of V_{REF}						%
1st to 2nd valley transition at LL and 2nd to 3rd valley HL (3rd to 4th valley HL for version B) V_{REF} decreases	V_{REF} decreases	$V_{VLY1-2/2-3}$	70	74.5	79	
2nd to 1st valley transition at LL and 3rd to 2nd valley HL (4th to 3rd valley HL for version B), V_{REF} incr.	V_{REF} increases	$V_{VLY2-1/3-2}$	73	78	83	
2nd to 4th valley transition at LL and 3rd to 5th valley HL (4th to 6th valley HL for version B), V_{REF} decr.	V_{REF} decreases	$V_{VLY2-4/3-5}$	46	49.5	53	
4th to 2nd valley transition at LL and 5th to 3rd valley HL (6th to 4th valley HL for version B), V_{REF} incr.	V_{REF} increases	$V_{VLY4-2/5-3}$	50	53.5	57	
4th to 7th valley transition at LL and 5th to 8th valley HL (6th to 9th valley HL for version B), V_{REF} decr.	V_{REF} decreases	$V_{VLY4-7/5-8}$	–	30	–	
7th to 4th valley transition at LL and 8th to 5th valley HL (9th to 6th valley HL for version B), V_{REF} incr.	V_{REF} increases	$V_{VLY7-4/8-5}$	–	33	–	
7th to 11th valley transition at LL and 8th to 12th valley HL (9th to 13th valley HL for version B), V_{REF} decr.	V_{REF} decreases	$V_{VLY7-11/8-12}$	–	15	–	
11th to 7th valley transition at LL and 12th to 8th valley HL (13th to 9th valley HL for version B), V_{REF} incr.	V_{REF} increases	$V_{VLY11-7/12-8}$	–	20	–	
11th to 13th valley transition at LL and 12th to 15th valley HL (13th to 16th valley HL for version B), V_{REF} decr.	V_{REF} decreases	$V_{VLY11-13/12-15}$	–	6	–	
13th to 11th valley transition at LL and 15th to 12th valley HL (16th to 13th valley HL for version B), V_{REF} incr.	V_{REF} increases	$V_{VLY13-11/15-12}$	–	8	–	

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For min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{CC} = 12 V)

Description	Test Condition	Symbol	Min	Typ	Max	Unit
DIMMING SECTION						
DIM pin voltage for zero output current (OFF voltage)	V_{DIM} decreasing	$V_{DIM(EN)}$	0.67	0.7	0.73	V
$V_{DIM(EN)}$ comparator hysteresis	V_{DIM} increasing	$V_{EN(HYS)}$	−	50	−	mV
DIM pin voltage for maximum output current (T_J = −40 to 125°C)		V_{DIM100}	2.9	3	3.1	V
DIM pin voltage for maximum output current at T_J = 25°C		V_{DIM100}	2.94	3	3.06	V
Dimming range		$V_{DIM(range)}$	–	2.3	–	V
Clamping voltage for DIM pin		$V_{DIM(CLP)}$	–	7	–	V
Dimming pin pull−up current source		$I_{DIM(pullup)}$	–	5	–	μA
THERMAL SHUTDOWN						
Thermal Shutdown (Note 4)	Device switching (F_{SW} around 65 kHz)	T_{SHDN}	130	150	170	°C
Thermal Shutdown Hysteresis (Note 4)		$T_{SHDN(HYS)}$	–	50	–	°C
BROWN−OUT AND OVP						
Brown−Out ON level (IC start pulsing)	V_{VIN} increasing	$V_{BO(on)}$	0.90	1	1.10	V
Brown−Out OFF level (IC shuts down)	V_{VIN} decreasing	$V_{BO(off)}$	0.85	0.9	0.95	V
BO comparators delay		$t_{BO(delay)}$	–	30	–	μs
Brown−Out blanking time for version A		$t_{BO(blank1)}$	1.4	2	2.6	ms
Brown−Out blanking time for version B		$t_{BO(blank2)}$	50	100	150	μs
Brown−out pin bias current		$I_{BO(bias)}$	−250	–	250	nA
Clamped voltage (VIN pin left open)	VIN pin open	$V_{VIN(clamp)}$	3.9	4.1	4.3	V
VIN pin Clamp series resistor		$R_{VIN(clamp)}$		1		kΩ
VIN pin detection level for OVP	V_{VIN} increasing	V_{OVP}	4.75	5	5.25	V
Delay before OVP confirmation		$t_{OVP(delay)}$		50		μs
Adjustable OVP auto−recovery timer (version B)		$t_{OVP(recovery1)}$		1		s
Adjustable OVP auto−recovery timer (version A)		$t_{OVP(recovery2)}$		4		s

4. Guaranteed by design

Application Information

The NCP1370 is a LED driver for flyback and non−isolated buck−boost / SEPIC converters. It implements a current−mode architecture quasi−resonant architecture to prevent valley−jumping instability. A proprietary circuitry ensures accurate regulation of the output current without the need of a secondary side feedback. The circuit features powerful protections to ensure a robust LED driver design without the need of extra external components or overdesign.

- **Quasi−Resonance Current−Mode Operation:** implementing quasi−resonance operation in peak current−mode control, the NCP1370 optimizes the efficiency by switching in the valley of the MOSFET drain−source voltage. Thanks to smart control algorithm, the controller locks−out in a selected valley and remains locked until the input voltage or the output current set point significantly changes.
- **Primary Side Constant Current Control:** thanks to a proprietary circuit, the controller accurately controls the output current without requiring a secondary side feedback (no optocoupler needed). An output current deviation below ±2% is typically obtained.
- **V_{CC} Over Voltage Protection:** if the voltage on VCC pin exceeds an internal limit, the controller shuts down and waits 4 seconds before restarting pulsing (version B) or stays latched (A version).
- **Adjustable peak current limit:** the cycle−by−cycle maximum peak current limit and the second over current protection level can be adjusted externally by connecting a resistor between ILIM pin and ground.
- **Brown−Out:** the controller includes a brown−out circuit which safely stops the controller in case the input voltage is too low. The device will automatically restart if the line recovers.
- **Adjustable Over voltage protection:** By connecting a zener diode to the VIN pin, an adjustable over voltage protection can be implemented to protect against open LEDs. Upon detection, the controller waits 4 s (version A) or 1 s (version B) before attempting to restart switching.
- **Cycle−by−cycle peak current limit:** when the current sense voltage exceeds pin ILIM voltage V_{ILIM}, the MOSFET is turned off for the rest of the switching cycle.
- **Winding Short−Circuit Protection (2^{nd} over current protection level):** an additional comparator with a short LEB filter (t_{BCS}) senses the CS signal and stops the controller if V_{CS} reaches 140% of V_{ILIMIT}). For noise immunity reasons, this comparator is enabled only during the main LEB duration t_{LEB}.
- **Output Short−circuit protection:** If a very low voltage is applied on ZCD pin for 90 ms (nominal), the controllers assume that the output or the ZCD pin is shorted to ground and enters shutdown. After waiting for 4 seconds, the controller restarts switching.
- **Linear or PWM dimming:** the DIM pin allows implementing both analog and PWM dimming.
- **OFF Mode:** The IC enters in OFF mode after detecting a fault and whenever the DIM pin voltage stays low during more than 4 seconds. In this mode, the IC is off and has a reduced current consumption. This allows simplifying the PCB design around the ON/OFF opto−coupler.
- **Floating or Short pin detection:** The NCP1370 protections help passing safety tests. For instance, the circuit stops operating when the CS pin is grounded or when the GND pin is open.

Constant Current Control

Capitalizing on the constant current control technique developed in the NCL3008X product, the NCP1370 accurately regulates the output current of a flyback converter from its primary side.

By connecting the clamping capacitor of the flyback converter to the sense resistor as shown in the typical application schematic (Figure 1), we have an image of the drain current waveform and of the leakage inductance current waveform. Thus, by looking at the current sense pin waveform, the controller is able to detect the reset of the transformer leakage inductance. Indeed, the leakage inductance limits the output rectifier peak current as shown in Figure 3 where it is shown that: $N_{sp} * I_{D,pk} < I_{L,pk}$.

Also, by monitoring the auxiliary winding voltage through the ZCD pin, we can detect the end of conduction of the secondary rectifier.

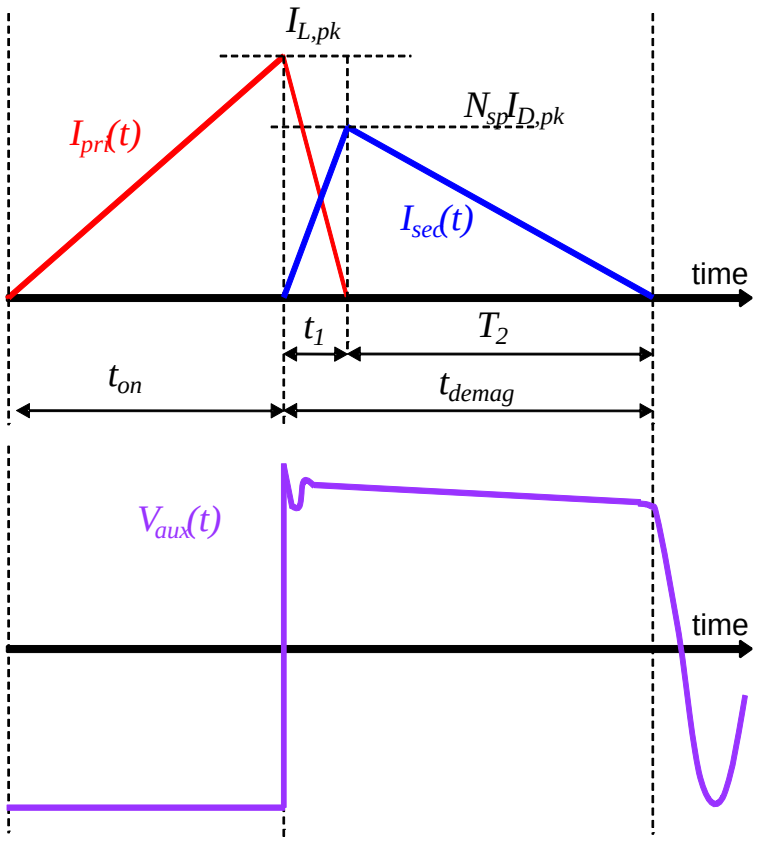


Figure 3. Flyback Currents and Auxiliary Winding Voltage in DCM

The constant current control block picks up the leakage inductor current, the end of conduction of the output rectifier and controls the drain current to maintain the output current constant.

We have:

$$I_{out} = \frac{V_{REF}}{2N_{sp}R_{sense}} \quad \text{(eq. 1)}$$

Where:

- V_{REF} is the output current internal reference
- N_{sp} is the secondary to primary transformer turns ratio: $N_{sp} = N_s / N_p$
- R_{sense} is the current sense resistor

The output current value is set by choosing the sense resistor:

$$R_{sense} = \frac{V_{REF}}{2N_{sp}I_{out}} \quad \text{(eq. 2)}$$

From (Equation 1), the first key point is that the output current is independent of the inductor value. Moreover, the leakage inductance does not influence the output current value as the reset time is taken into account by the controller.

Soft−Start

At startup or after recovering from a fault, there is a small internal soft−start of 200 μs maximum.

In addition, during startup, as the output voltage is zero volts, the demagnetization time is long and the constant current control block will slowly increase the peak current towards its nominal value as the output voltage grows. Figure 5 shows a soft−start simulation example for a 9 W LED power supply.

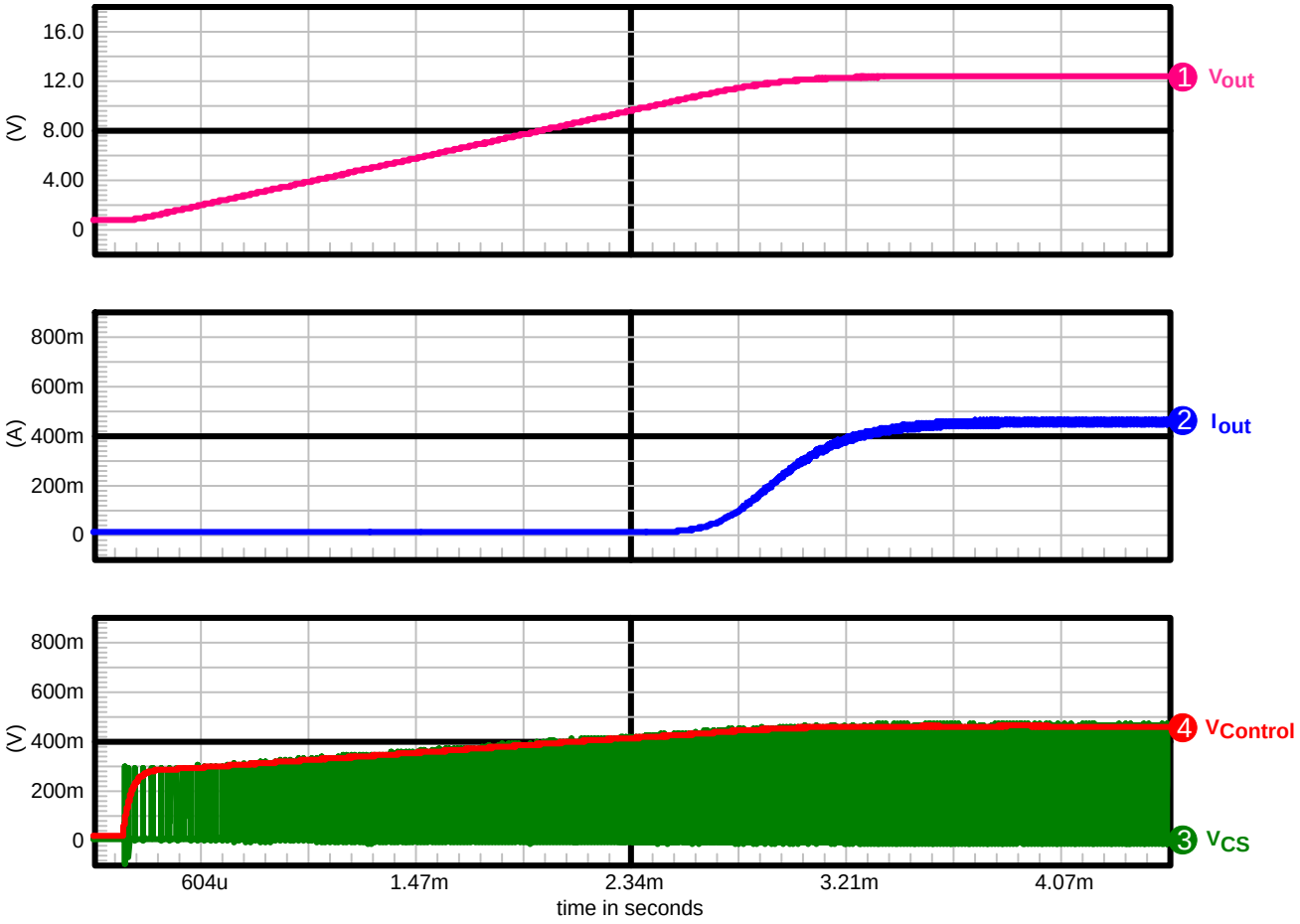


Figure 4. Startup Simulation showing the Natural Soft−start

Adjustable Cycle−by−Cycle Current Limit

The pin ILIM allows adjusting the threshold for maximum peak current limit V_{ILIMIT} and also the 2nd over current protection (OCP2) threshold $V_{CS(stop)}$ which helps protecting against short circuit of the secondary winding or of the output diode.

More precisely, the maximum peak current threshold V_{ILIMIT} is equal to the ILIM pin voltage and $V_{CS(stop)}$ value is derived from V_{ILIMIT}. By connecting a resistor between ILIM and GND pins, the value of internal cycle−by−cycle current limit V_{ILIMIT} is:

$$V_{ILIMIT} = V_{ILIM} = I_{LIM(REF)}R_{ILIM} \quad \text{(eq. 3)}$$

The threshold for immediate short circuit protection $V_{CS(stop)}$ is given by:

$$V_{CS(stop)} = 1.4 \cdot V_{ILIMIT} \quad \text{(eq. 4)}$$

Practically, V_{ILIMIT} can be adjusted from 0.5 V to 2.6 V, meaning $V_{CS(stop)}$ range is from 0.7 V to 3.64 V.

When the current sense voltage exceeds the internal threshold V_{ILIMIT}, the MOSFET is turned off for the rest of the switching cycle. Figure 5 shows the schematic of ILIM pin.

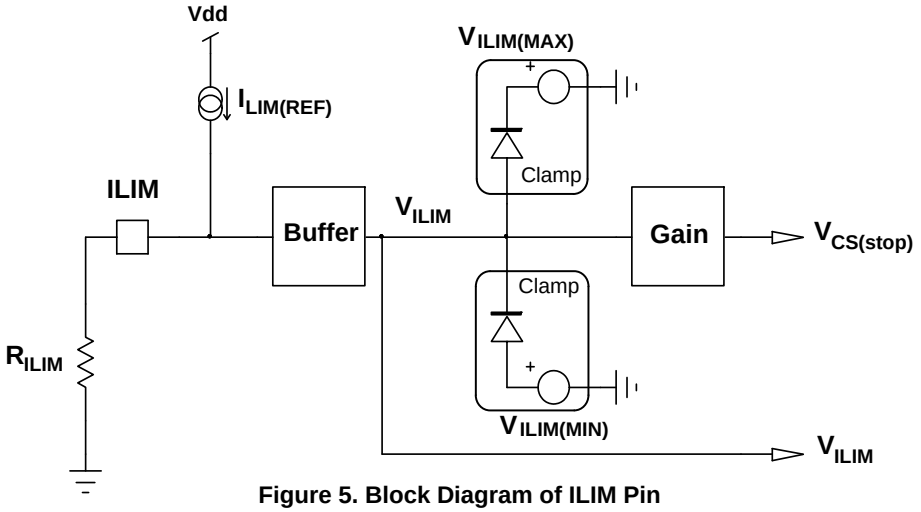


Figure 5. Block Diagram of ILIM Pin

The cycle−by−cycle peak current limit threshold V_{ILIMIT} also set the maximum duty cycle for a given application.

The maximum duty cycle is given by:

$$D_{MAX} = 1 - \frac{V_{REF}}{V_{ILIMIT}} - \frac{t_v}{T_{sw}} \quad \text{(eq. 5)}$$

Where:

- t_v is the valley duration
- T_{sw} is the switching period

For switching frequencies below 100 kHz, the term t_v/T_{sw} can be neglected:

$$D_{MAX} \approx 1 - \frac{V_{REF}}{V_{ILIMIT}} \quad \text{(eq. 6)}$$

Winding and Output diode Short−Circuit Protection (OCP2)

In parallel with the cycle−by−cycle sensing of the CS pin, another comparator with a reduced LEB (t_{BCS}) and a higher threshold ($V_{CS(stop)}$) is able to sense winding short−circuit and stop the controller. In version B, the controller stops the DRV pulses after counting 4 cycles of $V_{CS} > V_{CS(stop)}$. The controller attempts to re−start after waiting 4 seconds. In version A, after counting 4 cycles of $V_{CS} > V_{CS(stop)}$, the controller stays latched.

The controller is unlatched by one of the 3 following events:

- $V_{CC} < V_{CC(off)}$
- Standby by $V_{DIM} < V_{DIM(EN)}$ during 4 seconds
- BO_NOK becomes high

After being unlatched, the controller goes into OFF Mode.

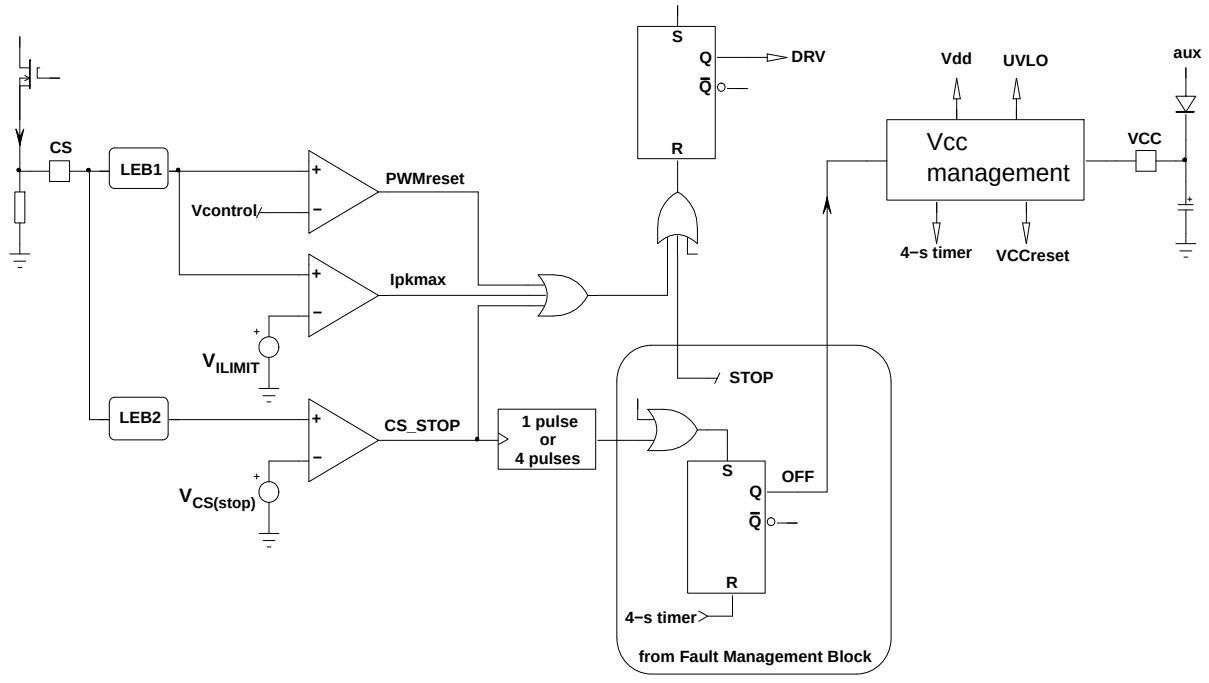


Figure 6. Winding Short Circuit Protection, Max. Peak Current Limit Circuits

PWM or Linear Dimming Detection

The pin DIM allows dimming the LED light. Analog dimming or digital (PWM) dimming can be used.

If the power supply designer apply an analog signal varying from $V_{DIM(EN)}$ to V_{DIM100} to the DIM pin, the output current will increase or decrease proportionally to the voltage applied. For $V_{DIM} = V_{DIM100}$, the power supply delivers the maximum output current.

If a voltage lower than $V_{DIM(EN)}$ is applied to the DIM pin, the DRV pulses are disabled. Thus, for digital dimming, a PWM signal with a low state value lower than $V_{DIM(EN)}$ and a high state value higher than V_{DIM100} should be applied.

The DIM pin is pulled up internally by a small current source or resistor. Thus, if the pin is left open, the controller is able to start.

Soft Stop during PWM Dimming

The NCP1370 features an internal soft−stop of 200 µs maximum in order to compensate the output current decrease caused by the soft−start during PWM dimming. Practically, when $V_{DIM} < V_{DIM(EN)}$, the controller decreases the peak current from its current state to nearly zero before stopping the DRV pulses.

This allows having a very good correlation between the dimming duty−cycle and the output current value when dimming at low duty−cycle.

Also, it is important to note that for good correlation between the dimming duty−cycle (which represent the expected output current value relative to the nominal value) and the actual measured output current, the high state duration of the dimming signal should not be below 200 µs.

Figure 8 shows the drain source waveform during soft−stop.

OFF Mode with DIM Pin

The OFF Mode is entered when V_{DIM} stays below $V_{DIM(EN)}$ for 4 seconds. In this mode, IC consumption is reduced to $I_{CC(off)}$ (below 50 µA). The OFF mode is exited only when V_{DIM} becomes higher than $V_{DIM(EN)}+V_{EN(HYS)}$.

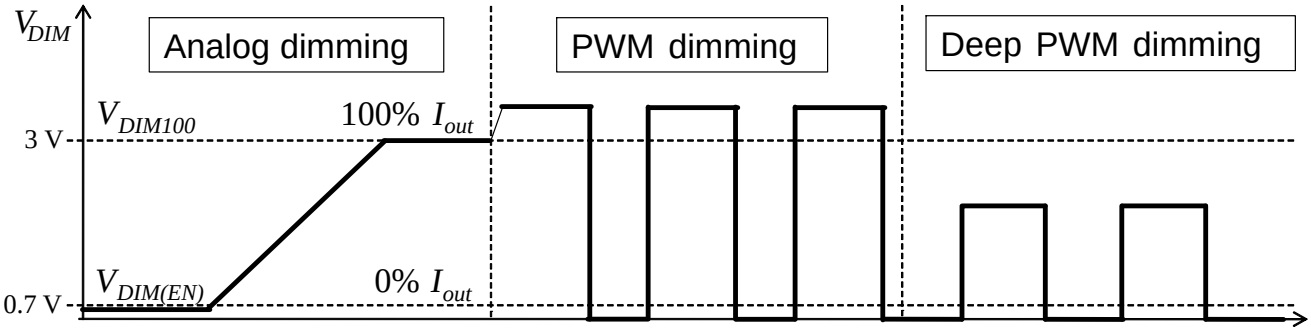


Figure 7. Pin DIM Chronograms

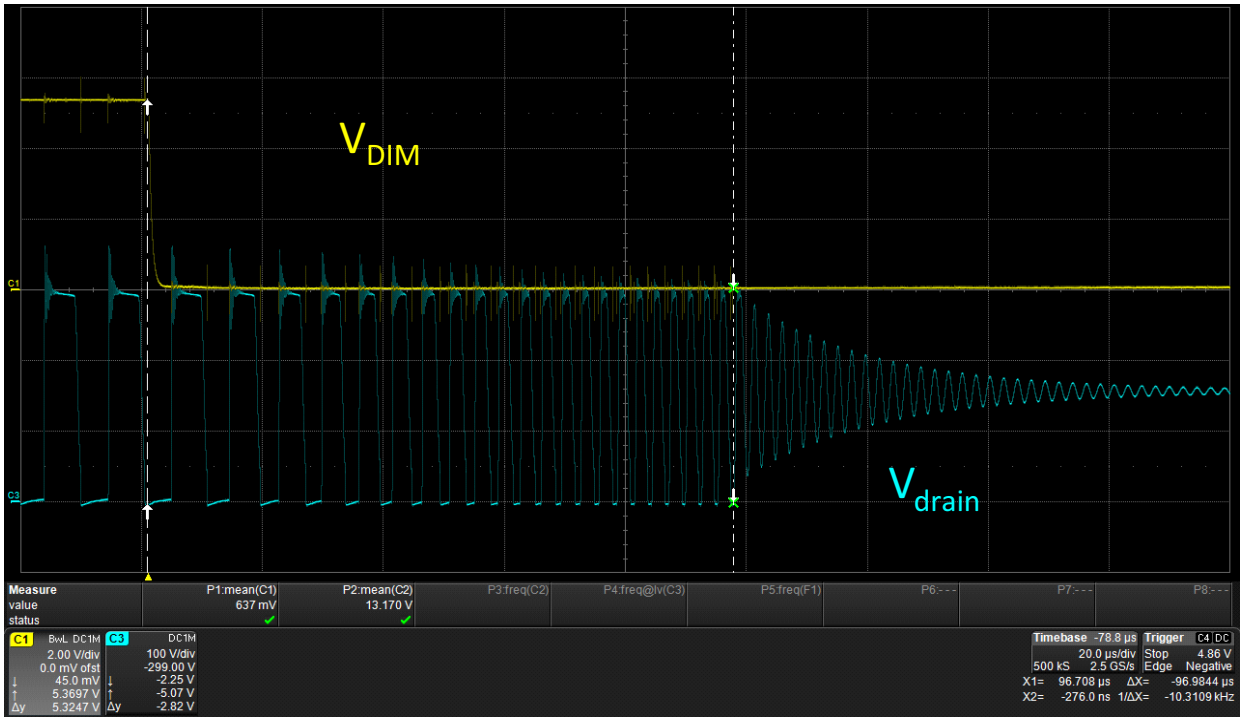


Figure 8. Soft−stop

V_{CC} Over Voltage Protection

In order to protect itself against too high supply voltage, the controller features an over voltage protection for the V_{CC} pin. When the V_{CC} voltage reaches the $V_{CC(OVP)}$ threshold, the controller stops the DRV pulses and shutdown. Depending on the version, the controller goes in auto−recovery mode (version B) or in latched mode (version A).

In the auto−recovery mode, the controller waits 4 s and tries to re−start. In order to restart pulsing, the controller goes through a complete sequence OFF Mode → FAULT Mode (see Fault Management section for more information)

In the latched mode, the controller stops pulsing and waits that one of the 3 following events occurs to reset the latch:

- $V_{CC} < V_{CC(off)}$
- Standby by $V_{DIM} < V_{DIM(EN)}$ during 4 seconds
- BO_NOK becomes high

When the OVP Latch is reset, the controller goes into OFF Mode.

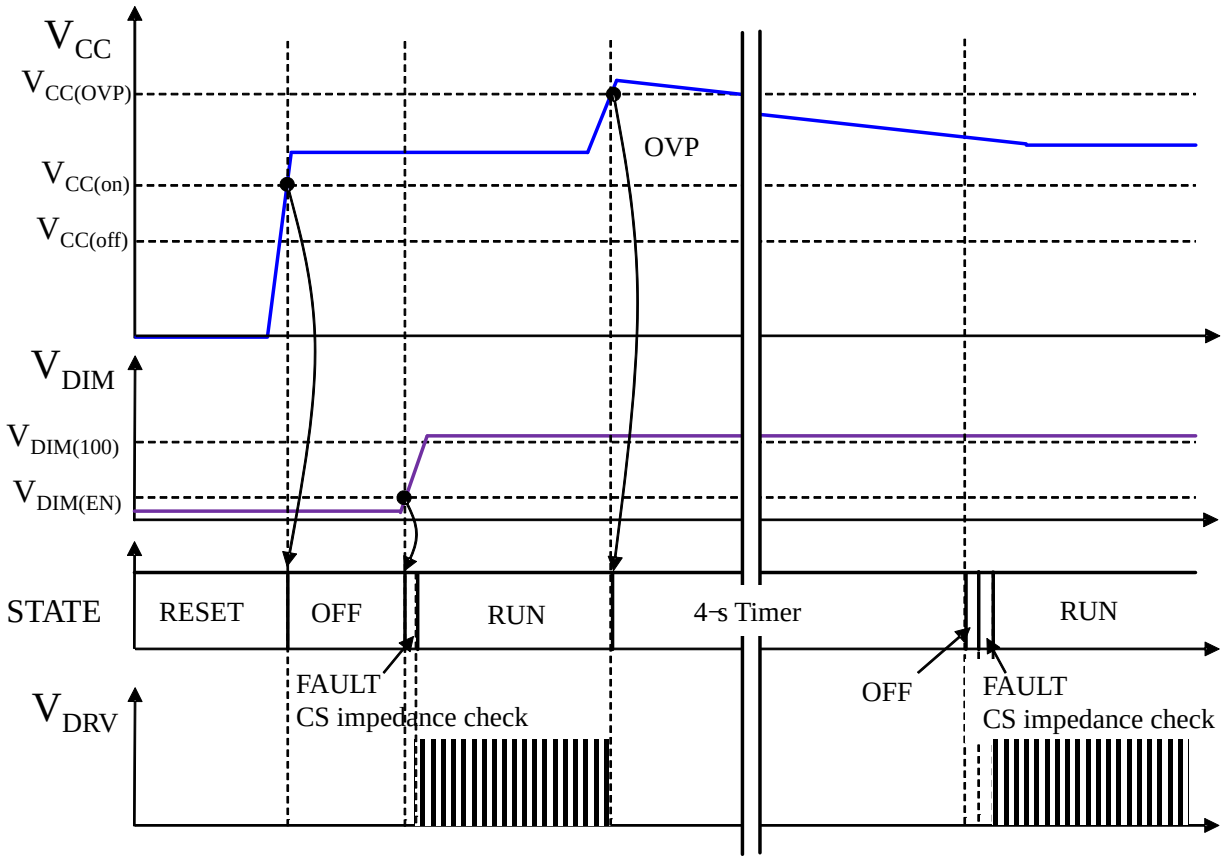


Figure 9. V_{CC} Over Voltage Protection Chronograms

Valley Selection

Quasi−Square wave resonant systems have a wide switching frequency excursion. The switching frequency increases when the output load decreases or when the input voltage increases. The switching frequency of such systems must be limited.

The NCP1370 changes valley as the input voltage increases and as the output current set−point is varied during dimming. This limits the switching frequency excursion. Once a valley is selected, the controller stays locked in the valley until the input voltage or the output current set−point varies significantly.

The input voltage is sensed by the VIN pin. The internal logic selects the operating valley according to VIN pin voltage and DIM pin voltage.

By default, when the output current is not dimmed, the controller operates in the first valley at low line and in the second valley at high line for version A. For version B, the controller operates in the 3rd valley at high line. Table 5 summarizes the valley selected by the controller as a function of the output current and the input voltage. The numbers in blue are the selected valleys for version B.

Table 5. VALLEY SELECTION

I_{out} value at which the controller changes valley (I_{out} decreasing)	**VIN pin voltage for valley change** V_{VIN} decreases ← 0 −− LL −− 2.3 V −− HL −− 5 V		**I_{out} value at which the controller changes valley** (I_{out} increasing)
100%	1st	2nd (3rd)	100%
75%	2nd	3rd (4th)	78%
50%	4th	5th (6th)	53%
30%	7th	8th (9th)	33%
15%	11th	12th (13th)	20%
6%	13th	15th (16th)	8%
0%			0%
I_{out} decreases ↓			I_{out} increases ↑
	0 −− LL −− 2.4 V −− HL −− 5 V → V_{VIN} increases **VIN pin voltage for valley change**		

Zero Crossing Detection Block

The ZCD pin allows detecting when the drain−source voltage of the power MOSFET reaches a valley.

A valley is detected when the voltage on pin 1 crosses down the 55−mV internal threshold.

In order to decrease the capacitor value needed on ZCD pin to turn−on the MOSFET right in the valley or in some case remove it, a small delay (250 ns) is added internally before turning−on the MOSFET.

At startup or in case of extremely damped free oscillations, the ZCD comparator may not be able to detect the valleys. To avoid such a situation, the NCP1370 features a Time−Out circuit that generates pulses if the voltage on ZCD pin stays below the 55−mV threshold for 6.5 μs.

The Time−out also acts as a substitute clock for the valley detection and simulates a missing valley in case of too damped free oscillations (Figure 11).

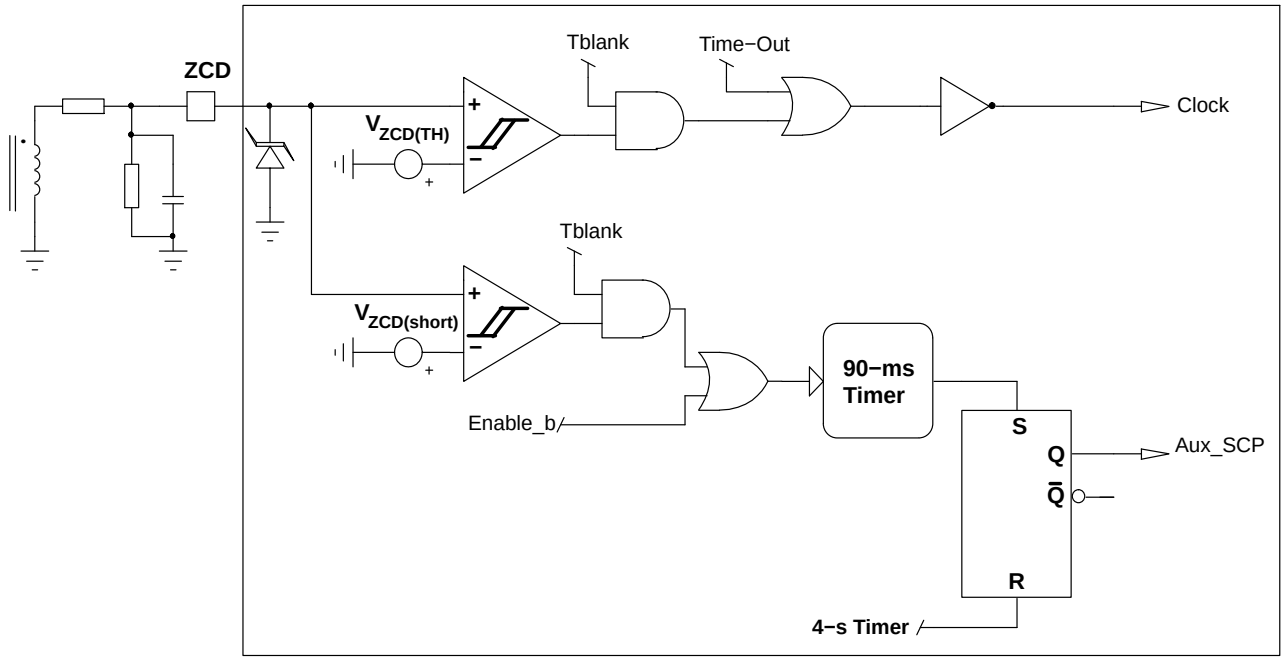


Figure 10. ZCD Block Schematic

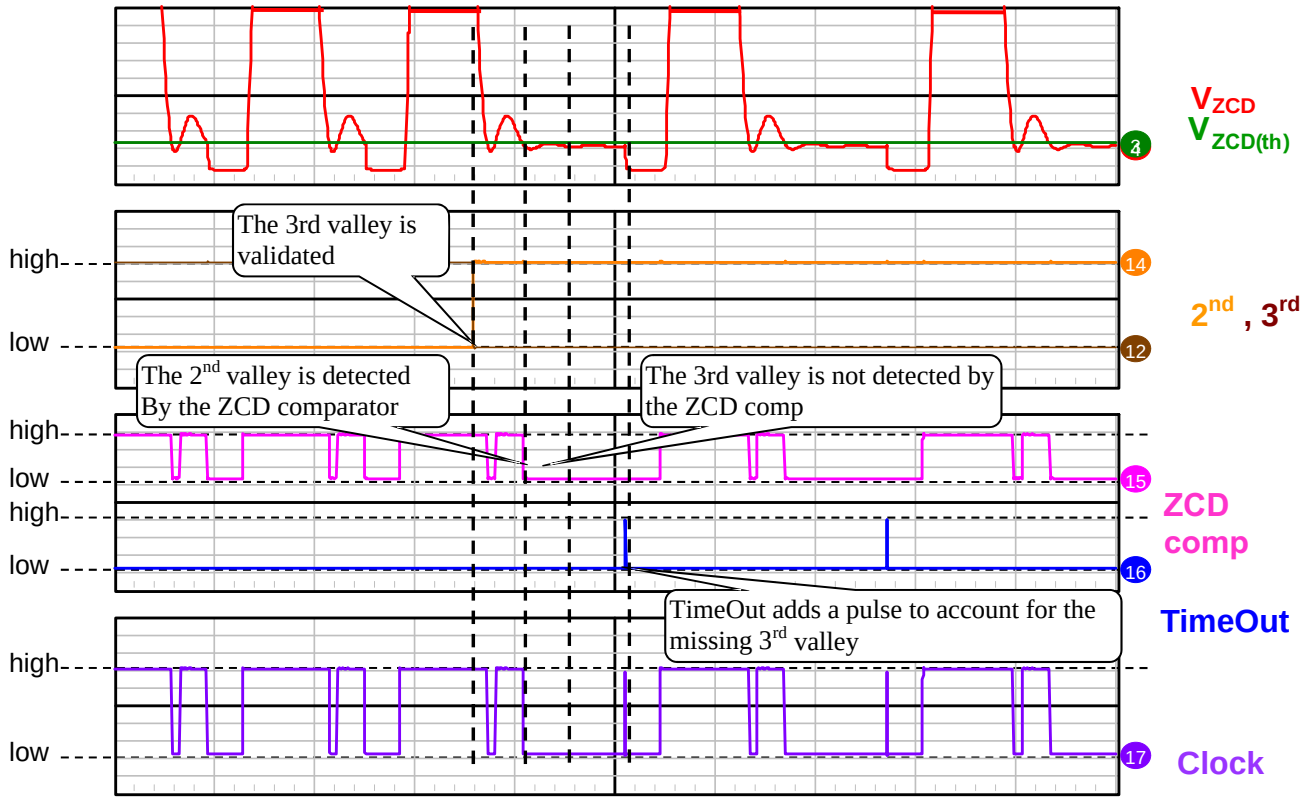


Figure 11. Time−out Chronograms

Output Short Circuit Protection

Because of the time−out function, if the ZCD pin or the auxiliary winding is shorted, the controller will continue switching leading to improper regulation of the LED current.

Moreover during an output short circuit, the controller will strive to maintain the constant current operation.

In order to avoid these scenarios, a secondary timer starts counting when the ZCD voltage is below the $V_{ZCD(short)}$ threshold (Figure 10). If this timer reaches 90 ms, the controller detects a fault and enters the auto−recovery fault mode: the controller stops pulsing and waits 4−s before going through a complete startup sequence.

This protection is disabled when $V_{DIM} < V_{DIM(EN)}$.

Line Feed−Forward

Because of the propagation delays, the MOSFET is not turned−off immediately when the current set−point is reached. As a result, the primary peak current is higher than expected and the output current increases. To compensate the peak current increase brought by the propagation delays, a positive voltage proportional to the line voltage is added on the current sense signal. The amount of offset voltage can be adjusted using the R_{CS} resistor as shown in Figure 12.

$$V_{CS(offset)} = K_{LFF} V_{pinVIN} R_{CS} \quad \text{(eq. 7)}$$

The offset voltage is applied only during the MOSFET on−time.

This offset voltage is always applied over the load range.

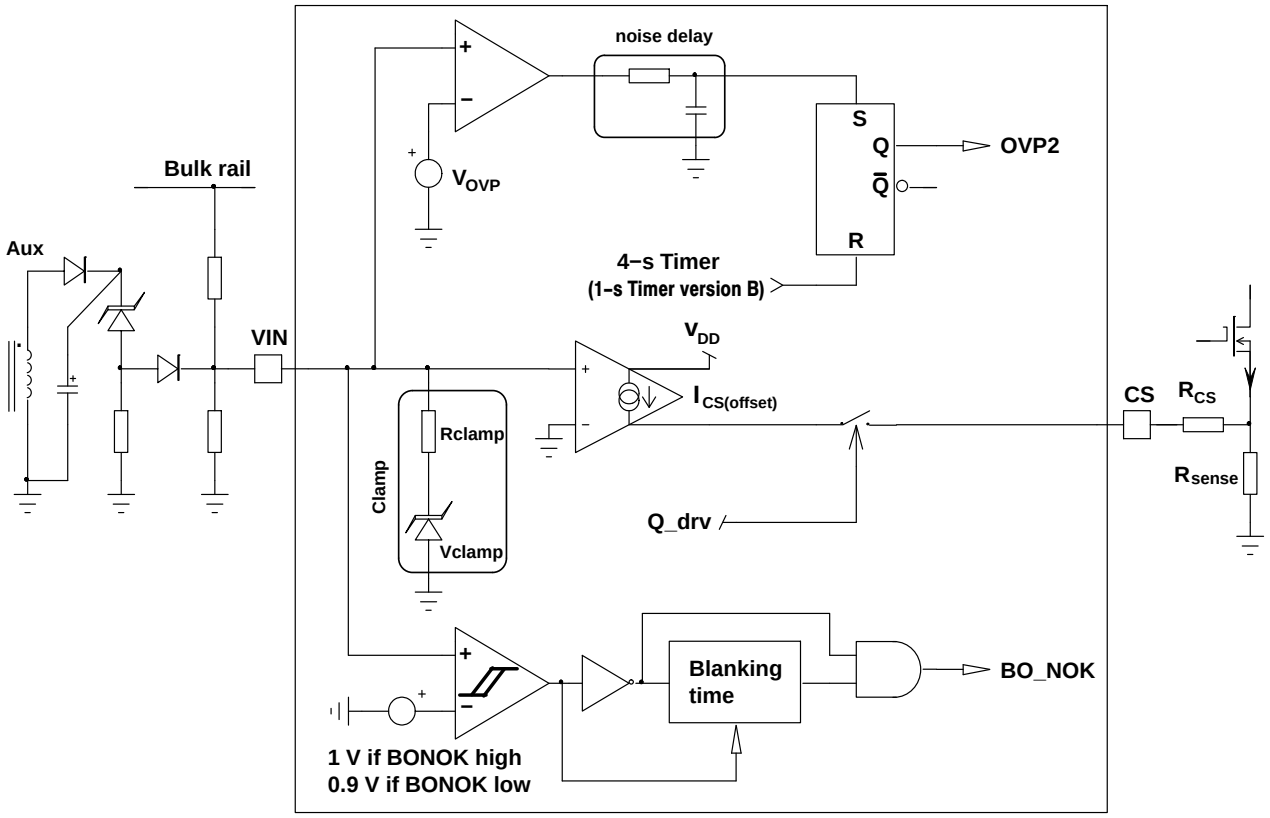


Figure 12. Line Feed−Forward, Adjustable OVP and Brown−out Schematic

Adjustable Over Voltage Protection

A clamping circuit on VIN pin limits the voltage excursion to 4.1 V (Figure 12). This level is high enough to allow good linearity of the line feedforward current for universal mains applications with an input voltage up to 265 V rms.

When the zener diode starts conducting, it injects current inside the clamping circuit and the voltage on VIN pin increases. When V_{VIN} exceeds V_{OVP} during $t_{OVP(delay)}$, the circuit detects an over voltage condition and stops the DRV pulses. The controller waits until the OVP timer ($t_{OVP(recovery)}$) has elapsed (4 s for version A, 1 s for version B) and restarts switching.

Brown−out

In order to protect the supply against a very low input voltage, the NCP1370 features a brown−out circuit with a fixed ON/OFF threshold (Figure 12). The controller is allowed to start if a voltage higher than 1 V is applied to the VIN pin and shuts−down if the VIN pin voltage decreases and stays below 0.9 V when the BO blanking timer has elapsed (BO_NOK high). When a brown−out condition is detected, the circuit stops pulsing and goes into the OFF mode detailed in the “Fault Management Section”.

Pin Connection Faults

- **CS pin Short to ground**
  The circuit senses the CS pin impedance every time it starts−up. If the measured impedance does not exceed 110 Ω typically, the circuit does not start pulsing and shutdown. The circuit attempts to restart after waiting 4 seconds. In practice, it is recommended to place a minimum of 250 Ω in series between the CS pin and the current sense resistor to take into account parasitic component effect and electrical parameters tolerance.
- **Fault of GND pin connection**
  If the GND pin is properly connected, the current drawn from the positive terminal of the V_{CC} capacitor flows out of the GND pin to return to the negative terminal of the V_{CC} capacitor. If the GND pin is not connected, the circuit ESD diodes offer another return path. The accidental non−connection of the GND pin is monitored by detecting that one of the ESD diode is conduction. Practically, the ESD diode of CS pin is monitored. If such a fault is detected for 200 μs, the circuit stops generating DRV pulses.

Fault Management and Startup Sequence

Figure 13 and Figure 14 shows the state diagrams of the NCP1370.

OFF Mode

At startup, as long as V_{CC} is not high enough, the controller is reset. Its current consumption is $I_{CC(start)}$. When $V_{CC} > V_{CC(on)}$, the controller goes in OFF mode and waits for the enable signal ($V_{DIM} > V_{DIM(EN)}$). In OFF mode, the IC consumption is very low (50 μA maximum).

The OFF mode is exited only if $V_{CC} > V_{CC(on)}$ and $V_{DIM} > V_{DIM(EN)}$. The controller then goes in FAULT mode.

More generally, the OFF mode is entered upon the following events:

- $V_{CC} < V_{CC(off)}$
- Brown−out edge
- $V_{DIM} < V_{DIM(EN)}$ after 4 seconds
- Die over temperature (TSD)
- The 4−s auto−recovery timer has elapsed

FAULT Mode

In this mode, the controller measures CS pin impedance. If CS pin is not shorted the controller is allowed to start the DRV pulses. If CS pin is shorted, the controller starts the 4 seconds timer. No DRV pulse is generated in this mode.

AR Mode

In the auto−recovery mode, the 4 seconds timer is counting, DRV is not pulsing. The 4 seconds timer starts counting when:

- $V_{DIM} < V_{DIM(EN)}$
- A short circuit on CS pin is detected
- $V_{CC} > V_{CC(OVP)}$
- An Output / Auxiliary winding Short circuit is detected: “Aux_SCP high”
- Second OCP level triggered

When the 4−s timer has elapsed, the controller goes in OFF Mode.

Adjustable OVP Management

When the adjustable OVP on VIN pin is triggered, the controller stops the DRV pulses and starts the OVP2 Timer (4 s in version A, 1 s in version B).

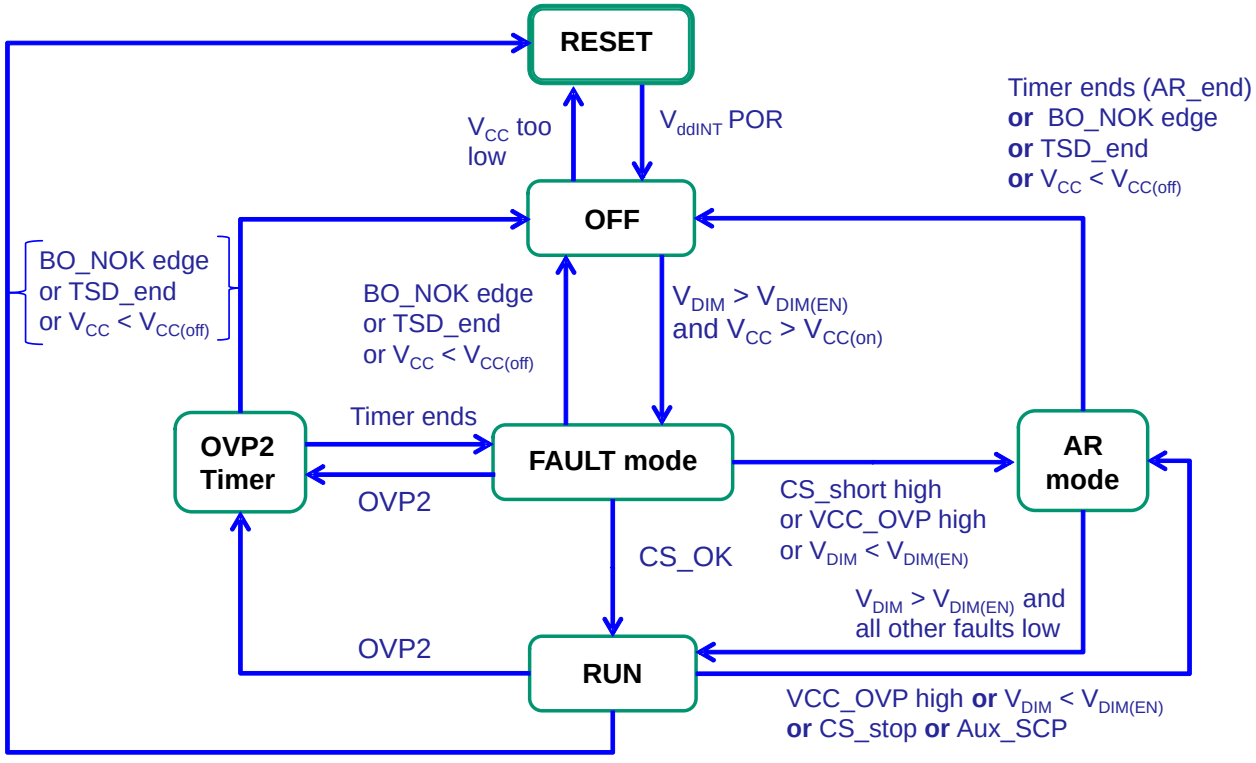
When the OVP2 timer has elapsed, the controller goes in FAULT mode and restart switching if no other fault is detected.

Latched Protection (V_{CC} OVP, Output Diode Short Circuit Protection in Version A)

When $V_{CC} > V_{CC(OVP)}$ or when the 2nd OCP is triggered, the DRV pulses stop and the controller is latched (Figure 14).

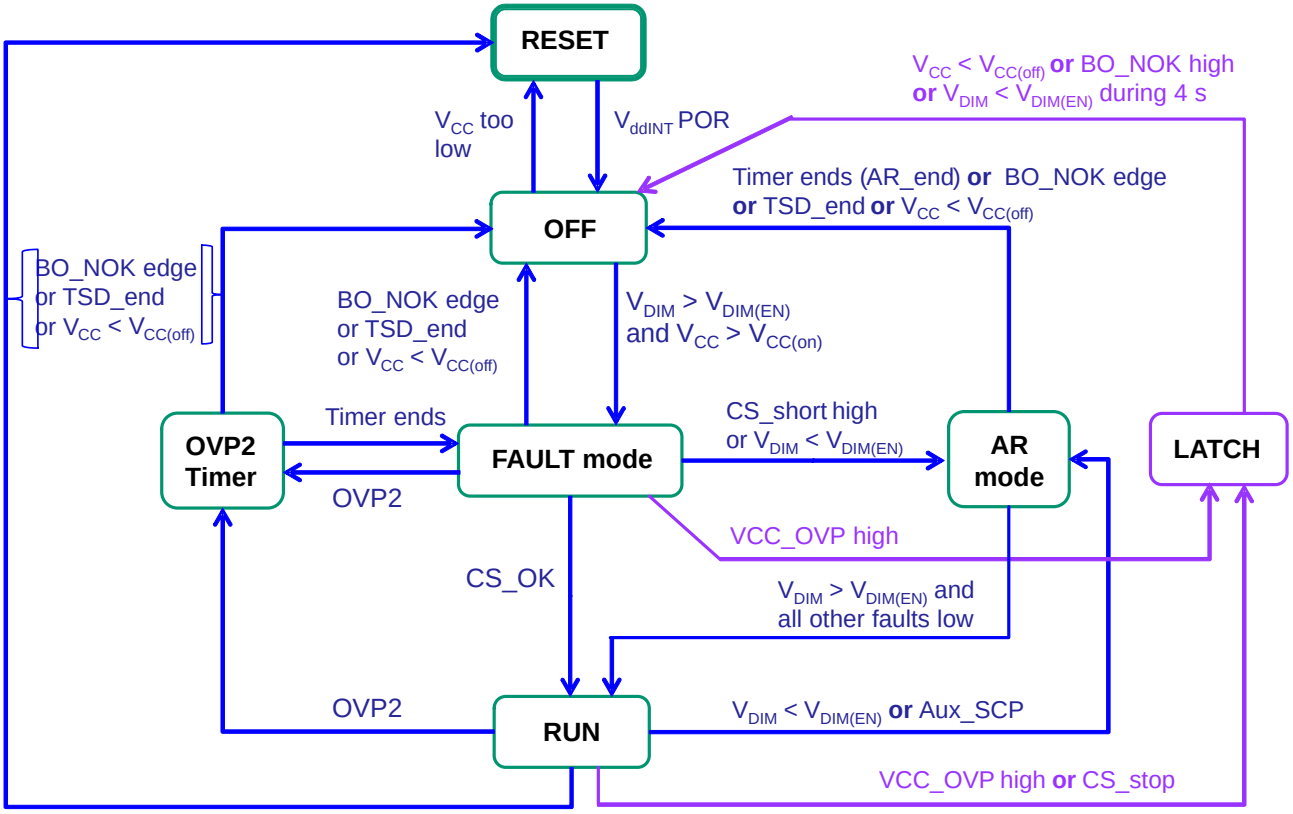
The Latch resets when one of the 3 following events occurs:

- $V_{CC} < V_{CC(off)}$
- $V_{DIM} < V_{DIM(EN)}$ during 4 seconds
- BO_NOK becomes high



With states:	RESET	→ Controller is dead
	OFF	→ Controller is in OFF Mode, $I_{CC} = I_{CC(off)}$ (50 μA max.)
	FAULT Mode	→ No switching, $I_{CC} = I_{CC1}$
	RUN	→ Controller is switching
	AR Mode	→ the 4−s auto−recovery timer is counting, No switching
	OVP2 Timer	→ The OVP2 Timer (4−s or 1−s) is counting, No DRV pulses

Figure 13. Fault State Diagram with Auto−recovery Faults



With states:	RESET	→ Controller is dead
	OFF	→ Controller is in OFF Mode, $I_{CC} = I_{CC(off)}$ (50 µA max.)
	FAULT Mode	→ No switching, $I_{CC} = I_{CC1}$
	RUN	→ Controller is switching
	AR Mode	→ the 4-s auto-recovery timer is counting, No switching
	OVP2 Timer	→ The OVP2 Timer (4-s or 1-s) is counting, No DRV pulses

Figure 14. Fault State Diagram with Latched Faults

ORDERING INFORMATION

Device	Package Type	Shipping†
NCP1370BDR2G	SOIC−8 (Pb free)	2500 / Tape & Reel

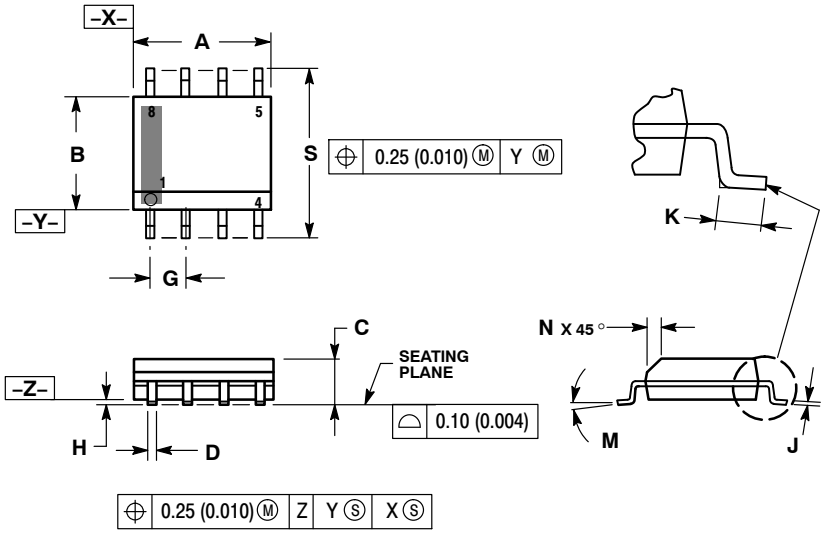
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

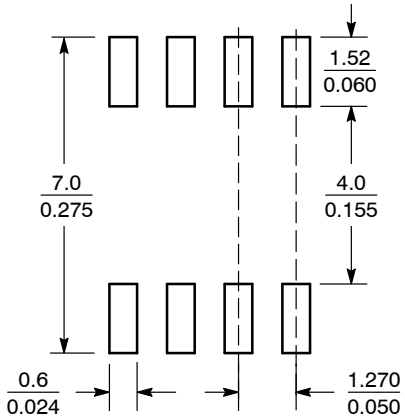
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

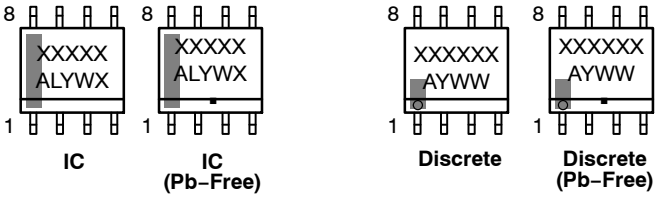
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC | IC (Pb−Free) | Discrete | Discrete (Pb−Free)

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**SOIC−8 NB**	**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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