

74LVT16374A; 74LVTH16374A

3.3 V 16-bit edge-triggered D-type flip-flop; 3-state

Rev. 12 — 6 August 2021

Product data sheet

1. General description

The 74LVT16374A; 74LVTH16374A is a 16-bit edge-triggered D-type flip-flop with 3-state outputs. The device can be used as two 8-bit flip-flops or one 16-bit flip-flop. The device features two clocks (1CP and 2CP) and two output enables (1 \overline{OE} and 2 \overline{OE}), each controlling 8-bits. The flip-flops will store the state of their individual D-inputs that meet the set-up and hold time requirements on the LOW-to-HIGH clock (nCP) transition. A HIGH on n \overline{OE} causes the outputs to assume a high-impedance OFF-state. Operation of the n \overline{OE} input does not affect the state of the flip-flops.

2. Features and benefits

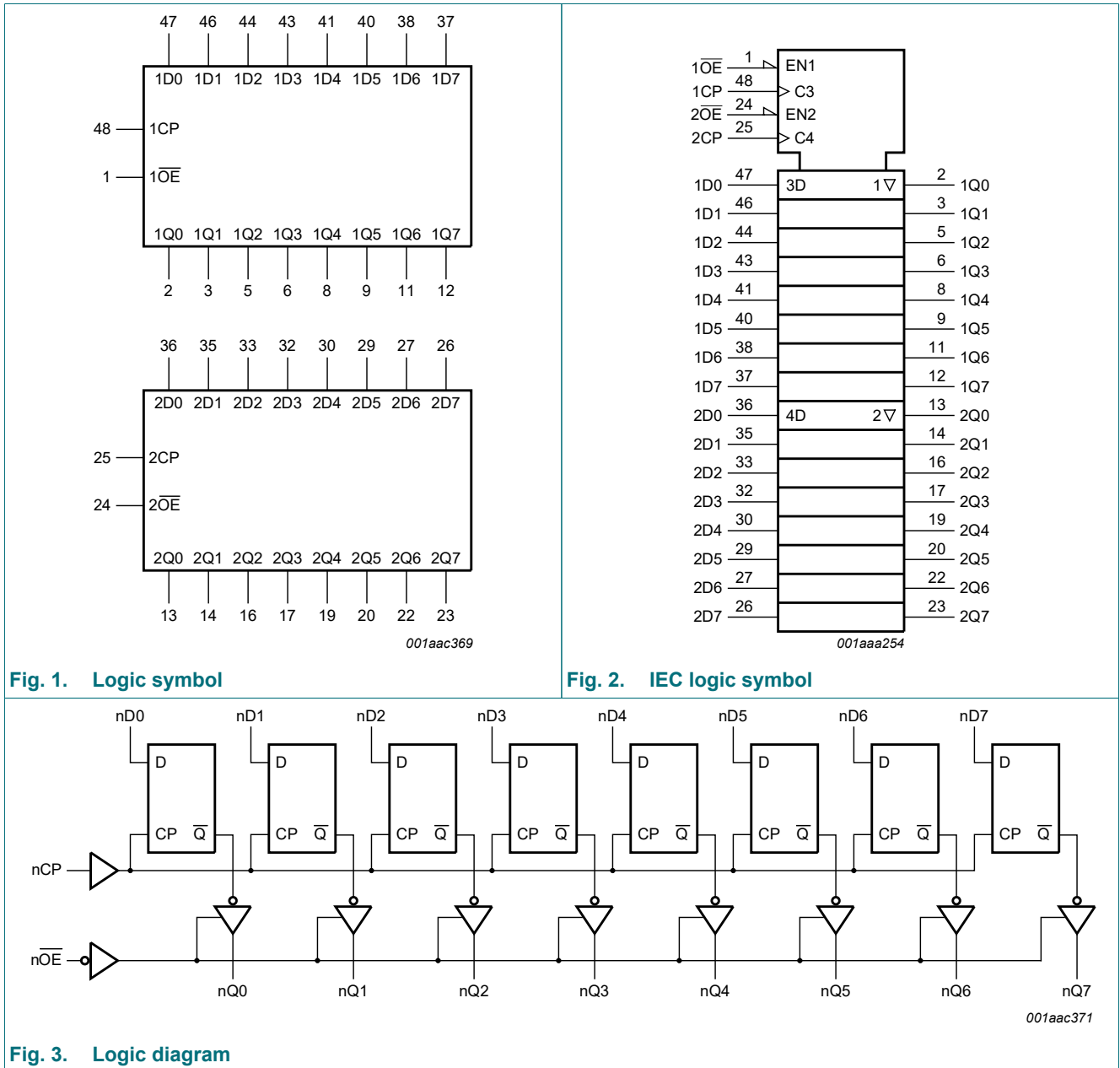
- 16-bit edge-triggered flip-flop
- 3-state buffers
- Output capability: +64 mA and -32 mA
- Wide supply voltage range from 2.7 to 3.6 V
- Overvoltage tolerant inputs to 5.5 V
- BiCMOS high speed and output drive
- Direct interface with TTL levels
- Input and output interface capability to systems at 5 V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs. (74LVTH16374A only)
- Live insertion and extraction permitted
- Power-up reset
- Power-up 3-state
- No bus current loading when output is tied to 5 V bus
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 500 mA per JESD 78 Class II Level B
- Complies with JEDEC standard JESD8C (2.7 V to 3.6 V)
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to 85 °C

3. Ordering information

Table 1. Ordering information

| Type number | Package | | | |
|-----------------|-------------------|---------|--|----------|
| | Temperature range | Name | Description | Version |
| 74LVT16374ADGG | -40 °C to +85 °C | TSSOP48 | plastic thin shrink small outline package; 48 leads; body width 6.1 mm | SOT362-1 |
| 74LVTH16374ADGG | | | | |

4. Functional diagram



5. Pinning information

5.1. Pinning

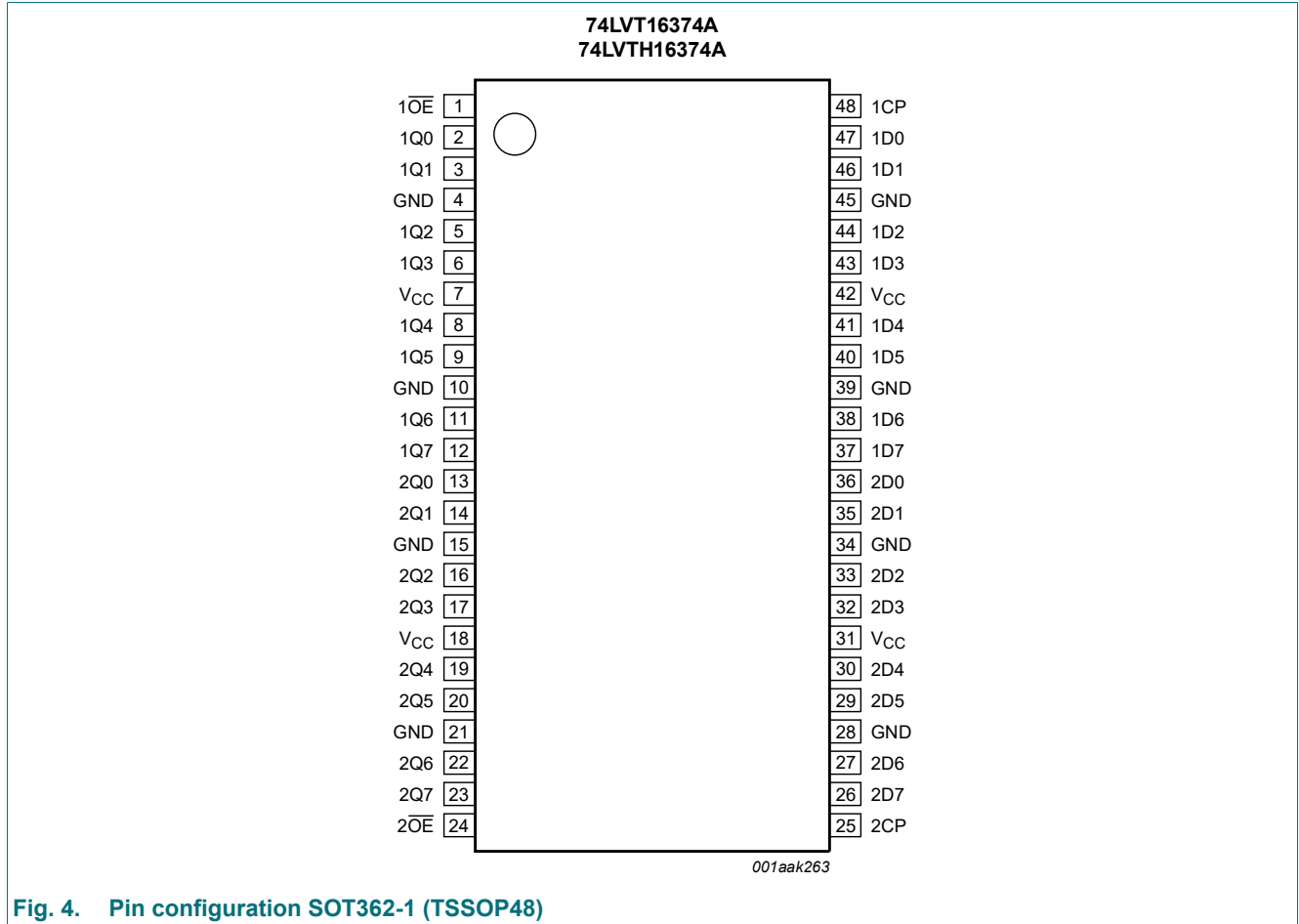


Fig. 4. Pin configuration SOT362-1 (TSSOP48)

5.2. Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|--|--------------------------------|----------------------------------|
| 1OE, 2OE | 1, 24 | output enable input (active LOW) |
| 1CP, 2CP | 48, 25 | clock input |
| 1Q0, 1Q1, 1Q2, 1Q3, 1Q4, 1Q5, 1Q6, 1Q7 | 2, 3, 5, 6, 8, 9, 11, 12 | data output |
| 2Q0, 2Q1, 2Q2, 2Q3, 2Q4, 2Q5, 2Q6, 2Q7 | 13, 14, 16, 17, 19, 20, 22, 23 | data output |
| GND | 4, 10, 15, 21, 28, 34, 39, 45 | ground (0 V) |
| V _{CC} | 7, 18, 31, 42 | supply voltage |
| 1D0, 1D1, 1D2, 1D3, 1D4, 1D5, 1D6, 1D7 | 47, 46, 44, 43, 41, 40, 38, 37 | data input |
| 2D0, 2D1, 2D2, 2D3, 2D4, 2D5, 2D6, 2D7 | 36, 35, 33, 32, 30, 29, 27, 26 | data input |

6. Functional description

Table 3. Function table

H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the HIGH-to-LOW clock transition;

L = LOW voltage level; l = LOW voltage level one set-up time prior to the HIGH-to-LOW clock transition;

NC = no change; X = don't care;

Z = high-impedance OFF-state; ↑ = LOW-to-HIGH clock transition.

| Operating mode | Input | | | Internal register | Output |
|------------------------|-------|-----|-----|-------------------|------------|
| | nOE | nCP | nDn | | nQ0 to nQ7 |
| Load and read register | L | ↑ | l | L | L |
| | L | ↑ | h | H | H |
| Hold | L | NC | X | NC | NC |
| Disable outputs | H | NC | X | NC | Z |
| | H | ↑ | nDn | nDn | Z |

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|-------------------------|---------------------------------------|------|------|------|
| V _{CC} | supply voltage | | -0.5 | +4.6 | V |
| V _I | input voltage | [1] | -0.5 | +7.0 | V |
| V _O | output voltage | output in OFF-state or HIGH-state [1] | -0.5 | +7.0 | V |
| I _{IK} | input clamping current | V _I < 0 V | -50 | - | mA |
| I _{OK} | output clamping current | V _O < 0 V | -50 | - | mA |
| I _O | output current | output in LOW-state | - | 128 | mA |
| | | output in HIGH-state | -64 | - | mA |
| T _{stg} | storage temperature | | -65 | +150 | °C |
| T _j | junction temperature | [2] | - | 150 | °C |
| P _{tot} | total power dissipation | T _{amb} = -40 °C to +85 °C | - | 500 | mW |

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

8. Recommended operating conditions

Table 5. Recommended operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|-------------------------------------|---|-----|-----|-----|--------------------|
| V_{CC} | supply voltage | | 2.7 | - | 3.6 | V |
| V_I | input voltage | | 0 | - | 5.5 | V |
| V_{IH} | HIGH-level input voltage | | 2.0 | - | - | V |
| V_{IL} | LOW-level input voltage | | - | - | 0.8 | V |
| I_{OH} | HIGH-level output current | | -32 | - | - | mA |
| I_{OL} | LOW-level output current | none | - | - | 32 | mA |
| | | current duty cycle $\leq 50\%$; $f_i \geq 1$ kHz | - | - | 64 | mA |
| T_{amb} | ambient temperature | in free-air | -40 | - | +85 | $^{\circ}\text{C}$ |
| $\Delta t/\Delta V$ | input transition rise and fall rate | outputs enabled | - | - | 10 | ns/V |

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | $T_{amb} = -40\text{ }^{\circ}\text{C to } +85\text{ }^{\circ}\text{C}$ | | | Unit |
|--------------|-----------------------------------|--|---|----------|-----------|---------------|
| | | | Min | Typ [1] | Max | |
| V_{IK} | input clamping voltage | $V_{CC} = 2.7\text{ V}$; $I_{IK} = -18\text{ mA}$ | -1.2 | -0.85 | - | V |
| V_{OH} | HIGH-level output voltage | $I_{OH} = -100\text{ }\mu\text{A}$; $V_{CC} = 2.7\text{ V to } 3.6\text{ V}$ | $V_{CC} - 0.2$ | V_{CC} | - | V |
| | | $I_{OH} = -8\text{ mA}$; $V_{CC} = 2.7\text{ V}$ | 2.4 | 2.5 | - | V |
| | | $I_{OH} = -32\text{ mA}$; $V_{CC} = 3.0\text{ V}$ | 2.0 | 2.3 | - | V |
| V_{OL} | LOW-level output voltage | $V_{CC} = 2.7\text{ V}$ | | | | |
| | | $I_{OL} = 100\text{ }\mu\text{A}$ | - | 0.07 | 0.2 | V |
| | | $I_{OL} = 24\text{ mA}$ | - | 0.3 | 0.5 | V |
| | | $V_{CC} = 3.0\text{ V}$ | | | | |
| | | $I_{OL} = 16\text{ mA}$ | - | 0.25 | 0.4 | V |
| | | $I_{OL} = 32\text{ mA}$ | - | 0.3 | 0.5 | V |
| $V_{OL(pu)}$ | power-up LOW-level output voltage | $V_{CC} = 3.6\text{ V}$; $I_O = 1\text{ mA}$; $V_I = V_{CC}$ or GND [2] | - | 0.1 | 0.55 | V |
| | | $V_{CC} = 3.6\text{ V}$; $V_I = 0\text{ V}$ | - | 0.1 | 0.55 | V |
| I_I | input leakage current | control pins | | | | |
| | | $V_{CC} = 3.6\text{ V}$; $V_I = V_{CC}$ or GND | - | 0.1 | ± 1 | μA |
| | | $V_{CC} = 0\text{ V or } 3.6\text{ V}$; $V_I = 5.5\text{ V}$ | - | 0.4 | 10 | μA |
| | | input data pins [3] | | | | |
| | | $V_{CC} = 0\text{ V or } 3.6\text{ V}$; $V_I = 5.5\text{ V}$ | - | 0.4 | 10 | μA |
| | | $V_{CC} = 3.6\text{ V}$; $V_I = V_{CC}$ | - | 0.1 | 1 | μA |
| I_{OFF} | power-off leakage current | $V_{CC} = 0\text{ V}$; V_I or $V_O = 0\text{ V to } 4.5\text{ V}$ | - | 0.1 | ± 100 | μA |
| | | $V_{CC} = 3.6\text{ V}$; $V_I = 0\text{ V}$ | - | 0.1 | ± 100 | μA |
| I_{BHL} | bus hold LOW current | $V_{CC} = 3\text{ V}$; $V_I = 0.8\text{ V}$ | 75 | 135 | - | μA |
| I_{BHH} | bus hold HIGH current | $V_{CC} = 3\text{ V}$; $V_I = 2.0\text{ V}$ | - | -135 | -75 | μA |
| I_{BHLO} | bus hold LOW overdrive current | input data pins; $V_I = 0\text{ V to } 3.6\text{ V}$; $V_{CC} = 3.6\text{ V}$ [4] | 500 | - | - | μA |

| Symbol | Parameter | Conditions | T _{amb} = -40 °C to +85 °C | | | Unit |
|-----------------------|------------------------------------|---|-------------------------------------|---------|------|------|
| | | | Min | Typ [1] | Max | |
| I _{BHHO} | bus hold HIGH overdrive current | input data pins; V _I = 0 V to 3.6 V; V _{CC} = 3.6 V [4] | - | - | -500 | μA |
| I _{LO} | output leakage current | output in HIGH-state when V _O > V _{CC} ; V _O = 5.5 V; V _{CC} = 3.0 V | - | 50 | 125 | μA |
| I _{O(pu/pd)} | power-up/power-down output current | V _{CC} ≤ 1.2 V; V _O = 0.5 V to V _{CC} ; V _I = GND or V _{CC} ; n _{OE} = don't care [5] | - | 1 | ±100 | μA |
| I _{OZ} | OFF-state output current | V _{CC} = 3.6 V; V _I = V _{IH} or V _{IL} | | | | |
| | | output HIGH: V _O = 3.0 V | - | 0.5 | 5 | μA |
| | | output LOW: V _O = 0.5 V | -5 | 0.5 | - | μA |
| I _{CC} | supply current | V _{CC} = 3.6 V; V _I = GND or V _{CC} ; I _O = 0 A | | | | |
| | | outputs HIGH | - | 0.07 | 0.12 | mA |
| | | outputs LOW | - | 4.0 | 6.0 | mA |
| | | outputs disabled [6] | - | 0.07 | 0.12 | mA |
| ΔI _{CC} | additional supply current | per input pin; V _{CC} = 3.0 V to 3.6 V; one input at V _{CC} - 0.6 V, other inputs at V _{CC} or GND [7] | - | 0.1 | 0.2 | mA |
| C _I | input capacitance | input pins; V _I = 0 V or 3.0 V | - | 3 | - | pF |
| C _O | output capacitance | output pins nQn; outputs disabled; V _O = 0 V or V _{CC} | - | 9 | - | pF |

[1] Typical values are measured at V_{CC} = 3.3 V and at T_{amb} = 25 °C.

[2] For valid test results, data must not be loaded into the flips-flops (or latches) after applying power.

[3] Unused pins at V_{CC} or GND.

[4] This is the bus hold overdrive current required to force the input to the opposite logic state.

[5] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms.

From V_{CC} = 1.2 V to V_{CC} = 3.3 V ± 0.3 V a transition time of 100 μs is permitted. This parameter is valid for T_{amb} = 25 °C only.

[6] I_{CC} is measured with outputs pulled to V_{CC} or GND.

[7] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

10. Dynamic characteristics

Table 7. Dynamic characteristics

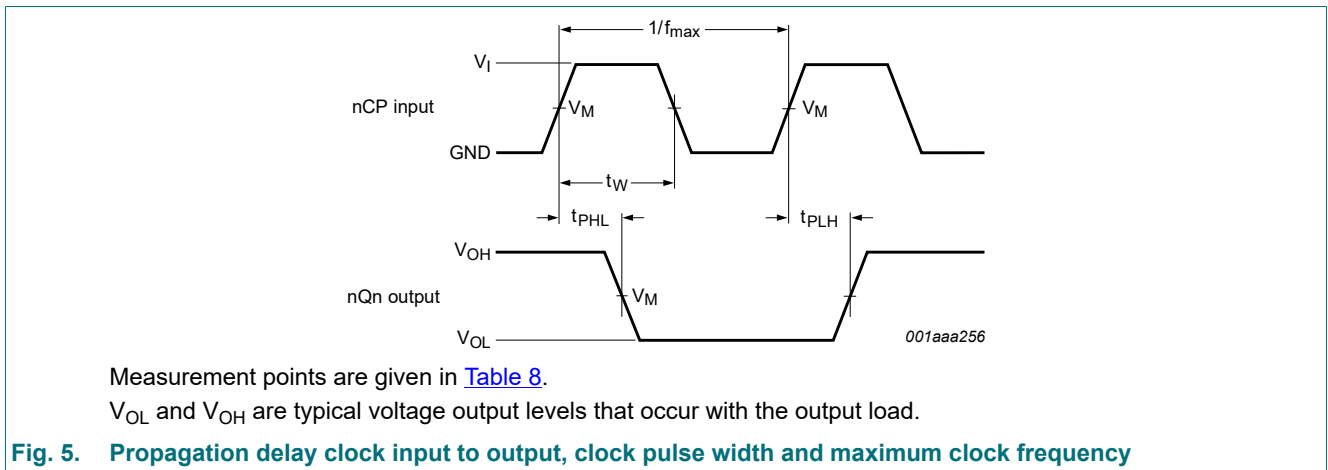
Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 8.

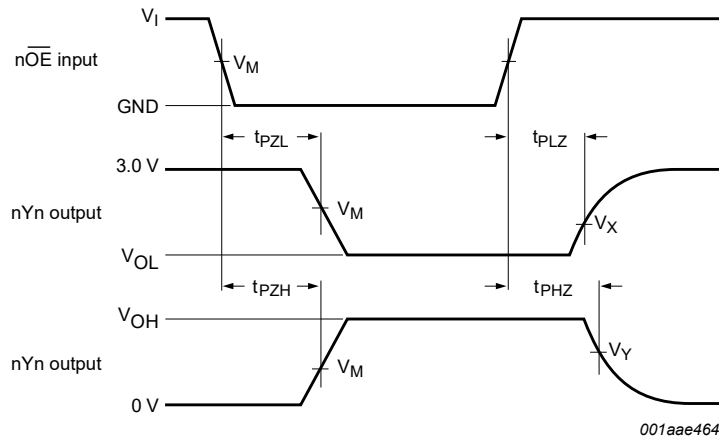
| Symbol | Parameter | Conditions | T _{amb} = -40 °C to +85 °C | | | Unit |
|------------------|-------------------------------------|--|-------------------------------------|---------|-----|------|
| | | | Min | Typ [1] | Max | |
| f _{max} | maximum frequency | nCP; V _{CC} = 3.3 V ± 0.3 V; see Fig. 5 | 150 | - | - | MHz |
| t _{PLH} | LOW to HIGH propagation delay | nCP to nQn; see Fig. 5 | | | | |
| | | V _{CC} = 3.3 V ± 0.3 V | 1.5 | 2.9 | 5.0 | ns |
| | | V _{CC} = 2.7 V | - | - | 5.6 | ns |
| t _{PHL} | HIGH to LOW propagation delay | nCP to nQn; see Fig. 5 | | | | |
| | | V _{CC} = 3.3 V ± 0.3 V | 1.5 | 3.0 | 5.0 | ns |
| | | V _{CC} = 2.7 V | - | - | 5.6 | ns |
| t _{PZH} | OFF-state to HIGH propagation delay | n _{OE} to nQn; see Fig. 6 | | | | |
| | | V _{CC} = 3.3 V ± 0.3 V | 1.5 | 3.2 | 4.8 | ns |
| | | V _{CC} = 2.7 V | - | - | 6.0 | ns |
| t _{PZL} | OFF-state to LOW propagation delay | n _{OE} to nQn; see Fig. 6 | | | | |
| | | V _{CC} = 3.3 V ± 0.3 V | 1.5 | 3.0 | 4.6 | ns |
| | | V _{CC} = 2.7 V | - | - | 5.2 | ns |

| Symbol | Parameter | Conditions | T _{amb} = -40 °C to +85 °C | | | Unit |
|------------------|-------------------------------------|--------------------------------------|-------------------------------------|---------|-----|------|
| | | | Min | Typ [1] | Max | |
| t _{PHZ} | HIGH to OFF-state propagation delay | n \overline{OE} to nQn; see Fig. 6 | | | | |
| | | V _{CC} = 3.3 V ± 0.3 V | 1.5 | 3.9 | 5.4 | ns |
| | | V _{CC} = 2.7 V | - | - | 6.0 | ns |
| t _{PLZ} | LOW to OFF-state propagation delay | n \overline{OE} to nQn; see Fig. 6 | | | | |
| | | V _{CC} = 3.3 V ± 0.3 V | 1.5 | 3.4 | 4.6 | ns |
| | | V _{CC} = 2.7 V | - | - | 5.0 | ns |
| t _{su} | set-up time | nDn to nCP; HIGH or LOW; see Fig. 7 | | | | |
| | | V _{CC} = 3.3 V ± 0.3 V | 2.0 | 0.7 | - | ns |
| | | V _{CC} = 2.7 V | 2.0 | - | - | ns |
| t _h | hold time | nDn to nCP; HIGH or LOW; see Fig. 7 | | | | |
| | | V _{CC} = 3.3 V ± 0.3 V | 0.8 | 0 | - | ns |
| | | V _{CC} = 2.7 V | 0.1 | - | - | ns |
| t _w | pulse width | nCP HIGH; see Fig. 5 | | | | |
| | | V _{CC} = 3.3 V ± 0.3 V | 1.5 | 0.6 | - | ns |
| | | V _{CC} = 2.7 V | 1.5 | - | - | ns |
| | | nCP LOW; see Fig. 5 | | | | |
| | | V _{CC} = 3.3 V ± 0.3 V | 3.0 | 1.6 | - | ns |
| | | V _{CC} = 2.7 V | 3.0 | - | - | ns |

[1] All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

10.1. Waveforms and test circuit

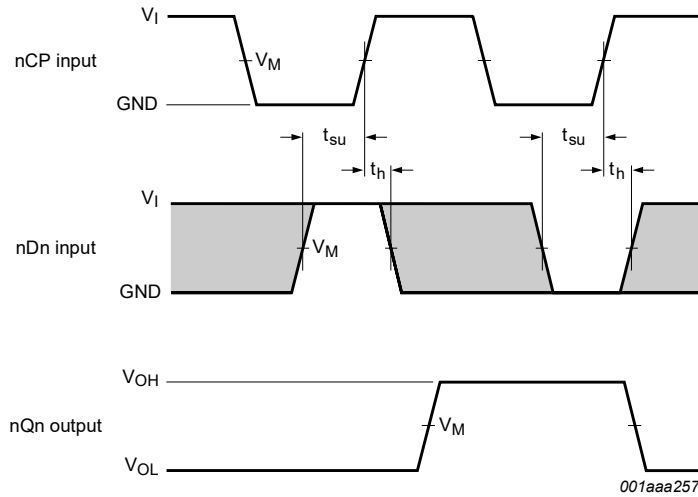




Measurements points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 6. Enable and disable times



Measurement points are given in [Table 8](#).

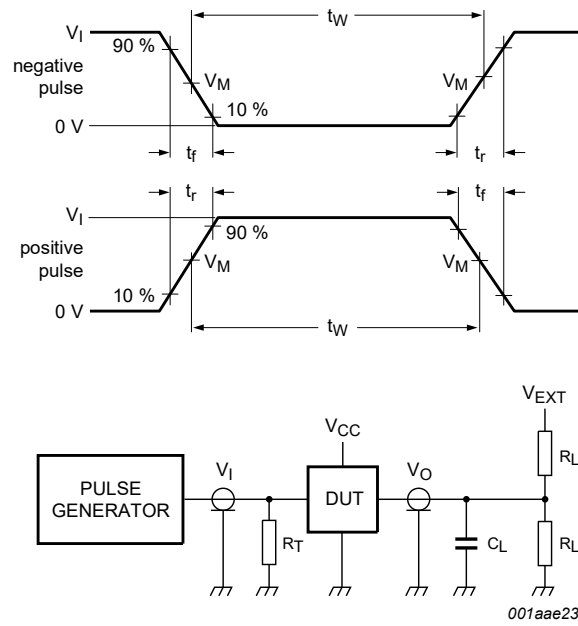
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 7. Data set-up and hold times

Table 8. Measurement points

| Input | Output | | |
|-------|--------|--------------------------|--------------------------|
| V_M | V_M | V_X | V_Y |
| 1.5 V | 1.5 V | $V_{OL} + 0.3 \text{ V}$ | $V_{OH} - 0.3 \text{ V}$ |



Test data is given in [Table 9](#).

Definitions test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = Test voltage for switching times.

Fig. 8. Test circuit for measuring switching times

Table 9. Test data

| Input | | | | Load | | V_{EXT} | | |
|-------|---------------|--------|---------------|-------|--------------|--------------------|--------------------|--------------------|
| V_I | f_i | t_w | t_r, t_f | C_L | R_L | t_{PHZ}, t_{PZH} | t_{PLZ}, t_{PZL} | t_{PLH}, t_{PHL} |
| 2.7 V | ≤ 10 MHz | 500 ns | ≤ 2.5 ns | 50 pF | 500 Ω | GND | 6 V | open |

11. Package outline

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1

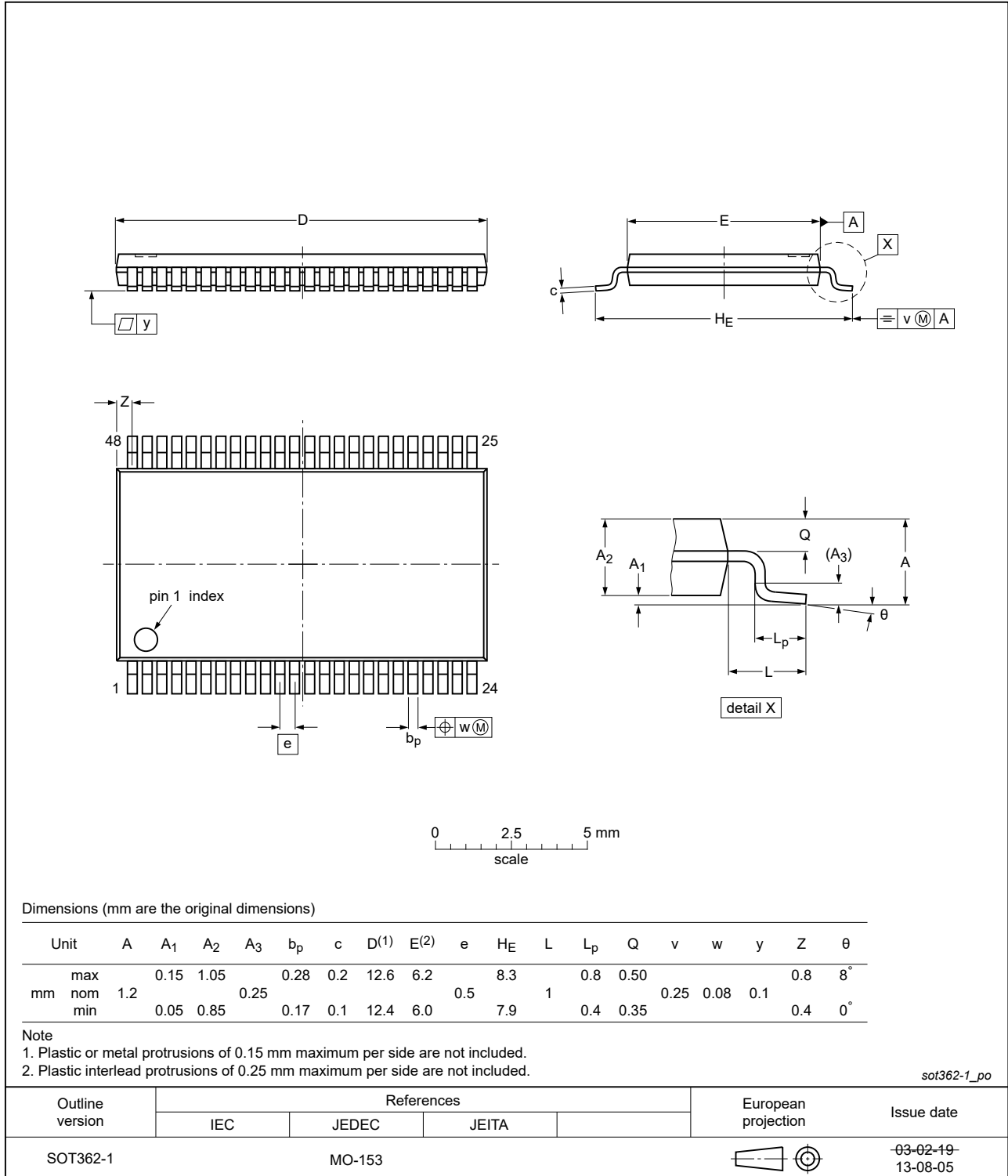


Fig. 9. Package outline SOT362-1 (TSSOP48)

12. Abbreviations

Table 10. Abbreviations

| Acronym | Description |
|---------|---|
| BiCMOS | Bipolar Complementary Metal Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

13. Revision history

Table 11. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|-----------------------|---|-----------------------|---------------|-----------------------|
| 74LVT_LVTH16374A v.12 | 20210806 | Product data sheet | - | 74LVT_LVTH16374A v.11 |
| Modifications: | <ul style="list-style-type: none"> Type number 74LVT16374ADL (SOT370-1/SSOP48) removed. Section 1 and Section 2 updated. Section 7: Derating value for P_{tot} total power dissipation removed. | | | |
| 74LVT_LVTH16374A v.11 | 20190205 | Product data sheet | - | 74LVT_LVTH16374A v.10 |
| Modifications: | <ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Type numbers 74LVT16374AEV (SOT702-1) and 74LVTH16374ABX (SOT1134-2) removed. Package outline drawing SOT362-1 (TSSOP48) updated. | | | |
| 74LVT_LVTH16374A v.10 | 20120402 | Product data sheet | - | 74LVT_LVTH16374A v.9 |
| Modifications: | <ul style="list-style-type: none"> For type number 74LVTH16374ABX the sot code has changed to SOT1134-2. | | | |
| 74LVT_LVTH16374A v.9 | 20111122 | Product data sheet | - | 74LVT_LVTH16374A v.8 |
| Modifications: | <ul style="list-style-type: none"> Legal pages updated. | | | |
| 74LVT_LVTH16374A v.8 | 20110620 | Product data sheet | - | 74LVT_LVTH16374A v.7 |
| 74LVT_LVTH16374A v.7 | 20100322 | Product data sheet | - | 74LVT_LVTH16374A v.6 |
| 74LVT_LVTH16374A v.6 | 20100118 | product data sheet | - | 74LVT16374A v.5 |
| 74LVT16374A v.5 | 20040916 | product data sheet | - | 74LVT16374A v.4 |
| 74LVT16374A v.4 | 20021101 | product specification | - | 74LVT16374A v.3 |
| 74LVT16374A v.3 | 19991018 | product specification | - | 74LVT16374A v.2 |
| 74LVT16374A v.2 | 19980219 | product specification | - | - |

3.3 V 16-bit edge-triggered D-type flip-flop; 3-state

14. Legal information

Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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