Rochester Electronics

Datasheet

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)

- Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

HARRIS SEMICONDUCTOR

HI-546, HI-547, HI-548, HI-549

Single 16 and 8, Differential 8-Channel and 4-Channel CMOS Analog MUXs with Active Overvoltage Protection

August 1997

Features

- Analog Overvoltage Protection ..... $70V_{P-P}$
- No Channel Interaction During Overvoltage
- Guaranteed r_{ON} Matching
- 44V Maximum Power Supply
- Break-Before-Make Switching
- Analog Signal Range..... ±15V
- Access Time (Typical)..... 500ns
- Standby Power (Typical).....7.5mW

Applications

- Data Acquisition
- Industrial Controls
- Telemetry

Description

The HI-546, HI-547, HI-548 and HI-549 are analog multiplexers with active overvoltage protection and guaranteed r_{ON} matching. Analog input levels may greatly exceed either power supply without damaging the device or disturbing the signal path of other channels. Active protection circuitry assures that signal fidelity is maintained even under fault conditions that would destroy other multiplexers.

Analog inputs can withstand constant $70V_{P-P}$ levels with ±15V supplies. Digital inputs will also sustain continuous faults up to 4V greater than either supply. In addition, signal sources are protected from short circuiting should multiplexer supply loss occur. Each input presents 1kΩ of resistance under this condition. These features make the HI-546, HI-547, HI-548 and HI-549 ideal for use in systems where the analog inputs originate from external equipment or separately powered circuitry. All devices are fabricated with 44V Dielectrically Isolated CMOS technology. The HI-546 is a single 16-Channel, the HI-547 is an 8-Channel differential, the HI-548 is a single 8-Channel and the HI-549 is a 4-Channel differential device. If input overvoltage protection is not needed the HI-506/507/508/509 multiplexers are recommended. For further information see Application Notes AN520 and AN521. The HI-546 and HI-547 devices are available in a 28 lead Plastic or Ceramic DIP and a 28 pad Ceramic LCC package. The HI-548/549 devices are available in a 16 lead Plastic or Ceramic DIP and a 20 pad Ceramic LCC package.

The HI-546, HI-547, HI-548 and HI-549 are offered in industrial/commercial and military grades. Additional Hi-Rel screening including 160 hour Burn-In is specified by the "-8" suffix. For MIL-STD-883 compliant parts, request the HI-546/883, HI-547/883, HI-548/883 and HI-549/883 datasheets.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI1-0546-4	-25 to 85	28 Ld CERDIP	F28.6
HI1-0546-5	0 to 75	28 Ld CERDIP	F28.6
HI1-0546-2	-55 to 125	28 Ld CERDIP	F28.6
HI1-0546/883	-55 to 125	28 Ld CERDIP	F28.6
HI3-0546-5	0 to 75	28 Ld PDIP	E28.6
HI3-0546-9	-40 to 85	28 Ld PDIP	E28.6
HI4-0546/883	-55 to 125	28 Ld CLCC	J28.A
HI4P0546-5	0 to 75	28 Ld PLCC	N28.45
HI9P0546-5	0 to 75	28 Ld SOIC	M28.3
HI9P0546-9	-40 to 85	28 Ld SOIC	M28.3
HI1-0547-2	-55 to 125	28 Ld CERDIP	F28.6
HI1-0547-4	-25 to 85	28 Ld CERDIP	F28.6
HI1-0547-5	0 to 75	28 Ld CERDIP	F28.6
HI1-0547/883	-55 to 125	28 Ld CERDIP	F28.6
HI3-0547-5	0 to 75	28 Ld PDIP	E28.6
HI4-0547/883	-55 to 125	28 Ld CLCC	J28.A
HI4P0547-5	0 to 75	28 Ld PLCC	N28.45
HI9P0547-5	0to 75	28 Ld SOIC	M28.3
HI9P0547-9	-40 to 85	28 Ld SOIC	M28.3

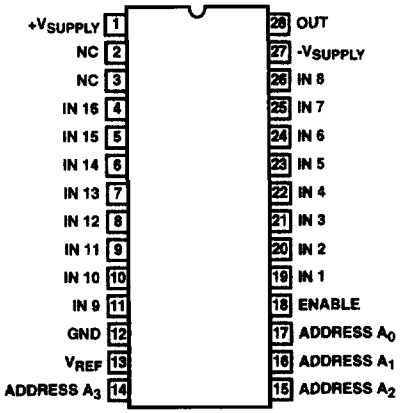
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI1-0548-2	-55 to 125	16 Ld CERDIP	F16.3
HI1-0548-4	-25 to 85	16 Ld CERDIP	F16.3
HI1-0548-5	0 to 75	16 Ld CERDIP	F16.3
HI1-0548/883	-55 to 125	16 Ld CERDIP	F16.3
HI3-0548-5	0 to 75	16 Ld PDIP	E16.3
HI4-0548/883	-55 to 125	20 Ld CLCC	J20.A
HI4P0548-5	0 to 75	20 Ld PLCC	N20.35
HI9P0548-5	0 to 75	16 Ld SOIC	M16.15
HI9P0548-9	-40 to 85	16 Ld SOIC	M16.15
HI1-0549-2	-55 to 125	16 Ld CERDIP	F16.3
HI1-0549-4	-25 to 85	16 Ld CERDIP	F16.3
HI1-0549-5	0 to 75	16 Ld CERDIP	F16.3
HI1-0549/883	-55 to 125	16 Ld CERDIP	F16.3
HI3-0549-5	0 to 75	16 Ld PDIP	E16.3
HI3-0549-9	-40 to 85	16 Ld PDIP	E16.3
HI4-0549/883	-55 to 125	20 Ld CLCC	J20.A
HI4P0549-5	0 to 75	20 Ld PLCC	N20.35
HI9P0549-5	0 to 75	16 Ld SOIC	M16.15
HI9P0549-9	-40 to 85	16 Ld SOIC	M16.15

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

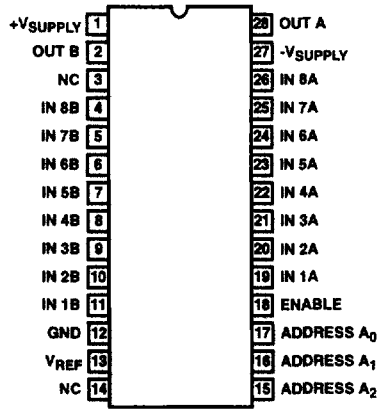
File Number **3150.1**

Pinouts

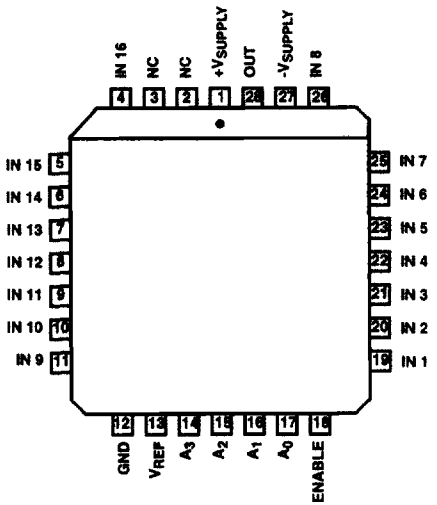
HI1-0546 (CERDIP), HI3-0546 (PDIP), HI9P0546 (SOIC)
TOP VIEW



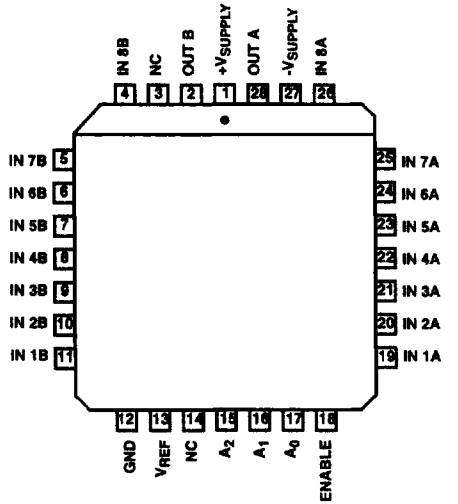
HI1-0547 (CERDIP), HI3-0547 (PDIP), HI9P0547 (SOIC)
TOP VIEW



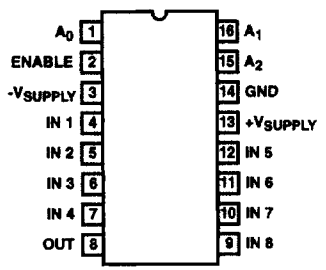
H14-0546 (CLCC)
HI4P0546 (PLCC)
TOP VIEW



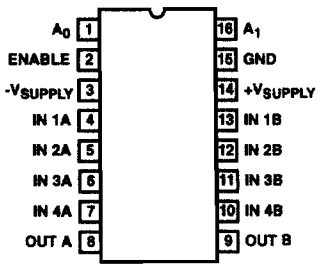
H14-0547 (CLCC)
HI4P0547 (PLCC)
TOP VIEW



HI1-0548 (CERDIP), HI3-0548 (PDIP), HI9P0548 (SOIC)
TOP VIEW

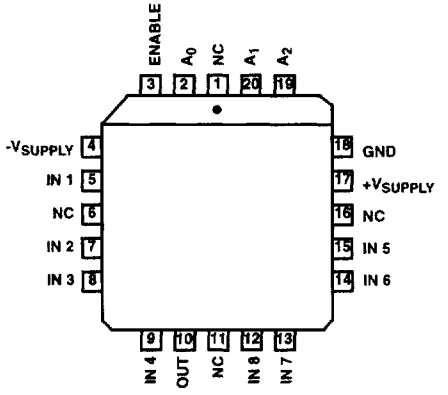


HI1-0549 (CERDIP), HI3-0549 (PDIP), HI9P0549 (SOIC)
TOP VIEW

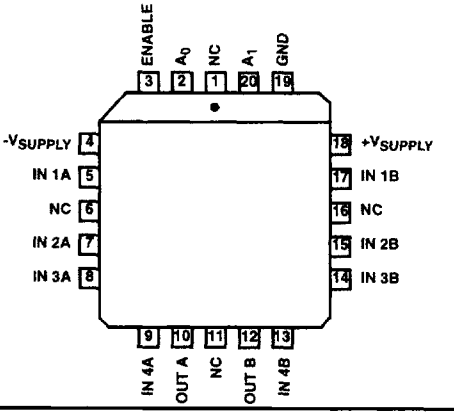


Pinouts (Continued)

HI14-0548 (CLCC)
HI4P0548 (PLCC)
TOP VIEW

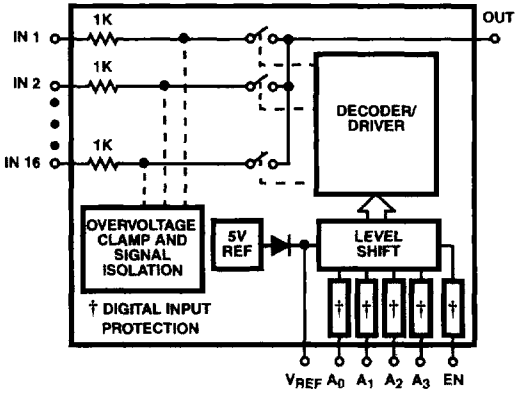


HI4-0549 (CLCC)
HI4P0549 (PLCC)
TOP VIEW

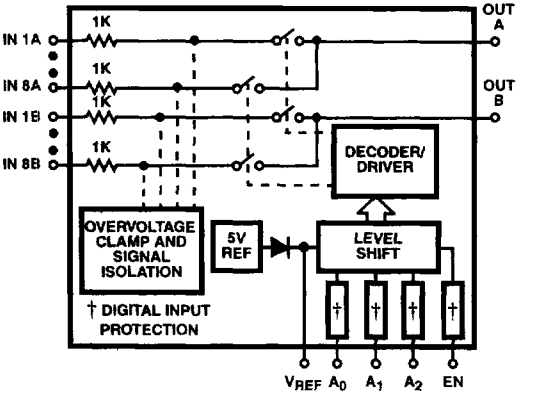


Functional Diagrams

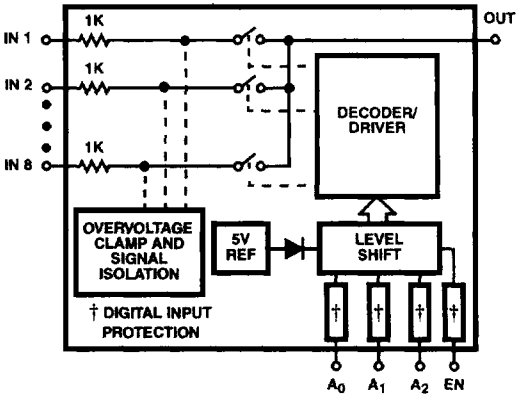
HI-546



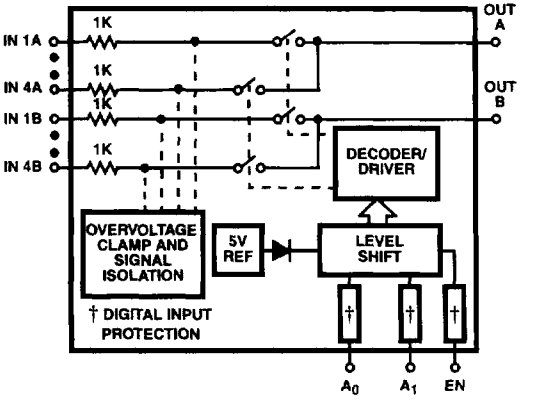
HI-547



HI-548

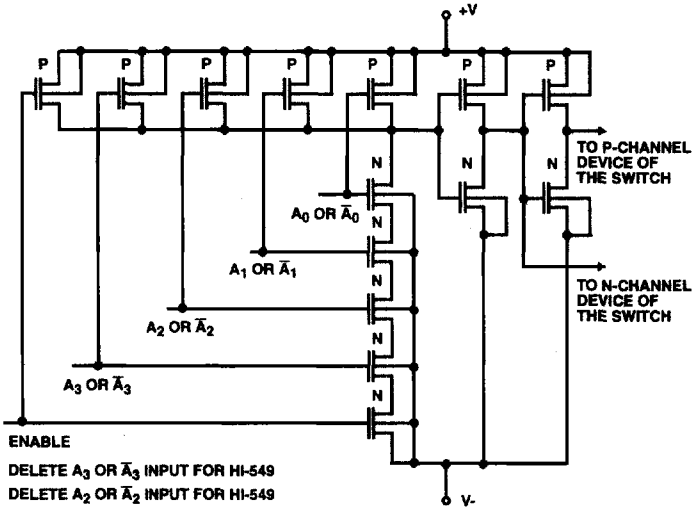


HI-549

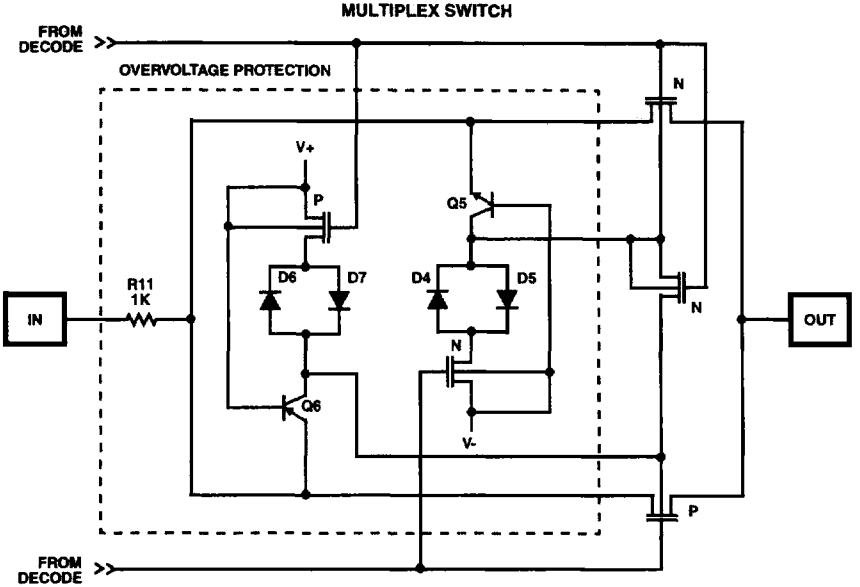


Schematic Diagrams

ADDRESS DECODER

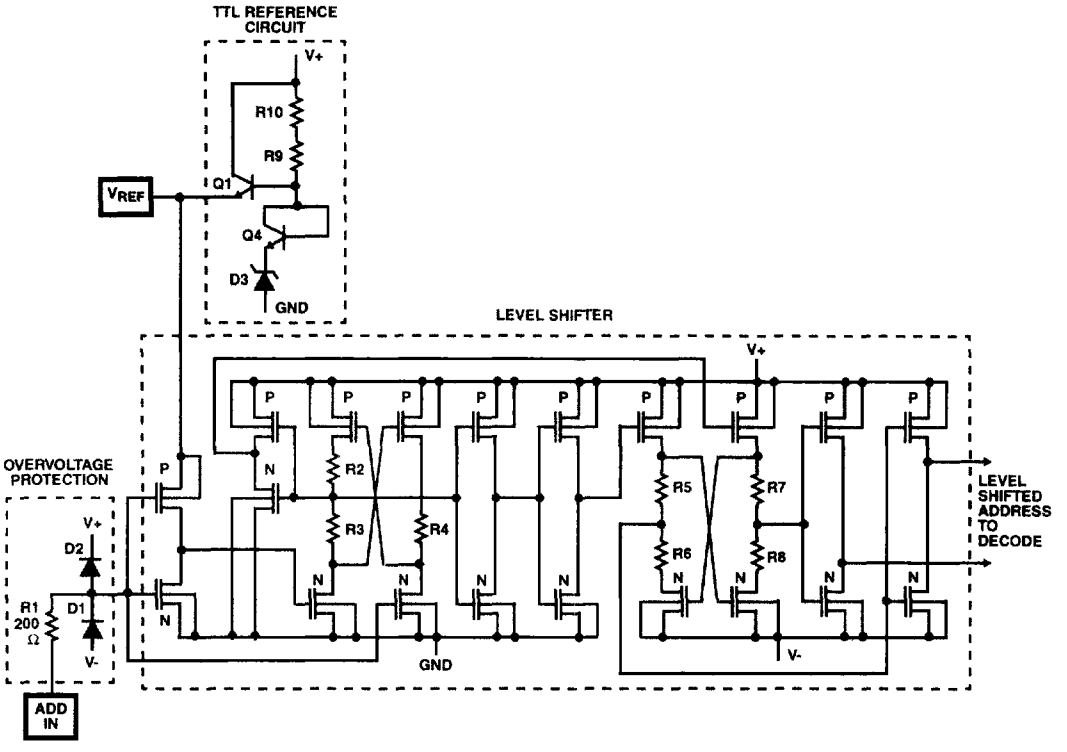


MULTIPLEX SWITCH



Schematic Diagrams (Continued)

ADDRESS INPUT BUFFER AND LEVEL SHIFTER



Absolute Maximum Ratings

$V_{SUPPLY(+)}$ to $V_{SUPPLY(-)}$ ..... +44V
$V_{SUPPLY(+)}$ to GND ..... +22V
$V_{SUPPLY(-)}$ to GND ..... -25V
Digital Input Overvoltage
$+V_{EN}$, $+V_A$ ..... $+V_{SUPPLY}$ +4V
$-V_{EN}$, $-V_A$ ..... $-V_{SUPPLY}$ -4V
or 20mA, Whichever Occurs First
Analog Signal Overvoltage (Note 6)
$+V_S$ ..... $+V_{SUPPLY}$ +20V
$-V_S$ ..... $-V_{SUPPLY}$ -20V
Continuous Current, S or D 20mA
Peak Current, S or D 40mA
(Pulsed at 1ms, 10% Duty Cycle Max)

Operating Conditions

Operating Temperature Ranges
HI-546/547/548/549-2 ..... -55°C to 125°C
HI-546/547/548/549-4 ..... -25°C to 85°C
HI-546/547/548/549-5 ..... 0°C to 75°C
HI-546/547/548/549-9 ..... -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
16 Ld CERDIP Package	85	32
28 Ld CERDIP Package	55	18
20 Ld CLCC Package	80	28
28 Ld CLCC Package	70	20
28 Ld PDIP Package	60	N/A
16 Ld PDIP Package	100	N/A
28 Ld PLCC Package	70	N/A
20 Ld PLCC Package	80	N/A
28 Ld SOIC Package	70	N/A
16 Ld SOIC Package	100	N/A

Maximum Junction Temperature
Ceramic Package ..... 175°C
Plastic Package ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(PLCC, SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Supplies = +15V, -15V; V_{REF} Pin = Open; V_{AH} (Logic Level High) = +4V; V_{AL} (Logic Level Low) = +0.8V; Unless Otherwise Specified. For Test Conditions, Consult Performance Curves

PARAMETER	TEST CONDITIONS	TEMP (°C)	HI-54X-2			HI-54X-4, -5, -9			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
SWITCHING CHARACTERISTICS									
Access Time, t_A		25	-	0.5	-	-	0.5	-	µs
		Full	-	-	1.0	-	-	1.0	µs
Break-Before Make Delay, t_{OPEN}		25	25	80	-	25	80	-	ns
Enable Delay (ON), $t_{ON(EN)}$		25	-	300	500	-	300	-	ns
		Full	-	-	1000	-	-	1000	ns
Enable Delay (OFF), $t_{OFF(EN)}$		25	-	300	500	-	300	-	ns
		Full	-	-	1000	-	-	1000	ns
Settling Time (0.1%)		25	-	1.2	-	-	1.2	-	µs
(0.01%)		25	-	3.5	-	-	3.5	-	µs
"Off Isolation"	Note 5	25	50	68	-	50	68	-	dB
Channel Input Capacitance, $C_{S(OFF)}$		25	-	5	-	-	5	-	pF
Channel Output Capacitance $C_{D(OFF)}$									
HI-546		25	-	52	-	-	52	-	pF
HI-547		25	-	30	-	-	30	-	pF
HI-548		25	-	25	-	-	25	-	pF
HI-549		25	-	12	-	-	12	-	pF
Input to Output Capacitance, $C_{DS(OFF)}$		25	-	0.1	-	-	0.1	-	pF
DIGITAL INPUT CHARACTERISTICS									
Input Low Threshold, TTL Drive, V_{AL}		Full	-	-	0.8	-	-	0.8	V

Electrical Specifications Supplies = +15V, -15V; V_{REF} Pin = Open; V_{AH} (Logic Level High) = +4V; V_{AL} (Logic Level Low) = +0.8V; Unless Otherwise Specified. For Test Conditions, Consult Performance Curves **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	HI-54X-2			HI-54X-4, -5, -9			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input High Threshold, V_{AH}	Note 7	Full	4.0	-	-	4.0	-	-	V
MOS Drive (HI-546/547 Only), V_{AL}	Note 8	25	-	-	0.8	-	-	0.8	V
MOS Drive (HI-546/547 Only), V_{AH}	Note 8	25	6.0	-	-	6.0	-	-	V
Input Leakage Current (High or Low), I_A	Note 4	Full	-	-	1.0	-	-	1.0	µA
ANALOG CHANNEL CHARACTERISTICS									
Analog Signal Range, V_S		Full	-15	-	+15	-15	-	+15	V
On Resistance, r_{ON}	Note 1	25	-	1.2	1.5	-	1.5	1.8	kΩ
		Full	-	1.5	1.8	-	1.8	2.0	kΩ
Δr_{ON}, (Any Two Channels)		25	-	-	7.0	-	-	7.0	%
Off Input Leakage Current, $I_{S(OFF)}$	Note 2	25	-	0.03	-	-	0.03	-	nA
		Full	-	-	50	-	-	50	nA
Off Output Leakage Current, $I_{D(OFF)}$	Note 2	25	-	0.1	-	-	0.1	-	nA
HI-546		Full	-	-	300	-	-	300	nA
HI-547		Full	-	-	200	-	-	200	nA
HI-548		Full	-	-	200	-	-	200	nA
HI-549		Full	-	-	100	-	-	100	nA
With Input Overvoltage Applied, $I_{D(OFF)}$	Note 3	25	-	4.0	-	-	4.0	-	nA
		Full	-	-	2.0	-	-	-	µA
On Channel Leakage Current, $I_{D(ON)}$	Note 2	25	-	0.1	-	-	0.1	-	nA
HI-546		Full	-	-	300	-	-	300	nA
HI-547		Full	-	-	200	-	-	200	nA
HI-548		Full	-	-	200	-	-	200	nA
HI-549		Full	-	-	100	-	-	100	nA
Differential Off Output Leakage Current (HI-547, HI-549 Only), I_{DIFF}		Full	-	-	50	-	-	50	nA
POWER REQUIREMENTS									
Power Dissipation, P_D		Full	-	7.5	-	-	7.5	-	mW
Current, I+	Note 6	Full	-	0.5	2.0	-	0.5	2.0	mA
Current, I-	Note 6	Full	-	0.02	1.0	-	0.02	1.0	mA

NOTES:

1. $V_{OUT} = \pm 10V$, $I_{OUT} = \mp 100\mu A$.
2. 10nA is the practical lower limit for high speed measurement in the production test environments.
3. Analog Overvoltage = ±33V.
4. Digital input leakage is primarily due to the clamp diodes (see Schematic). Typical leakage is less than 1nA at 25°C.
5. $V_{EN} = 0.8V$, $R_L = 1K$, $C_L = 15pF$, $V_S = 7V_{RMS}$, f = 100kHz.
6. V_{EN}, $V_A = 0V$ or 4V.
7. To drive from DTL/TTLCircuits, 1kΩ pull-up resistors to $+5V_{SUPPLY}$ are recommended.
8. $V_{REF} = +10V$.

Typical Performance Curves $T_A = 25^oC$, $V_{SUPPLY} = \pm15V$, $V_{AH} = +4V$, $V_{AL} = 0.8V$, V_{REF} = Open, Unless Otherwise Specified

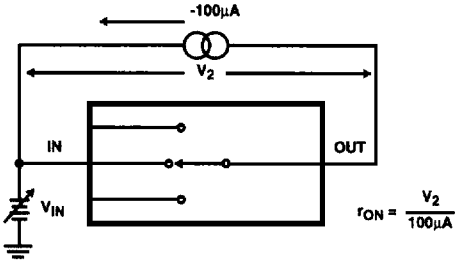


FIGURE 1A. ON RESISTANCE TEST CIRCUIT

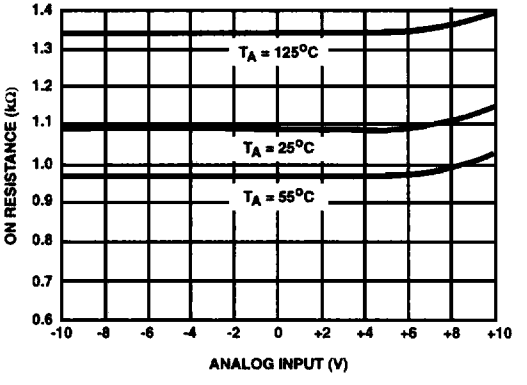


FIGURE 1B. ON RESISTANCE vs ANALOG INPUT VOLTAGE

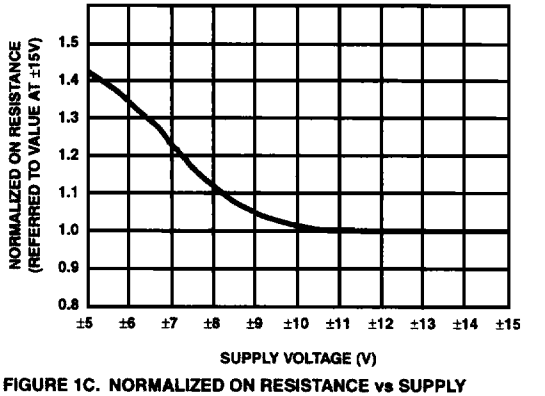


FIGURE 1C. NORMALIZED ON RESISTANCE vs SUPPLY VOLTAGE

FIGURE 1. ON RESISTANCE

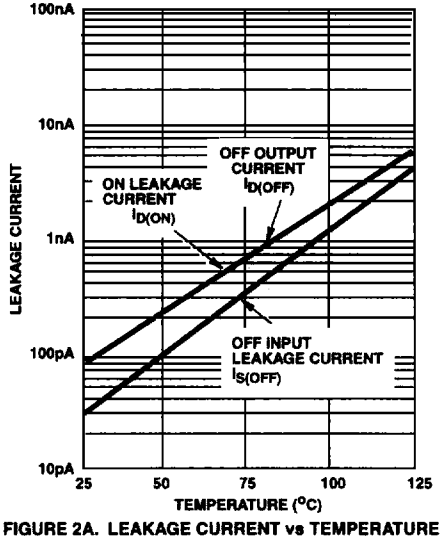


FIGURE 2A. LEAKAGE CURRENT vs TEMPERATURE

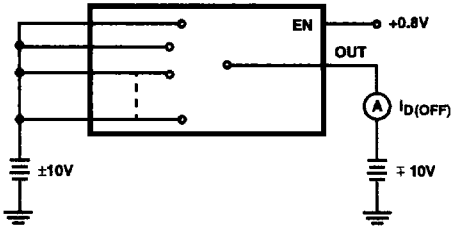


FIGURE 2B. $I_{D(OFF)}$ TEST CIRCUIT

Typical Performance Curves $T_A = 25^oC$, $V_{SUPPLY} = \pm15V$, $V_{AH} = +4V$, $V_{AL} = 0.8V$, V_{REF} = Open, Unless Otherwise Specified (Continued)

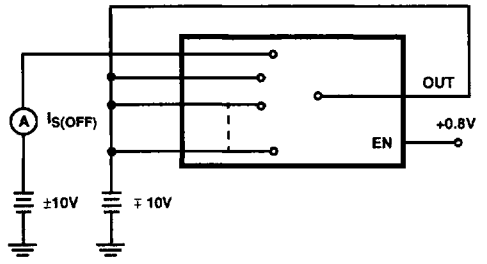


FIGURE 2C. $I_{S(OFF)}$ TEST CIRCUIT

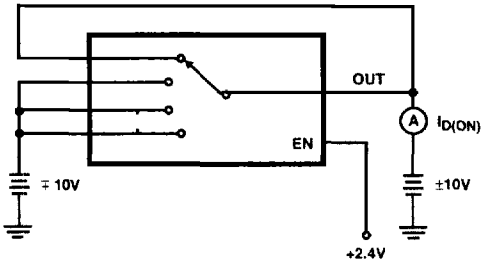


FIGURE 2D. $I_{D(ON)}$ TEST CIRCUIT

NOTE:

1. Two measurements per channel: +10V/-10V and -10V/+10V. (Two measurements per device for $I_{D(OFF)}$: +10V/-10V and -10V/+10V.)

FIGURE 2. LEAKAGE CURRENT

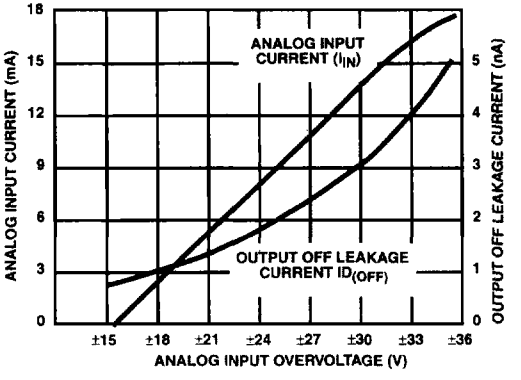


FIGURE 3A. ANALOG INPUT CURRENT AND OUTPUT OFF LEAKAGE CURRENT vs ANALOG INPUT OVER-VOLTAGE

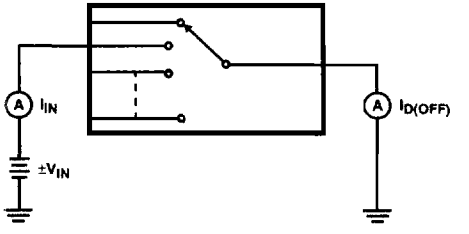


FIGURE 3B. ANALOG INPUT OVERVOLTAGE TEST CIRCUIT

FIGURE 3. ANALOG INPUT OVERVOLTAGE CHARACTERISTICS

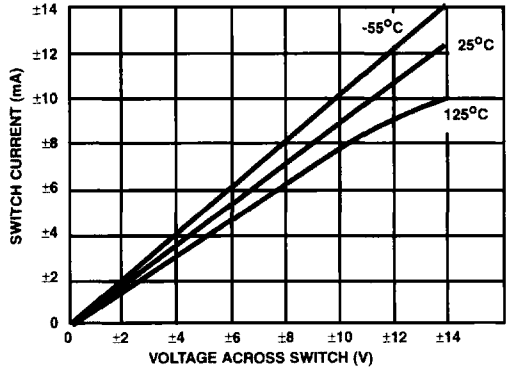


FIGURE 4A. ON CHANNEL CURRENT vs VOLTAGE

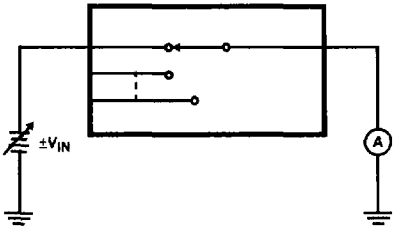


FIGURE 4B. ON CHANNEL CURRENT TEST CIRCUIT

FIGURE 4. ON CHANNEL CURRENT

Typical Performance Curves $T_A = 25^oC$, $V_{SUPPLY} = \pm15V$, $V_{AH} = +4V$, $V_{AL} = 0.8V$, V_{REF} = Open, Unless Otherwise Specified (Continued)

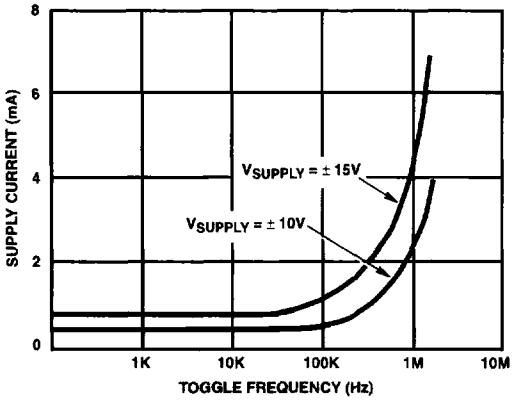
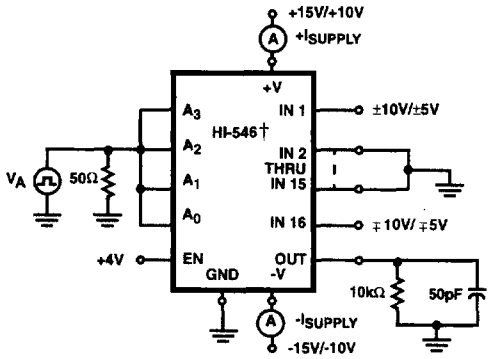


FIGURE 5A. SUPPLY CURRENT vs TOGGLE FREQUENCY



†Similar connection for HI-547/HI-548/HI-549.

FIGURE 5B. SUPPLY CURRENT vs TOGGLE FREQUENCY

FIGURE 5. SUPPLY CURRENT

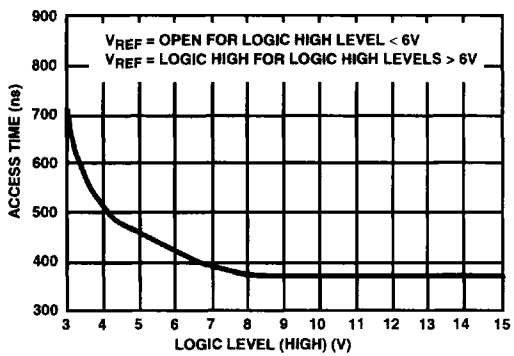
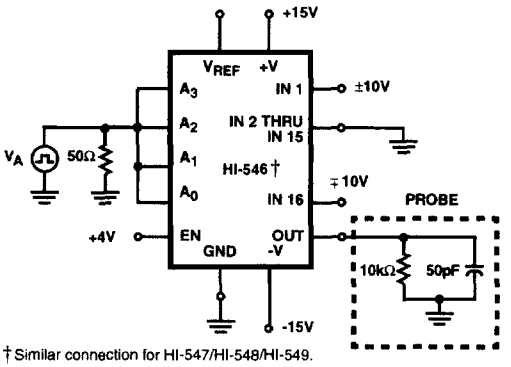


FIGURE 6A. ACCESS TIME vs LOGIC LEVEL (HIGH)



†Similar connection for HI-547/HI-548/HI-549.

FIGURE 6B. ACCESS TIME TEST CIRCUIT

FIGURE 6. ACCESS TIME

Switching Waveforms

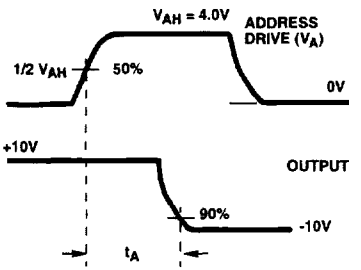


FIGURE 7A. ACCESS TIME MEASUREMENT

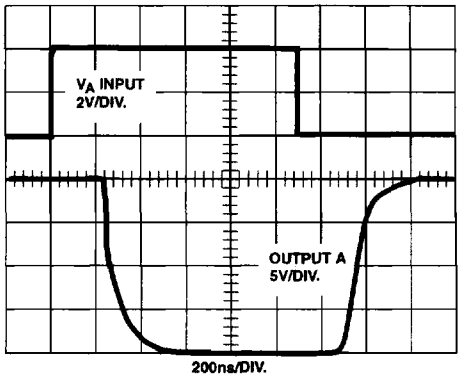
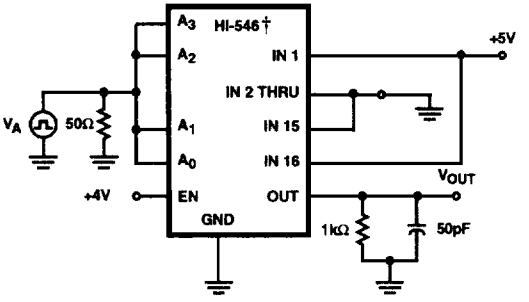


FIGURE 7B. ACCESS TIME WAVEFORMS

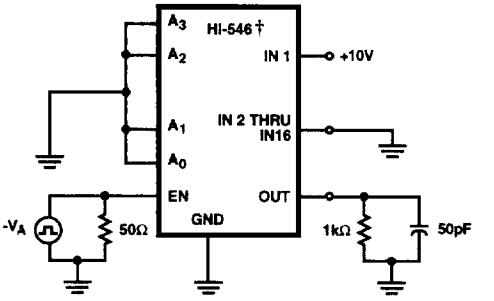
FIGURE 7. ACCESS TIME (Refer to Figure 6B for Test Circuit)

Switching Waveforms (Continued)



† Similar connection for HI-547/HI-548/HI-549

FIGURE 8A. BREAK-BEFORE-MAKE DELAY TEST CIRCUIT



† Similar connection for HI-547/HI-548/HI-549

FIGURE 9A. ENABLE DELAY TEST CIRCUIT

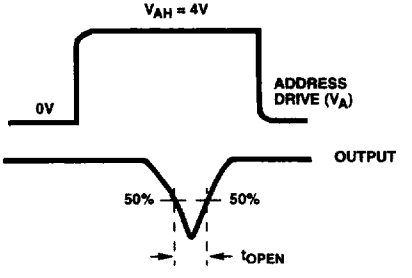


FIGURE 8B. BREAK-BEFORE-MAKE DELAY MEASUREMENT

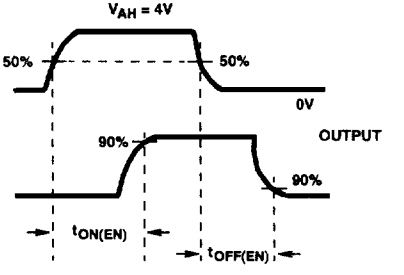


FIGURE 9B. ENABLE DELAY MEASUREMENTS

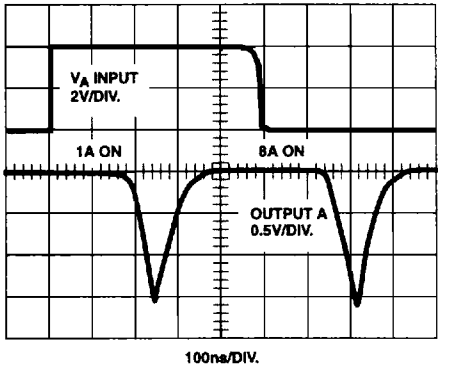


FIGURE 8C. BREAK-BEFORE-MAKE DELAY WAVEFORMS

FIGURE 8. BREAK-BEFORE-MAKE DELAY (t_{OPEN})

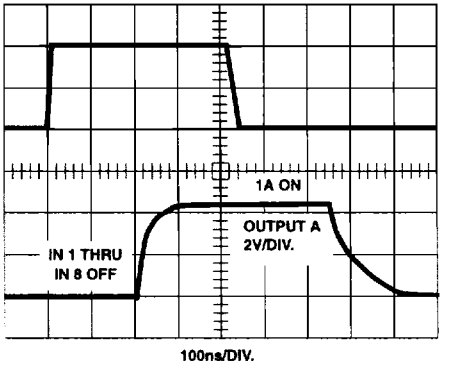


FIGURE 9C. ENABLE DELAY WAVEFORMS

FIGURE 9. ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)

Truth Tables

HI-546

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	None
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

HI-547

A_2	A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	X	L	None
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-548

A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	L	None
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-549

A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	L	None
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

Die Characteristics

DIE DIMENSIONS:

83.9 mils x 159 mils x 19 mils

METALLIZATION:

Type: CuAl
Thickness: 16kÅ ±2kÅ

SUBSTRATE POTENTIAL (NOTE):

$-V_{SUPPLY}$

PASSIVATION:

Type: Nitride Over Silox
Nitride Thickness: 3.5kÅ ±1kÅ
Silox Thickness: 12kÅ ±2kÅ

WORST CASE CURRENT DENSITY:

1.4×10^5 A/cm^2

TRANSISTOR COUNT:

HI-546: 485
HI-547: 485

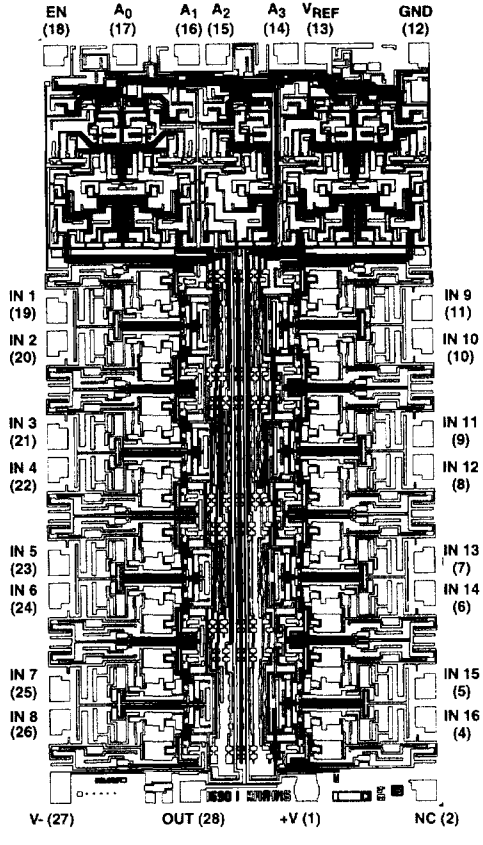
PROCESS:

CMOS-DI

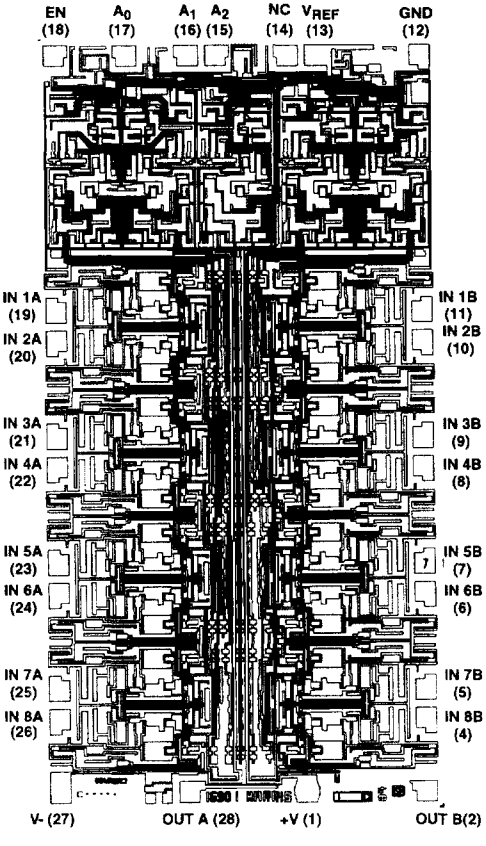
NOTE: The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential.

Metallization Mask Layouts

HI-546



HI-547



Die Characteristics

DIE DIMENSIONS:

83 mils x 108 mils x 19 mils

METALLIZATION:

Type: CuAl
Thickness: 16kÅ ±2kÅ

SUBSTRATE POTENTIAL (NOTE):

$-V_{SUPPLY}$

PASSIVATION:

Type: Nitride Over Silox
Nitride Thickness: 3.5kÅ ±1kÅ
Silox Thickness: 12kÅ ±2kÅ

WORST CASE CURRENT DENSITY:

1.4×10^5 A/cm

TRANSISTOR COUNT:

HI-548: 253
HI-549: 253

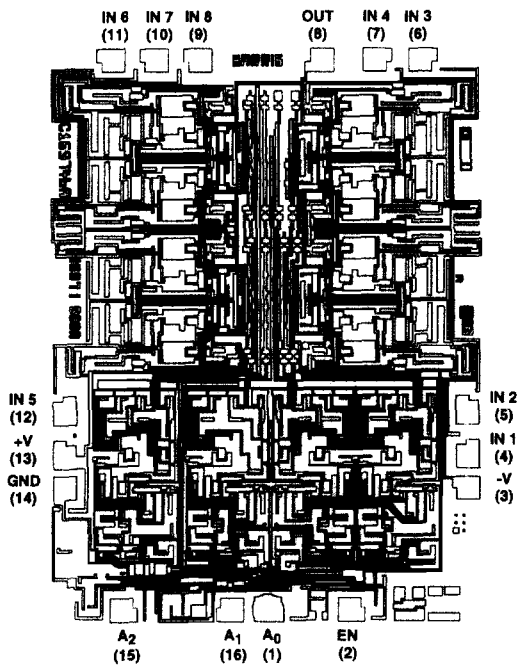
PROCESS:

CMOS-DI

NOTE: The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential.

Metallization Mask Layouts

HI-548



HI-549