

January 1998

## Fast CMOS 16-Bit Latched Transceivers

### Features

- Advanced 0.6 micron CMOS Technology
- These Devices Are High-speed, Low Power Devices with High Current Drive
- $V_{CC} = 5V \pm 10\%$
- Hysteresis on All Inputs
- CD74FCT16543T
  - High Output Drive:  $I_{OH} = -32mA$ ;  $I_{OL} = 64mA$
  - Power Off Disable Outputs Permit "Live Insertion"
  - Typical  $V_{OLP}$  (Output Ground Bounce)  $< 1.0V$  at  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$
- CD74FCT162543T
  - Balanced Output Drivers:  $\pm 24mA$
  - Reduced System Switching Noise
  - Typical  $V_{OLP}$  (Output Ground Bounce)  $< 0.6V$  at  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$
- CD74FCT162H543T
  - Bus Hold Retains Last Active Bus State During Three-State
  - Eliminates the Need for External Pull-Up Resistors

### Description

These devices are 16-bit latched transceivers organized with two sets of eight D-type latches with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable ( $\overline{x}CEAB$ ) input must be LOW in order to enter data from  $xAx$  or to take data from  $xBx$ , as indicated in the Truth Table. With  $\overline{x}CEAB$  LOW, a LOW signal makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the  $\overline{x}LEAB$  signal puts the A latches in the storage mode and their outputs no longer change the A inputs. With  $\overline{x}CEAB$  and  $\overline{x}OEAB$  both LOW, the three-state B output buffers are active and reflect the data present at the output of the A latches. Control of data from B to A is similar, but uses the  $\overline{x}CEBA$ ,  $\overline{x}LEBA$ , and  $\overline{x}OEBA$  inputs.

The CD74FCT16543T output buffers are designed with a Power-Off disable allowing "live insertion" of boards when used as backplane drivers.

The CD74FCT162543T has  $\pm 24mA$  balanced output drivers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications.

The CD74FCT162H543T has "Bus Hold" which retains the input's last state whenever the input goes to high impedance preventing "floating" inputs and eliminating the need for pull-up/down resistors.

### Ordering Information

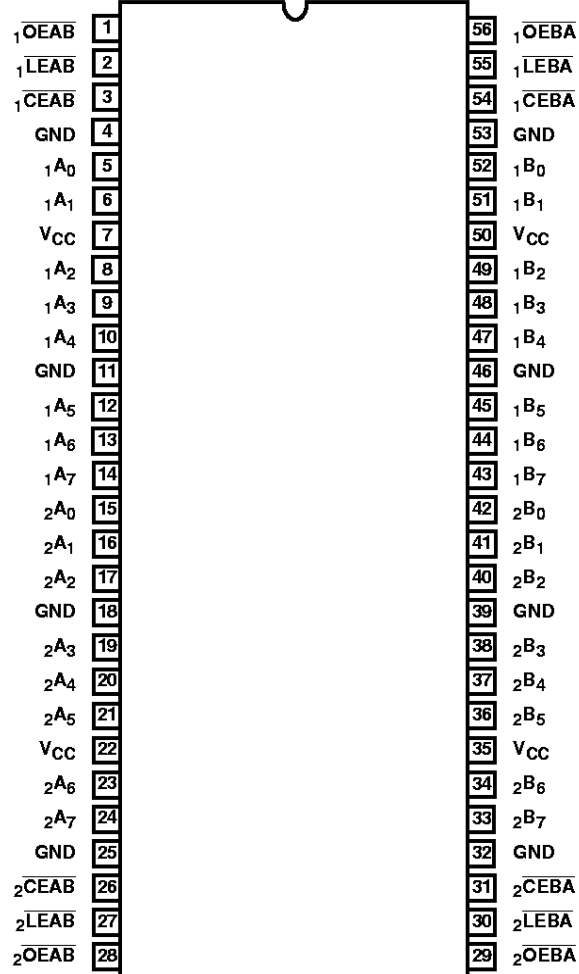
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT16543ATMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16543ATSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16543CTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16543CTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16543DTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16543DTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16543ETMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16543ETSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16543TMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16543TSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162543ATMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162543ATSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162543CTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162543CTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162543DTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162543DTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162543ETMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162543ETSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162543TMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162543TSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162H543ATMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162H543ATSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162H543CTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162H543CTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162H543DTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162H543DTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162H543ETMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162H543ETSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162H543TMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162H543TSM	-40 to 85	56 Ld SSOP	M56.300-P

NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

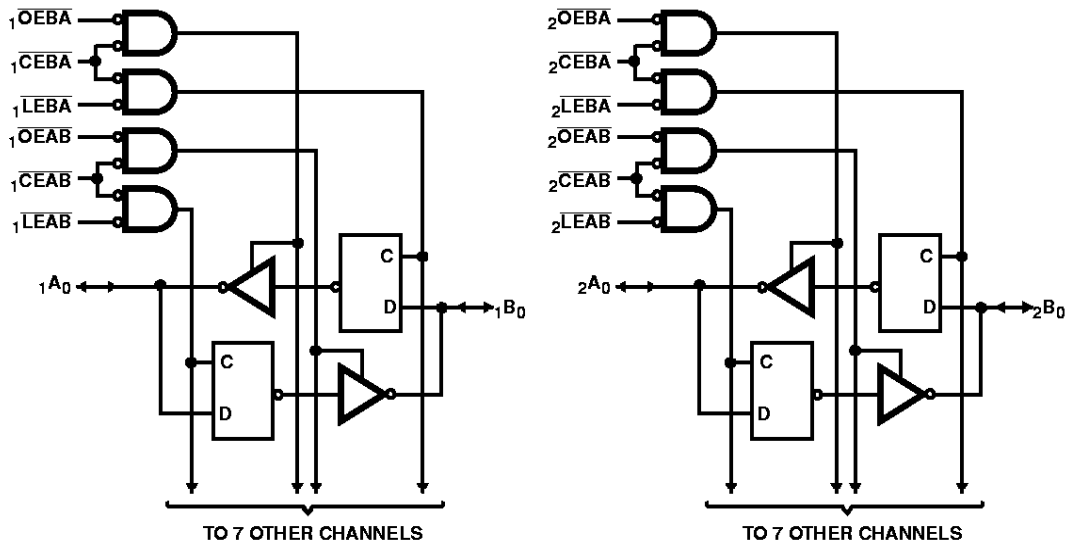
CD74FCT16543T, CD74FCT162543T, CD74FCT162H543T

Pinout

CD74FCT16543T, CD74FCT162543T, CD74FCT162H543T  
(SSOP, TSSOP)  
TOP VIEW



**Functional Block Diagram**



TRUTH TABLE (NOTES 1, 3)

INPUTS			LATCH STATUS	OUTPUT BUFFERS
$\overline{x}CEAB$	$\overline{x}LEAB$	$\overline{x}OEAB$	$xAx$ TO $xBx$	$xBx$
H	X	X	Storing	High Z
X	H	X	Storing	X
X	X	H	X	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous A Inputs (Note 2)

NOTES:

1. A-to-B data flow is shown. B-to-A flow control is the same except using  $\overline{x}CEBA$ ,  $\overline{x}LEBA$ , and  $\overline{x}OEBA$ .
2. Before  $\overline{x}LEAB$  LOW-to-HIGH Transition
3. H = High Voltage Level  
L = Low Voltage Level  
X = Don't Care or Irrelevant  
Z = High Impedance

**Pin Descriptions**

PIN NAME	DESCRIPTION
$\overline{x}OEAB$	A-to-B Output Enable Input (Active LOW)
$\overline{x}OEBA$	B-to-A Output Enable Input (Active LOW)
$\overline{x}CEAB$	A-to-B Enable Input (Active LOW)
$\overline{x}CEBA$	B-to-A Enable Input (Active LOW)
$\overline{x}LEAB$	A-to-B Latch Enable Input (Active LOW)
$\overline{x}LEBA$	B-to-A Latch Enable Input (Active LOW)
$xAx$	A-to-B Data Inputs or B-to-A Three-State Outputs
$xBx$	B-to-A Data Inputs or A-to-B Three-State Outputs (Note 4)
GND	Ground
$V_{CC}$	Power

NOTE:

4. For the CD74FCT162H543T, these pins have "Bus Hold". All other pins are standard, outputs, or I/Os.

## CD74FCT16543T, CD74FCT162543T, CD74FCT162H543T

### Absolute Maximum Ratings

DC Input Voltage ..... -0.5V to 7.0V  
 DC Output Current ..... 120mA

### Operating Conditions

Operating Temperature Range ..... -40°C to 85°C  
 Supply Voltage to Ground Potential  
   Inputs and V<sub>CC</sub> Only ..... -0.5V to 7.0V  
 Supply Voltage to Ground Potential  
   Outputs and D/O Only ..... -0.5V to 7.0V

### Thermal Information

Thermal Resistance (Typical, Note 5) θ<sub>JA</sub> (°C/W)  
   TSSOP Package ..... 85  
   SSOP Package ..... 70  
 Maximum Junction Temperature ..... 150°C  
 Maximum Storage Temperature Range ..... -65°C to 150°C  
 Maximum Lead Temperature (Soldering 10s) ..... 300°C  
   (Lead Tips Only)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

### NOTE:

5. θ<sub>JA</sub> is measured with the component mounted on an evaluation PC board in free air.

### Electrical Specifications

PARAMETER	SYMBOL	(NOTE 6) TEST CONDITIONS	MIN	(NOTE 7) TYP	MAX	UNITS	
<b>DC ELECTRICAL SPECIFICATIONS</b> Over the Operating Range, T <sub>A</sub> = -40°C to 85°C, V <sub>CC</sub> = 5.0V ±10%							
Input HIGH Voltage	V <sub>IH</sub>	Guaranteed Logic HIGH Level	2.0	-	-	V	
Input LOW Voltage	V <sub>IL</sub>	Guaranteed Logic LOW Level	-	-	0.8	V	
Input HIGH Current	I <sub>IH</sub>	Standard Input, V <sub>CC</sub> = Max					
		V <sub>IN</sub> = V <sub>CC</sub>	-	-	1	μA	
Input HIGH Current	I <sub>IH</sub>	Standard I/O, V <sub>CC</sub> = Max					
		V <sub>IN</sub> = V <sub>CC</sub>	-	-	1	μA	
Input HIGH Current	I <sub>IH</sub>	Bus Hold Input (Note 9) V <sub>CC</sub> = Max					
		V <sub>IN</sub> = V <sub>CC</sub>	-	-	±100	μA	
Input HIGH Current	I <sub>IH</sub>	Bus Hold I/O (Note 9) V <sub>CC</sub> = Max					
		V <sub>IN</sub> = V <sub>CC</sub>	-	-	±100	μA	
Input LOW Current	I <sub>IL</sub>	Standard Input, V <sub>CC</sub> = Min					
		V <sub>IN</sub> = GND	-	-	-1	μA	
Input LOW Current	I <sub>IL</sub>	Standard I/O, V <sub>CC</sub> = Min					
		V <sub>IN</sub> = GND	-	-	-1	μA	
Input LOW Current	I <sub>IL</sub>	Bus Hold Input (Note 9) V <sub>CC</sub> = Min					
		V <sub>IN</sub> = GND	-	-	±100	μA	
Input LOW Current	I <sub>IL</sub>	Bus Hold I/O (Note 9) V <sub>CC</sub> = Min					
		V <sub>IN</sub> = GND	-	-	±100	μA	
Bus Hold Sustain Current	I <sub>BHH</sub>	Bus Hold Input (Note 9) V <sub>CC</sub> = Min	V <sub>IN</sub> = 2.0V	-50	-	-	μA
	I <sub>BHL</sub>		V <sub>IN</sub> = 0.8V	50	-	-	μA
High Impedance Output Current (Three-State) (Note 10)	I <sub>OZH</sub>	V <sub>CC</sub> = Max	V <sub>OUT</sub> = 2.7V	-	-	1	μA
	I <sub>OZL</sub>	V <sub>CC</sub> = Max	V <sub>OUT</sub> = 0.5V	-	-	-1	μA
Clamp Diode Voltage	V <sub>IK</sub>	V <sub>CC</sub> = Min, I <sub>IN</sub> = -18mA	-	-0.7	-1.2	V	
Short Circuit Current	I <sub>OS</sub>	V <sub>CC</sub> = Max (Note 8), V <sub>OUT</sub> = GND	-80	-140	-200	mA	
Output Drive Current	I <sub>O</sub>	V <sub>CC</sub> = Max (Note 8), V <sub>OUT</sub> = 2.5V	-50	-	-180	mA	
Input Hysteresis	V <sub>H</sub>		-	100	-	mV	

**CD74FCT16543T, CD74FCT162543T, CD74FCT162H543T**

**Electrical Specifications (Continued)**

PARAMETER	SYMBOL	(NOTE 6) TEST CONDITIONS	MIN	(NOTE 7) TYP	MAX	UNITS	
<b>CD74FCT16543T OUTPUT DRIVE SPECIFICATIONS</b> Over the Operating Range							
Output HIGH Voltage	V <sub>OH</sub>	V <sub>CC</sub> = Min, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -3.0mA	2.5	3.5	-	V
			I <sub>OH</sub> = -15.0mA	2.4	3.5	-	V
			I <sub>OH</sub> = -32.0mA	2.0	3.0	-	V
Output LOW Voltage	V <sub>OL</sub>	V <sub>CC</sub> = Min, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 64mA	-	0.2	0.55	V
Power Down Disable	I <sub>OFF</sub>	V <sub>CC</sub> = 0V, V <sub>IN</sub> or V <sub>OUT</sub> ≤ 4.5V	-	-	±100	μA	
<b>CD74FCT162543T, CD74FCT162H543T OUTPUT DRIVE SPECIFICATIONS</b> Over the Operating Range							
Output HIGH Voltage	V <sub>OH</sub>	V <sub>CC</sub> = Min, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -24.0mA	2.4	3.3	-	V
Output LOW Voltage	V <sub>OL</sub>	V <sub>CC</sub> = Min, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 24mA	-	0.3	0.55	V
Output LOW Current	I <sub>ODL</sub>	V <sub>CC</sub> = 5V, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , V <sub>OUT</sub> = 1.5V (Note 8)	60	115	150	mA	
Output HIGH Current	I <sub>ODH</sub>	V <sub>CC</sub> = 5V, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , V <sub>OUT</sub> = 1.5V (Note 8)	-60	-115	-150	mA	
<b>CAPACITANCE</b> T <sub>A</sub> = 25°C, f = 1MHz							
Input Capacitance (Note 11)	C <sub>IN</sub>	V <sub>IN</sub> = 0V	-	4.5	6	pF	
Output Capacitance (Note 11)	C <sub>OUT</sub>	V <sub>OUT</sub> = 0V	-	5.5	8	pF	
<b>POWER SUPPLY SPECIFICATIONS</b>							
Quiescent Power Supply Current	I <sub>CC</sub>	V <sub>CC</sub> = Max	V <sub>IN</sub> = GND or V <sub>CC</sub>	-	0.1	500	μA
Supply Current per Input at TTL HIGH	ΔI <sub>CC</sub>	V <sub>CC</sub> = Max	V <sub>IN</sub> = 3.4V (Note 12)	-	0.5	1.5	mA
Supply Current per Input per MHz (Note 13)	I <sub>CCD</sub>	V <sub>CC</sub> = Max, Outputs Open x <sub>CEAB</sub> and $\overline{\text{OEAB}}$ = GND x <sub>CEBA</sub> = V <sub>CC</sub> One Bit Toggling 50% Duty Cycle	V <sub>IN</sub> = V <sub>CC</sub> V <sub>IN</sub> = GND	-	60	100	μA/MHz
Total Power Supply Current (Note 15)	I <sub>C</sub>	V <sub>CC</sub> = Max, Outputs Open f <sub>I</sub> = 10MHz, 50% Duty Cycle x <sub>LEAB</sub> , x <sub>CEAB</sub> , and x <sub>OEAB</sub> = GND x <sub>CEBA</sub> = V <sub>CC</sub> One Bit Toggling	V <sub>IN</sub> = V <sub>CC</sub> V <sub>IN</sub> = GND	-	0.6	1.5 (Note 14)	mA
			V <sub>IN</sub> = 3.4V V <sub>IN</sub> = GND	-	0.9	2.3 (Note 14)	mA
		V <sub>CC</sub> = Max, Outputs Open f <sub>I</sub> = 2.5MHz, 50% Duty Cycle x <sub>LEAB</sub> , x <sub>CEAB</sub> , and x <sub>OEAB</sub> = GND x <sub>CEBA</sub> = V <sub>CC</sub> 16 Bits Toggling	V <sub>IN</sub> = V <sub>CC</sub> V <sub>IN</sub> = GND	-	2.4	4.5 (Note 14)	mA
			V <sub>IN</sub> = 3.4V V <sub>IN</sub> = GND	-	6.4	16.5 (Note 14)	mA

**CD74FCT16543T, CD74FCT162543T, CD74FCT162H543T**

**Switching Specifications Over Operating Range**

PARAMETER	SYMBOL	(NOTE 16) TEST CONDITIONS	T		AT		CT		DT		ET		UNITS
			(NOTE 17) MIN	MAX	(NOTE 17) MIN	MAX	(NOTE 17) MIN	MAX	(NOTE 17) MIN	MAX	(NOTE 17) MIN	MAX	
Propagation Delay Transparent Mode $xA_x$ to $xB_x$ or $xB_x$ to $xA_x$	$t_{PLH}$ , $t_{PHL}$	$C_L = 50pF$ $R_L = 500\Omega$	2.5	8.5	2.5	6.5	2.5	5.3	2.5	4.4	1.5	3.4	ns
Propagation Delay $xLEBA$ to $xA_x$ $xLEAB$ to $xB_x$	$t_{PLH}$ , $t_{PHL}$		2.5	12.5	2.5	8.0	2.5	7.0	2.5	5.0	1.5	3.7	ns
Output Enable Time $xOEBA$ or $xOEAB$ to $xA_x$ or $xB_x$	$t_{PZH}$ , $t_{PZL}$		2.0	12.0	2.0	9.0	2.0	8.0	2.0	5.4	1.5	4.8	ns
Output Disable Time (Note 18) $xOEBA$ or $xOEAB$ to $xA_x$ or $xB_x$	$t_{PHZ}$ , $t_{PLZ}$		2.0	9.0	2.0	7.5	2.0	6.5	2.0	4.3	1.5	4.0	ns
Setup Time HIGH or LOW, $xA_x$ or $xB_x$ to $xLEAB$ or $xLEBA$	$t_{SU}$		3.0	-	2.0	-	2.0	-	2.0	-	1.0	-	ns
Hold Time HIGH or LOW, $xA_x$ or $xB_x$ to $xLEAB$ or $xLEBA$	$t_H$		2.0	-	2.0	-	2.0	-	1.5	-	1.0	-	ns
$xLEAB$ or $xLEBA$ Pulse Width LOW (Note 18)	$t_W$		5.0	-	5.0	-	5.0	-	3.0	-	3.0	-	ns
Output Skew (Note 19)	$t_{SK(O)}$		-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	ns

NOTES:

6. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
7. Typical values are at  $V_{CC} = 5.0V$ ,  $25^\circ C$  ambient and maximum loading, except as noted.
8. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
9. Pins with Bus Hold are identified in the pin description.
10. This specification does not apply to bi-directional functionalities with Bus Hold.
11. This parameter is determined by device characterization but is not production tested.
12. Per TTL driven input ( $V_{IN} = 3.4V$ ); all other inputs at  $V_{CC}$  or GND.
13. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
14. Values for these conditions are examples of the  $I_{CC}$  formula. These limits are guaranteed but not tested.
15.  $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$   
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$   
 $I_{CC}$  = Quiescent Current  
 $\Delta I_{CC}$  = Power Supply Current for a TTL High Input ( $V_{IN} = 3.4V$ )  
 $D_H$  = Duty Cycle for TTL Inputs High  
 $N_T$  = Number of TTL Inputs at  $D_H$   
 $I_{CCD}$  = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)  
 $f_{CP}$  = Clock Frequency for Register Devices (Zero for Non-Register Devices)  
 $f_I$  = Input Frequency  
 $N_I$  = Number of Inputs at  $f_I$   
 All currents are in milliamps and all frequencies are in megahertz.
16. See test circuit and wave forms.
17. Minimum limits are guaranteed but not tested on Propagation Delays.
18. This parameter is guaranteed but not production tested.
19. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.