

74F564 Octal D-Type Flip-Flop with TRI-STATE® Outputs

General Description

The 'F564 is a high-speed, low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable (\overline{OE}). The information presented to the D inputs is sorted in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

This device is functionally identical to the 'F574, but has inverted outputs.

Features

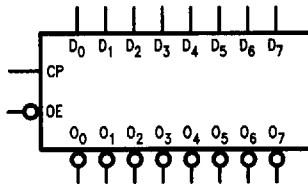
- Inputs and outputs on opposite sides of package allow easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to 'F574
- TRI-STATE outputs for bus-oriented applications

Ordering Code: See Section 11

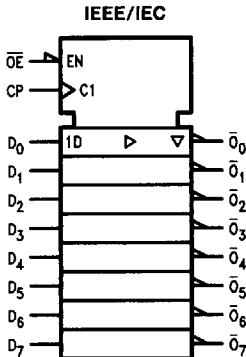
Commercial	Package Number	Package Description
74F564PC	N20A	20-Lead (0.300" Wide) Molded Dual-In-Line
74F564SJ (Note 1)	M20D	20-Lead (0.300" Wide) Molded Small Outline, EIAJ

Note 1: Devices also available in 13" reel. Use suffix = SJX.

Logic Symbols

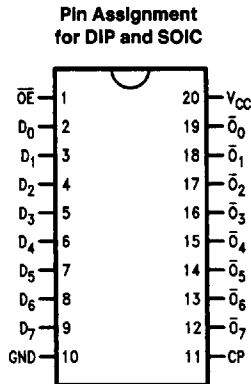


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Connection Diagram



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Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
D_0-D_7	Data Inputs	1.0/1.0	20 μ A/ -0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μ A/ -0.6 mA
\overline{OE}	TRI-STATE Output Enable Input (Active LOW)	1.0/1.0	20 μ A/ -0.6 mA
$\overline{O}_0-\overline{O}_7$	TRI-STATE Outputs	150/40 (33.3)	-3 mA/24 mA (20 mA)

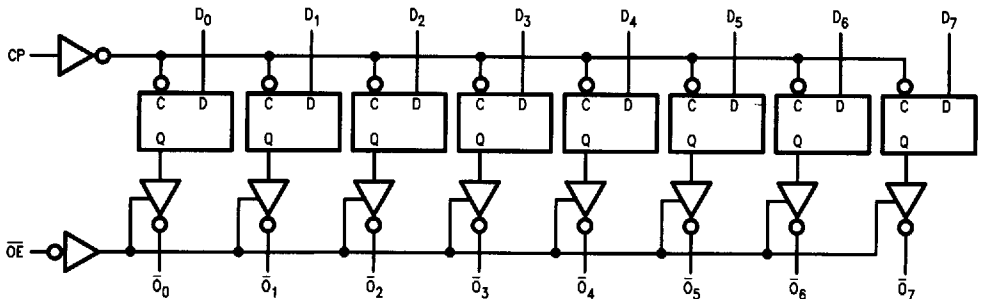
Functional Description

The 'F564 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable (\overline{OE}) LOW, the contents of the eight flip-flops are available at the outputs. When \overline{OE} is HIGH, the outputs go to the high impedance state. Operation of the \overline{OE} input does not affect the state of the flip-flops.

Function Table

Inputs			Internal	Outputs	Function
\overline{OE}	CP	D	Q	O	
H	H	L	NC	Z	Hold
H	H	H	NC	Z	Hold
H	↗	L	H	Z	Load
H	↗	H	L	Z	Load
L	↗	L	H	H	Data Available
L	↗	H	L	L	Data Available
L	H	L	NC	NC	No Change in Data
L	H	H	NC	NC	No Change in Data

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance
 ↗ = LOW-to-HIGH Transition
 NC = No Change

Logic Diagram


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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
Plastic	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	-0.5V to V _{CC}
TRI-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Commercial	
Supply Voltage	+4.5V to +5.5V
Commercial	

DC Electrical Characteristics

Symbol	Parameter	74F			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	74F 10% V _{CC}	2.5		V	Min	I _{OH} = -1 mA
		74F 10% V _{CC}	2.4				I _{OH} = -3 mA
		74F% 5% V _{CC}	2.7				I _{OH} = -1 mA
		74F% 5% V _{CC}	2.7				I _{OH} = -3 mA
V _{OL}	Output LOW Voltage	74F 10% V _{CC}		0.5	V	Min	I _{OL} = 24 mA
I _{IH}	Input HIGH Current	74F		5.0	μA	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test	74F		7.0	μA	Max	V _{IN} = 7.0V
I _{CEX}	Output HIGH Leakage Current	74F		50	μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	74F	4.75		V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current	74F		3.75	μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current			-0.6	mA	Max	V _{IN} = 0.5V
I _{OZH}	Output Leakage Current			50	μA	Max	V _{OUT} = 2.7V
I _{OZL}	Output Leakage Current			-50	μA	Max	V _{OUT} = 0.5V
I _{OS}	Output Short-Circuit Current		-60	-150	mA	Max	V _{OUT} = 0V
I _{ZZ}	Bus Drainage Test			500	μA	0.0V	V _{OUT} = 5.25V
I _{CCZ}	Power Supply Current		55	86	mA	Max	V _O = HIGH Z

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			74F		Units	Fig. No.
		T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A , V _{CC} = Com C _L = 50 pF			
		Min	Typ	Max	Min	Max		
f _{max}	Maximum Clock Frequency	100			70		MHz	2-1
t _{PLH} t _{PHL}	Propagation Delay CP to \bar{O}_n	2.5	5.2	8.5	2.5	8.5	ns	2-3
t _{PZH} t _{PZL}	Output Enable Time	3.0	5.6	9.0	2.5	10.0	ns	2-5
t _{PHZ} t _{PLZ}	Output Disable Time	1.5	3.4	5.5	1.5	6.5		
		1.5	2.7	5.5	1.5	6.5		

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74F		74F		Units	Fig. No.
		T _A = +25°C V _{CC} = +5.0V		T _A , V _{CC} = Com			
		Min	Max	Min	Max		
t _s (H) t _s (L)	Setup Time, HIGH or LOW D _n to CP	2.0		2.0		ns	2-6
		2.5		2.5			
t _h (H) t _h (L)	Hold Time, HIGH or LOW D _n to CP	2.0		2.0		ns	2-4
		2.0		2.0			
t _w (H) t _w (L)	CP Pulse Width HIGH or LOW	5.0		5.0		ns	
		5.0		5.0			