

January 1997

**NOT RECOMMENDED  
FOR NEW DESIGNS**  
Use CMOS Technology

## BiCMOS FCT Interface Logic, Octal Register/Transceiver, Three-State

### Features

- **Buffered Inputs**
- **Typical Propagation Delay: 6.4ns at  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ ,  $C_L = 50pF$**
- **Noninverting**
- **Family Features**
  - SCR Latchup Resistant BiCMOS Process and Circuit Design
  - Speed of Bipolar FAST™/AS/S
  - 64mA Output Sink Current
  - Output Voltage Swing Limited to 3.7V at  $V_{CC} = 5V$
  - Controlled Output Edge Rates
  - Input/Output Isolation to  $V_{CC}$
  - BiCMOS Technology with Low Quiescent Power

### Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT543EN	0 to 70	24 Ld PDIP	E24.3
CD74FCT543M	0 to 70	24 Ld SOIC	M24.3
CD74FCT543SM	0 to 70	24 Ld SSOP	M24.209

NOTE: When ordering the suffix M and SM packages, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

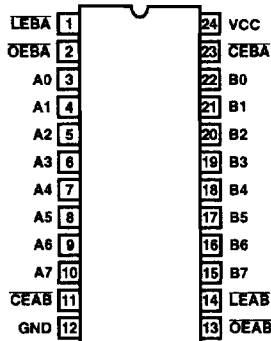
### Description

The CD74FCT543 three-state, octal register/transceiver uses a small geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output HIGH level to two diode drops below  $V_{CC}$ . This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes  $V_{CC}$  bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 64 milliamperes.

This device contains two sets of eight D-Type latches with separate input and output controls for each set. For data flow from A to B, for example, the A to B Enable ( $\overline{CEAB}$ ) input must be LOW in order to enter data from A0-A7 or to take data from B0-B7, as indicated in the Truth Table. With  $\overline{CEAB}$  LOW, a LOW signal on the A to B Latch Enable ( $\overline{LEAB}$ ) input makes the A to B latches transparent; a subsequent LOW to HIGH transition of the  $\overline{LEAB}$  signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With  $\overline{CEAB}$  and  $\overline{OEAB}$  both LOW, the three state B output buffers are active and reflect the data present at the output of the A latches. Control of data from B to A is similar, but uses the  $\overline{CEBA}$ ,  $\overline{LEBA}$ , and  $\overline{OEBA}$  inputs.

### Pinout

CD74FCT543  
(PDIP, SOIC, SSOP)  
TOP VIEW



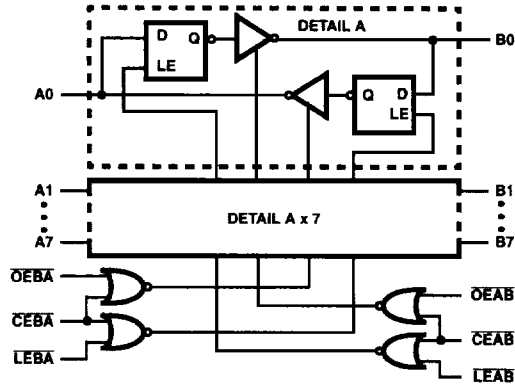
8  
BiCMOS FCT  
PRODUCTS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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# CD74FCT543

## Functional Diagram



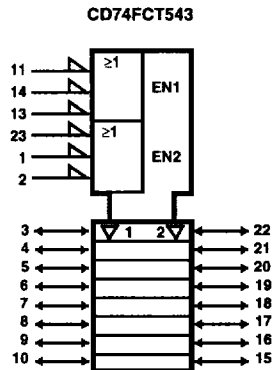
TRUTH TABLE For A to B (Symmetric with B to A)

INPUTS			LATCH STATUS	OUTPUT BUFFERS
CEAB	LEAB	OEAB	A TO B	B0 THRU B7
H	X	X	Storing	High Z
X	H	-	Storing	-
X	-	H	-	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous A Inputs (Note 1)

**NOTE:**

- Before  $\overline{LEAB}$  LOW to HIGH Transition  
 H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 A to B data flow shown; B to A flow control is the same, except using  $\overline{CEBA}$ ,  $\overline{LEBA}$ , and  $\overline{OEBA}$ .

## IEC Logic Symbol



# CD74FCT543

## Absolute Maximum Ratings

DC Supply Voltage ( $V_{CC}$ )	-0.5V to 6V
DC Input Diode Current, $I_{IK}$ (For $V_I < -0.5V$ )	-20mA
DC Output Diode Current, $I_{OK}$ (for $V_O < -0.5V$ )	-50mA
DC Output Sink Current per Output Pin, $I_O$	70mA
DC Output Source Current per Output Pin, $I_O$	-30mA
DC $V_{CC}$ Current ( $I_{CC}$ )	140mA
DC Ground Current ( $I_{GND}$ )	528mA

## Thermal Information

Thermal Resistance (Typical, Note 2)	$\theta_{JA}$ ( $^{\circ}C/W$ )
PDIP Package	75
SOIC Package	75
SSOP Package	125
Maximum Junction Temperature	150 $^{\circ}C$
Maximum Storage Temperature Range	-65 $^{\circ}C$ to 150 $^{\circ}C$
Maximum Lead Temperature (Soldering 10s)	300 $^{\circ}C$ (SOIC and SSOP-Lead Tips Only)

## Operating Conditions

Operating Temperature Range ( $T_A$ )	0 $^{\circ}C$ to 70 $^{\circ}C$
Supply Voltage Range, $V_{CC}$	4.75V to 5.25V
DC Input Voltage, $V_I$	0 to $V_{CC}$
DC Output Voltage, $V_O$	0 to $\leq V_{CC}$
Input Rise and Fall Slew Rate, $dt/dv$	0 to 10ns/V

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### NOTE:

- $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

## Electrical Specifications Commercial Temperature Range 0 $^{\circ}C$ to 70 $^{\circ}C$ , $V_{CC}$ Max = 5.25V, $V_{CC}$ Min = 4.75V

PARAMETER	SYMBOL	TEST CONDITIONS		$V_{CC}$ (V)	AMBIENT TEMPERATURE ( $T_A$ )				UNITS
					25 $^{\circ}C$		0 $^{\circ}C$ TO 70 $^{\circ}C$		
					MIN	MAX	MIN	MAX	
High Level Input Voltage	$V_{IH}$			4.75 to 5.25	2	-	2	-	V
Low Level Input Voltage	$V_{IL}$			4.75 to 5.25	-	0.8	-	0.8	V
High Level Output Voltage	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-15	Min	2.4	-	2.4	-	V
Low Level Output Voltage	$V_{OL}$	$V_{IH}$ or $V_{IL}$	64	Min	-	0.55	-	0.55	V
High Level Input Current	$I_{IH}$	$V_{CC}$		Max	-	0.1	-	1	$\mu A$
Low Level Input Current	$I_{IL}$	GND		Max	-	-0.1	-	-1	$\mu A$
Three-State Leakage Current	$I_{OZH}$	$V_{CC}$		Max	-	0.5	-	10	$\mu A$
		GND		Max	-	-0.5	-	-10	$\mu A$
Input Clamp Voltage	$V_{IK}$	$V_{CC}$ or GND	-18	Min	-	-1.2	-	-1.2	V
Short Circuit Output Current (Note 3)	$I_{OS}$	$V_O = 0$ $V_{CC}$ or GND		Max	-60	-	-60	-	mA
Quiescent Supply Current, MSI	$I_{CC}$	$V_{CC}$ or GND	0	Max	-	8	-	80	$\mu A$
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	$\Delta I_{CC}$	3.4V (Note 4)		Max	-	1.6	-	1.6	mA

### NOTES:

- Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
- Inputs that are not measured are at  $V_{CC}$  or GND.
- FCT Input Loading: All inputs are 1 unit load. Unit load is  $\Delta I_{CC}$  limit specified in Electrical Specifications table, e.g., 1.6mA Max. at 70 $^{\circ}C$ .

## CD74FCT543

### Switching Specifications Over Operating Range FCT Series $t_r, t_f = 2.5\text{ns}$ , $C_L = 50\text{pF}$ , $R_L$ (Figure 4)

PARAMETER	SYMBOL	$V_{CC}$ (V)	25°C	0°C TO 70°C			UNITS
			TYP	MIN	TYP	MAX	
<b>Propagation Delays</b>							
An $\leftrightarrow$ Bn	$t_{PLH}, t_{PHL}$	5	6.4	2.5	-	8.5	ns
LEBA to An or LEAB to Bn	$t_{PLH}, t_{PHL}$	5	9.4	2.5	-	12.5	ns
CEBA or CEAB to An or Bn	$t_{PLZ}, t_{PHZ}$	5	6.8	2	-	9	ns
	$t_{PZL}, t_{PZH}$	5	9	2	-	12	ns
Power Dissipation Capacitance	$C_{PD}$ (Note 6)	-	49	-	49	-	pF
Minimum (Valley) $V_{OHV}$ During Switching of Other Outputs (Output Under Test Not Switching)	$V_{OHV}$	5	0.5	-	-	-	V
Maximum (Peak) $V_{OLP}$ During Switching of Other Outputs (Output Under Test Not Switching)	$V_{OLP}$	5	1	-	-	-	V
Input Capacitance	$C_I$	-	-	-	-	10	pF
Input/Output Capacitance	$C_{I/O}$	-	-	-	-	15	pF

NOTE:

6.  $C_{PD}$ , measured per flip-flop, is used to determine the dynamic power consumption.

$P_D$  (per package) =  $V_{CC} I_{CC} + \Sigma(V_{CC}^2 f_I C_{PD} + V_O^2 f_O C_L + V_{CC} \Delta I_{CC} D)$  where:

$V_{CC}$  = supply voltage

$\Delta I_{CC}$  = flow through current x unit load

$C_L$  = output load capacitance

D = duty cycle of input high

$f_O$  = output frequency

$f_I$  = input frequency

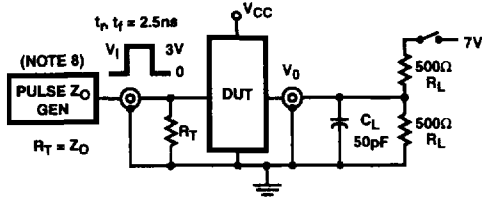
### Prerequisite for Switching

PARAMETER	SYMBOL	$V_{CC}$ (V)	25°C	0°C TO 70°C		UNITS
			TYP	MIN	MAX	
Data to Latch Enable Setup Time	$t_{SU}$	5 (Note 7)	-	3	-	ns
Data to Latch Enable Hold Time	$t_H$	5	-	2	-	ns
Latch Enable Pulse Width	$t_W$	5	-	9	-	ns

NOTE:

7. 5V: Minimum is at 4.75V for 0°C to 70°C, Typical is at 5V.

Test Circuits and Waveforms



NOTE:

8. Pulse Generator for All Pulses: Rate  $\leq 1.0\text{MHz}$ ;  $Z_{OUT} \leq 50\Omega$ ;  $t_r, t_f \leq 2.5\text{ns}$ .

FIGURE 1. TEST CIRCUIT

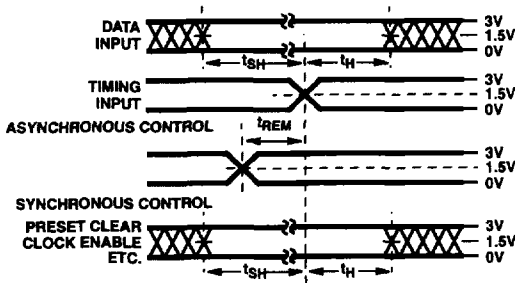


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

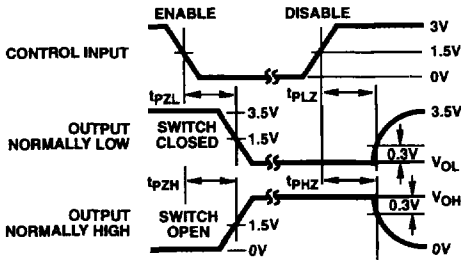


FIGURE 4. ENABLE AND DISABLE TIMING

SWITCH POSITION	
TEST	SWITCH
$t_{pZL}, t_{pZL}$ , Open Drain	Closed
$t_{pZH}, t_{pZH}, t_{pLH}, t_{pLH}$	Open

DEFINITIONS:

$C_L$  = Load capacitance, includes jig and probe capacitance.

$R_T$  = Termination resistance, should be equal to  $Z_{OUT}$  of the Pulse Generator.

$V_{IN} = 0\text{V}$  to  $3\text{V}$ .

Input:  $t_r = t_f = 2.5\text{ns}$  (10% to 90%), unless otherwise specified

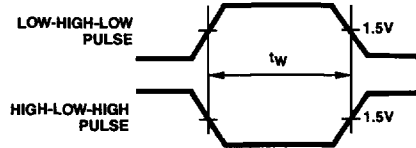


FIGURE 3. PULSE WIDTH

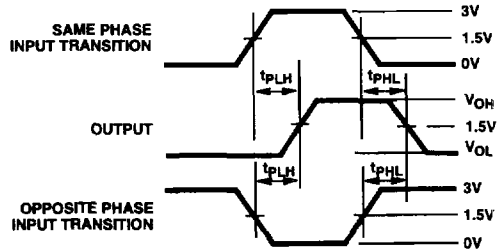
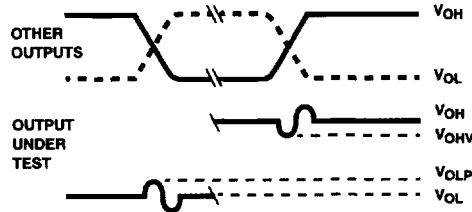


FIGURE 5. PROPAGATION DELAY



NOTES:

- $V_{OLP}$  is measured with respect to a ground reference near the output under test.  $V_{OHV}$  is measured with respect to  $V_{OH}$ .
- Input pulses have the following characteristics:  
 $P_{RR} \leq 1\text{MHz}$ ,  $t_r = 2.5\text{ns}$ ,  $t_f = 2.5\text{ns}$ , skew 1ns.
- R.F. fixture with 700MHz design rules required. IC should be soldered into test board and bypassed with  $0.1\mu\text{F}$  capacitor. Scope and probes require 700MHz bandwidth.

FIGURE 6. SIMULTANEOUS SWITCHING TRANSIENT WAVEFORMS

BICMOS FCT PRODUCTS