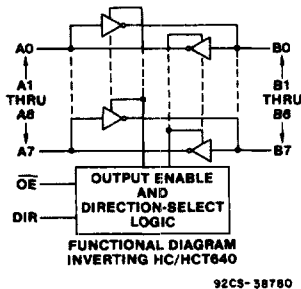


# CD54/74HC640, CD54/74HCT640 CD54/74HC643, CD54/74HCT643

## High-Speed CMOS Logic



### Octal 3-State Bus Transceivers

Inverting (HC/HCT640)  
True/Inverting (HC/HCT643)

**Type Features:**

- 3-state outputs
- Buffered inputs
- Applications in multiple-data-bus architecture

The RCA-CD54/74HC640, 643 and CD54/74HCT640, 643 silicon-gate CMOS 3-state bidirectional inverting and non-inverting buffers are intended for two-way asynchronous communication between data buses. They have high drive current outputs which enable high-speed operation when driving large bus capacitances. These circuits possess the low power dissipation of CMOS circuits, and have speeds comparable to low power Schottky TTL circuits. They can drive 15 LSTTL loads.

The CD54/74HC640 and CD54/74HCT640 are inverting buffers; the CD54/74HC643 and CD54/74HCT643 are true/inverting buffers.

The direction of data flow (A to B, B to A) is controlled by the DIR input.

Outputs are enabled by a low on the Output Enable input ( $\overline{OE}$ ); a high  $\overline{OE}$  puts these devices in the high impedance mode.

The CD54HC640, 643 and the CD54HCT640, 643 are supplied in 20-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC640, 643 and CD74HCT640, 643 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line surface mount plastic packages (M suffix). These devices are also supplied in chip form (H suffix).

**Family Features:**

- **Fanout (over temperature range):**  
Standard outputs - 10 LSTTL loads  
Bus driver outputs - 15 LSTTL loads
- **Wide operating temperature range:**  
CD74HC/HCT: -40 to +85° C
- **Balanced propagation delay and transition times**
- **Significant power reduction compared to LSTTL logic ICs**
- **Alternate source is Philips/Signetics**
- **CD54HC/CD74HC types:**  
2 to 6 V operation  
High noise immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$   
@  $V_{CC} = 5$  V
- **CD54HCT/CD74HCT types:**  
4.5 to 5.5 V operation  
Direct LSTTL input logic compatibility  
 $V_{IL} = 0.8$  V max.,  $V_{IH} = 2$  V min.  
CMOS input compatibility  
 $I_i \leq 1 \mu A$  @  $V_{OL}$ ,  $V_{OH}$

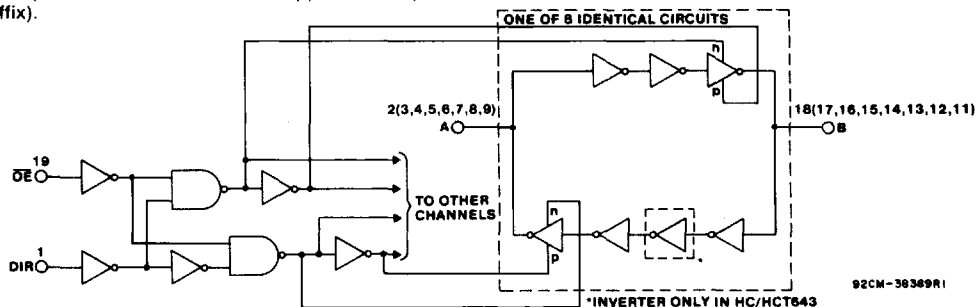
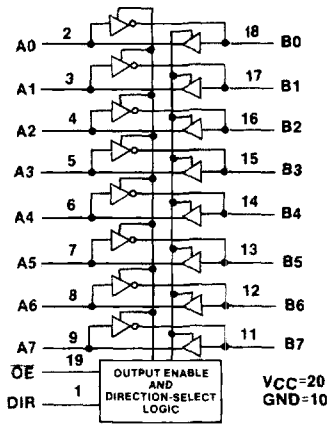


Fig. 1 - Logic diagram.

# CD54/74HC640, CD54/74HCT640 CD54/74HC643, CD54/74HCT643



**FUNCTIONAL DIAGRAM  
TRUE/INVERTING HC/HCT643**

92CS-38484

**TRUTH TABLE**

CONTROL INPUTS		HC, HCT640 Series		HC, HCT643 Series	
		DATA PORT STATUS		DATA PORT STATUS	
$\overline{OE}$	DIR	$A_n$	$B_n$	$A_n$	$B_n$
L	L	$\overline{O}$	I	O	I
H	H	Z	Z	Z	Z
H	L	Z	Z	Z	Z
L	H	I	$\overline{O}$	I	$\overline{O}$

To prevent excess currents in the High-Z modes all I/O terminals should be terminated with 10K $\Omega$  to 1M $\Omega$  resistors.

H = High

O = Output (Same Level as Input)

L = Low

$\overline{O}$  = Output (Inversion of Input Level)

I = Input

Z = High Impedance

**MAXIMUM RATINGS, Absolute-Maximum Values:**

**DC SUPPLY-VOLTAGE, ( $V_{CC}$ ):**

(Voltages referenced to ground) ..... -0.5 to +7 V

DC INPUT DIODE CURRENT,  $I_{IK}$  (FOR  $V_i < -0.5$  V OR  $V_i > V_{CC} + 0.5$  V) .....  $\pm 20$  mA

DC OUTPUT DIODE CURRENT,  $I_{OK}$  (FOR  $V_o < -0.5$  V OR  $V_o > V_{CC} + 0.5$  V) .....  $\pm 20$  mA

DC DRAIN CURRENT, PER OUTPUT ( $I_o$ ) (FOR  $-0.5$  V <  $V_o < V_{CC} + 0.5$  V) .....  $\pm 35$  mA

DC  $V_{CC}$  OR GROUND CURRENT, ( $I_{CC}$ ) .....  $\pm 70$  mA

**POWER DISSIPATION PER PACKAGE ( $P_D$ ):**

For  $T_A = -40$  to  $+60^\circ$  C (PACKAGE TYPE E) ..... 500 mW

For  $T_A = +60$  to  $+85^\circ$  C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/ $^\circ$ C to 300 mW

For  $T_A = -55$  to  $+100^\circ$  C (PACKAGE TYPE F, H) ..... 500 mW

For  $T_A = +100$  to  $+125^\circ$  C (PACKAGE TYPE F, H) ..... Derate Linearly at 8 mW/ $^\circ$ C to 300 mW

For  $T_A = -40$  to  $+70^\circ$  C (PACKAGE TYPE M) ..... 400 mW

For  $T_A = +70$  to  $+125^\circ$  C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/ $^\circ$  C to 70 mW

**OPERATING-TEMPERATURE RANGE ( $T_A$ ):**

PACKAGE TYPE F, H ..... -55 to  $+125^\circ$  C

PACKAGE TYPE E, M ..... -40 to  $+85^\circ$  C

STORAGE TEMPERATURE ( $T_{stg}$ ) ..... -65 to  $+150^\circ$  C

**LEAD TEMPERATURE (DURING SOLDERING):**

At distance 1/16  $\pm$  1/32 in. (1.59  $\pm$  0.79 mm) from case for 10 s max. ....  $+265^\circ$  C

Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only .....  $+300^\circ$  C

**RECOMMENDED OPERATING CONDITIONS**

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For $T_A$ =Full Package Temperature Range) $V_{CC}^*$			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage, $V_i$ , $V_o$	0	$V_{CC}$	V
Operating Temperature, $T_A$ :			
CD74 Types	-40	+85	$^\circ$ C
CD54 Types	-55	+125	
Input Rise and Fall Times, $t_r$ , $t_f$ :			
at 2 V	0	1000	ns
at 4.5 V	0	500	
at 6 V	0	400	

\*Unless otherwise specified, all voltages are referenced to Ground.

# CD54/74HC640, CD54/74HCT640 CD54/74HC643, CD54/74HCT643

## STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CD74HC640/643/CD54HC640/643										CD74HCT640/643/CD54HCT640/643								UNITS			
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPE			74HCT TYPE		54HCT TYPE				
	V <sub>i</sub> V	I <sub>o</sub> mA	V <sub>cc</sub> V	+25°C			-40/ +85°C		-55/ +125°C		V <sub>i</sub> V	V <sub>cc</sub> V	+25°C			-40/ +85°C		-55/ +125°C				
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min		Max		
High-Level Input Voltage	V <sub>IH</sub>		2	1.5	—	—	1.5	—	1.5	—	—	4.5	to	2	—	—	2	—	2	—	V	
			4.5	3.15	—	—	3.15	—	3.15	—	—	5.5										
			6	4.2	—	—	4.2	—	4.2	—												
Low-Level Input Voltage	V <sub>IL</sub>		2	—	—	0.5	—	0.5	—	0.5	—	4.5	to	—	—	0.8	—	0.8	—	0.8	—	V
			4.5	—	—	1.35	—	1.35	—	1.35	—	5.5										
			6	—	—	1.8	—	1.8	—	1.8	—											
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IL</sub> or	2	1.9	—	—	1.9	—	1.9	—	V <sub>IL</sub> or	4.5	4.4	—	—	4.4	—	4.4	—	4.4	—	V
CMOS Loads	V <sub>IH</sub>	-0.02	4.5	4.4	—	—	4.4	—	4.4	—	V <sub>IH</sub>	5.5										
			6	5.9	—	—	5.9	—	5.9	—												
TTL Loads		V <sub>IL</sub> or									V <sub>IL</sub> or	4.5	3.98	—	—	3.84	—	3.7	—			V
Bus Driver	V <sub>IH</sub>		-7.8	6	5.48	—	—	5.34	—	5.2	—	V <sub>IH</sub>										
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IL</sub> or	2	—	—	0.1	—	0.1	—	0.1	—	V <sub>IL</sub> or	4.5	—	—	0.1	—	0.1	—	0.1	—	V
CMOS Loads	V <sub>IH</sub>	0.02	4.5	—	—	0.1	—	0.1	—	0.1	—	5.5										
			6	—	—	0.1	—	0.1	—	0.1	—											
TTL Loads		V <sub>IL</sub> or									V <sub>IL</sub> or	4.5	—	—	0.26	—	0.33	—	0.4	—		V
Bus Driver	V <sub>IH</sub>		6	4.5	—	—	0.26	—	0.33	—	0.4	V <sub>IH</sub>										
			7.8	6	—	—	0.26	—	0.33	—	0.4											
Input Leakage Current	I <sub>i</sub>	V <sub>cc</sub> or Gnd	6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V <sub>cc</sub> and Gnd	5.5	—	—	±0.1	—	±1	—	±1	—	±1	μA
Quiescent Device Current	I <sub>cc</sub>	V <sub>cc</sub> or Gnd	0	6	—	—	8	—	80	—	160	V <sub>cc</sub> or Gnd	5.5	—	—	8	—	80	—	160	—	μA
Additional Quiescent Device Current per Input Pin: 1 Unit Load	ΔI <sub>cc</sub> *										V <sub>cc</sub> -2.1	4.5 to 5.5	—	100	360	—	450	—	490	—	μA	
3-State Leakage Current	I <sub>oz</sub>	V <sub>IL</sub> or V <sub>IH</sub>	V <sub>O</sub> = V <sub>cc</sub> or Gnd	6	—	—	±0.5	—	±5	—	±10	V <sub>IL</sub> or V <sub>IH</sub>	5.5	—	—	±0.5	—	±5	—	±10	—	μA

\*For dual-supply systems theoretical worst case (V<sub>i</sub> = 2.4 V, V<sub>cc</sub> = 5.5 V) specification is 1.8 mA.

### HCT INPUT LOADING TABLE

INPUT	UNIT LOADS *	
	HCT640	HCT643
DIR	0.9	0.9
OE, A	1.5	1.5
B	1.5	0.4

\* Unit load is ΔI<sub>cc</sub> limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

# CD54/74HC640, CD54/74HCT640 CD54/74HC643, CD54/74HCT643

SWITCHING CHARACTERISTICS ( $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{ C}$ , Input  $t_r$ ,  $t_f = 6\text{ ns}$ )

CHARACTERISTIC	$C_L$ pF	SYMBOL	TYPICAL VALUES				UNITS
			HC640	HCT640	HC643	HCT643	
Propagation Delay	15	$t_{PHL}, t_{PLH}$	7	9	7	9	ns
A → $\bar{B}$ , B → $\bar{A}$			—	—	9	10	
B → A		$t_{PHZ}, t_{PLZ}$	12	12	12	12	
Enable to High Z			$t_{PZH}, t_{PZL}$	12	12	12	
Enable from High Z							
Power Dissipation Capacitance	—	$C_{PD}^*$	38	41	45	55	pF

\*  $C_{PD}$  is used to determine the dynamic power consumption per channel.

$P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ , where:  $f_i$  = input frequency.  $C_L$  = output load capacitance.  $V_{CC}$  = supply voltage.

SWITCHING CHARACTERISTICS ( $C_L = 50\text{ pF}$ , Input  $t_r, t_f = 6\text{ ns}$ )

CHARACTERISTIC	SYMBOL	$V_{CC}$	25°C				-40°C to +85°C				-55°C to +125°C				UNITS														
			HC		HCT		74HC		74HCT		54HC		54HCT																
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.															
Propagation Delay	$t_{PLH}$	2	—	90	—	—	—	115	—	—	—	135	—	—	ns														
A → $\bar{B}$	$t_{PHL}$	4.5	—	18	—	22	—	23	—	28	—	27	—	33															
B → $\bar{A}$		6	—	15	—	—	—	20	—	—	—	23	—	—															
B → A	$t_{PLH}$	2	—	110	—	—	—	140	—	—	—	165	—	—	ns														
	$t_{PHL}$	4.5	—	22	—	26	—	28	—	33	—	33	—	39															
		6	—	19	—	—	—	24	—	—	—	28	—	—															
Output High-Z:	$t_{PZH}$	2	—	150	—	—	—	190	—	—	—	225	—	—	ns														
To High Level,																$t_{PZL}$	4.5	—	30	—	30	—	38	—	38	—	45	—	45
To Low Level																													
Output High Level,	$t_{PHZ}$	2	—	150	—	—	—	190	—	—	—	225	—	—	ns														
Output Low Level																$t_{PLZ}$	4.5	—	30	—	30	—	38	—	38	—	45	—	45
to High Z																													
Output High Z:	$t_{PZH}$	2	—	150	—	—	—	190	—	—	—	225	—	—	ns														
To High Level																$t_{PZL}$	4.5	—	30	—	33	—	38	—	41	—	45	—	50
To Low Level																													
Output High Level,	$t_{PHZ}$	2	—	150	—	—	—	190	—	—	—	225	—	—	ns														
Output Low Level																$t_{PLZ}$	4.5	—	30	—	30	—	38	—	38	—	45	—	45
to High Z																													
Output Transition Time	$t_{TLH}$	2	—	60	—	—	—	75	—	—	—	90	—	—	ns														
	$t_{THL}$	4.5	—	12	—	12	—	15	—	15	—	18	—	18															
		6	—	10	—	—	—	13	—	—	—	15	—	—															
Input Capacitance	$C_{in}$		—	10	—	10	—	10	—	10	—	10	—	10	pF														
3-State Output Capacitance	$C_o$		—	20	—	20	—	20	—	20	—	20	—	20	pF														

# CD54/74HC640, CD54/74HCT640 CD54/74HC643, CD54/74HCT643

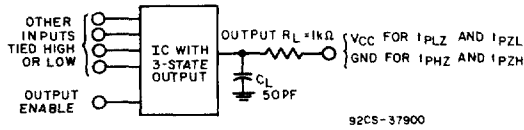
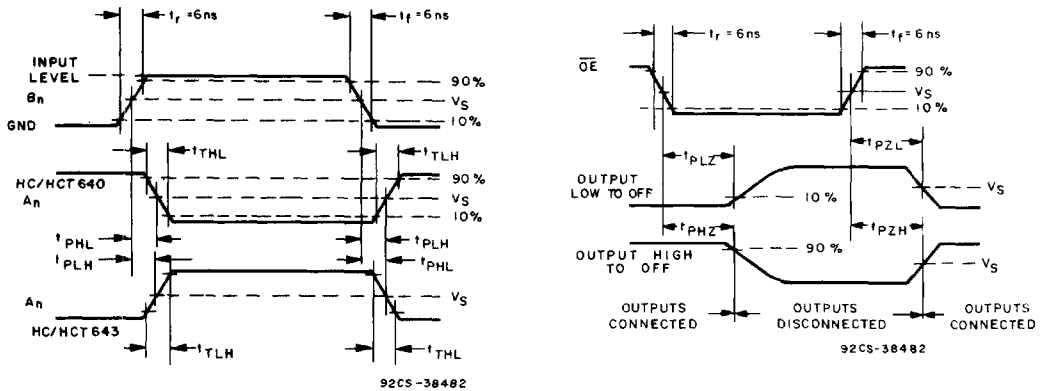
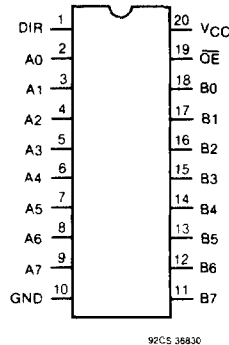


Fig. 2 - Three-state propagation delay test circuit.



	54/74HC	54/74HCT
Input Level	$V_{CC}$	3 V
Switching Voltage, $V_S$	50% $V_{CC}$	1.3 V

Fig. 3 - Transition times and propagation delay times.



**TERMINAL ASSIGNMENT**