

MC74AC374, MC74ACT374

Octal D-Type Flip-Flop with 3-State Outputs

The MC74AC374/74ACT374 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable (\overline{OE}) are common to all flip-flops.

- Buffered Positive Edge-Triggered Clock
- 3-State Outputs for Bus-Oriented Applications
- Outputs Source/Sink 24 mA
- See MC74AC273 for Reset Version
- See MC74AC377 for Clock Enable Version
- See MC74AC373 for Transparent Latch Version
- See MC74AC574 for Broadside Pinout Version
- See MC74AC564 for Broadside Pinout Version with Inverted Outputs
- 'ACT374 Has TTL Compatible Inputs

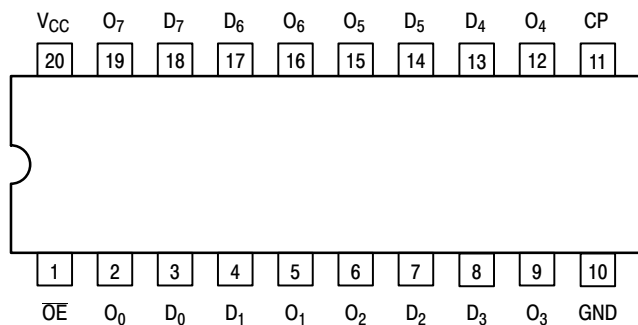


Figure 1. Pinout: 20 Lead Packages Conductors (Top View)

PIN ASSIGNMENT

PIN	FUNCTION
D ₀ –D ₇	Data Inputs
CP	Clock Pulse Input
\overline{OE}	3-State Output Enable Input
O ₀ –O ₇	3-State Outputs

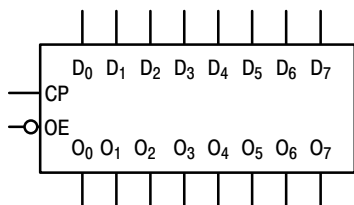
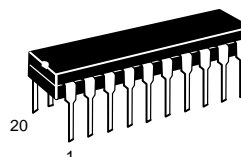


Figure 2. Logic Symbol

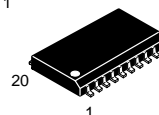


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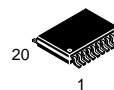
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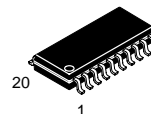
PDIP-20
N SUFFIX
CASE 738



SO-20
DW SUFFIX
CASE 751



TSSOP-20
DT SUFFIX
CASE 948E



EIAJ-20
M SUFFIX
CASE 967

ORDERING INFORMATION

Device	Package	Shipping
MC74AC374N	PDIP-20	18 Units/Rail
MC74ACT374N	PDIP-20	18 Units/Rail
MC74AC374DW	SOIC-20	38 Units/Rail
MC74AC374DWR2	SOIC-20	1000 Tape & Reel
MC74ACT374DW	SOIC-20	38 Units/Rail
MC74ACT374DWR2	SOIC-20	1000 Tape & Reel
MC74AC374DT	TSSOP-20	75 Units/Rail
MC74ACT374DT	TSSOP-20	75 Units/Rail
MC74ACT374DTR2	TSSOP-20	2500 Tape & Reel
MC74AC374M	EIAJ-20	40 Units/Rail
MC74AC374MEL	EIAJ-20	2000 Tape & Reel
MC74ACT374M	EIAJ-20	40 Units/Rail
MC74ACT374MEL	EIAJ-20	2000 Tape & Reel

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 7 of this data sheet.

MC74AC374, MC74ACT374

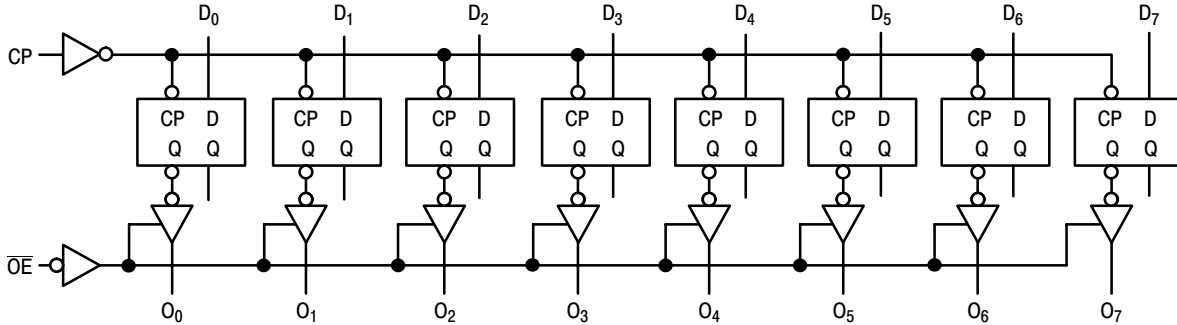
TRUTH TABLE

Inputs			Outputs
D _n	CP	\overline{OE}	O _n
H	┐	L	H
L	┐	L	L
X	X	H	Z

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance
 ┐ = LOW-to-HIGH Transition

FUNCTIONAL DESCRIPTION

The MC74AC374/74ACT374 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-state true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable (\overline{OE}) LOW, the contents of the eight flip-flops are available at the outputs. When the \overline{OE} is HIGH, the outputs go to the high impedance state. Operation of the \overline{OE} input does not affect the state of the flip-flops.



NOTE: That this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 3. Logic Diagram

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{IN}	DC Input Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
V _{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
I _{IN}	DC Input Current, per Pin	±20	mA
I _{OUT}	DC Output Sink/Source Current, per Pin	±50	mA
I _{CC}	DC V _{CC} or GND Current per Output Pin	±50	mA
T _{stg}	Storage Temperature	-65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

MC74AC374, MC74ACT374

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit	
V _{CC}	Supply Voltage	'AC	2.0	5.0	6.0	V
		'ACT	4.5	5.0	5.5	
V _{IN} , V _{OUT}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V _{CC}	V	
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	–	150	–	ns/V
		V _{CC} @ 4.5 V	–	40	–	
		V _{CC} @ 5.5 V	–	25	–	
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	–	10	–	ns/V
		V _{CC} @ 5.5 V	–	8.0	–	
T _J	Junction Temperature (PDIP)	–	–	140	°C	
T _A	Operating Ambient Temperature Range	–40	25	85	°C	
I _{OH}	Output Current – High	–	–	–24	mA	
I _{OL}	Output Current – Low	–	–	24	mA	

- V_{IN} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
- V_{IN} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74ACT		Unit	Conditions	
			T _A = +25°C		T _A = –40°C to +85°C				
			Typ	Guaranteed Limits					
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1		V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V	
		4.5	2.25	3.15	3.15				
		5.5	2.75	3.85	3.85				
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9		V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V	
		4.5	2.25	1.35	1.35				
		5.5	2.75	1.65	1.65				
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9		V	I _{OUT} = –50 μA	
		4.5	4.49	4.4	4.4				
		5.5	5.49	5.4	5.4				
			3.0	–	2.56	2.46		V	*V _{IN} = V _{IL} or V _{IH} –12 mA I _{OH} –24 mA –24 mA
			4.5	–	3.86	3.76			
			5.5	–	4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1		V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1				
		5.5	0.001	0.1	0.1				
			3.0	–	0.36	0.44		V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA
			4.5	–	0.36	0.44			
			5.5	–	0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5	–	±0.1	±1.0		μA	V _I = V _{CC} , GND	
I _{OZ}	Maximum 3-State Current	5.5	–	±0.5	±5.0		μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , GND V _O = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5	–	–	75		mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5	–	–	–75		mA	V _{OHD} = 3.85 V Min	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

NOTE: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

MC74AC374, MC74ACT374

DC CHARACTERISTICS (continued)

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Unit	Conditions
			T _A = +25°C		T _A = -40°C to +85°C			
			Typ	Guaranteed Limits				
I _{CC}	Maximum Quiescent Supply Current	5.5	–	8.0	80		μA	V _{IN} = V _{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

NOTE: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

AC CHARACTERISTICS (For Figures and Waveforms – See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Unit	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Clock Frequency	3.3 5.0	60 100	110 155	– –	60 100	– –	MHz	3–3
t _{PLH}	Propagation Delay CP to O _n	3.3 5.0	3.0 2.5	11 8.0	13.5 9.5	1.5 1.5	15.5 10.5	ns	3–6
t _{PHL}	Propagation Delay CP to O _n	3.3 5.0	2.5 2.0	10 7.0	12.5 9.0	2.0 1.5	14 10	ns	3–6
t _{PZH}	Output Enable Time	3.3 5.0	3.0 2.0	9.5 7.0	11.5 8.5	1.5 1.0	13 9.5	ns	3–7
t _{PZL}	Output Enable Time	3.3 5.0	2.5 2.0	9.0 6.5	11.5 8.5	1.5 1.0	13 9.5	ns	3–8
t _{PHZ}	Output Disable Time	3.3 5.0	3.0 2.0	10.5 8.0	12.5 11	2.0 2.0	14.5 12.5	ns	3–7
t _{PLZ}	Output Disable Time	3.3 5.0	2.0 1.5	8.0 6.5	11.5 8.5	1.0 1.0	12.5 10	ns	3–8

*Voltage Range 3.3 V is 3.3 V ±0.3 V.

Voltage Range 5.0 V is 5.0 V ±0.5 V.

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74AC		74AC		Unit	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Setup Time, HIGH or LOW D _n to CP	3.3 5.0	2.0 1.0	5.5 4.0	6.0 4.5		ns	3–9
t _h	Hold Time, HIGH or LOW D _n to CP	3.3 5.0	-1.0 0	1.0 1.5	1.0 1.5		ns	3–9
t _w	CP Pulse Width HIGH or LOW	3.3 5.0	4.0 2.5	5.5 4.0	6.0 4.5		ns	3–6

*Voltage Range 3.3 V is 3.3 V ±0.3 V.

Voltage Range 5.0 V is 5.0 V ±0.5 V.

MC74AC374, MC74ACT374

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Unit	Conditions
			T _A = +25°C		T _A = -40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V	
		5.5	1.5	2.0	2.0			
V _{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V	
		5.5	1.5	0.8	0.8			
V _{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	V	I _{OUT} = -50 μA	
		5.5	5.49	5.4	5.4			
		4.5	-	3.86	3.76	V	*V _{IN} = V _{IL} or V _{IH} I _{OH} = -24 mA	
		5.5	-	4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	V	I _{OUT} = 50 μA	
		5.5	0.001	0.1	0.1			
		4.5	-	0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} I _{OL} = 24 mA	
		5.5	-	0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5	-	±0.1	±1.0	μA	V _I = V _{CC} , GND	
ΔI _{CC} T	Additional Max. I _{CC} /Input	5.5	0.6	-	1.5	mA	V _I = V _{CC} - 2.1 V	
I _{OZ}	Maximum 3-State Current	5.5	-	±0.5	±5.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , GND V _O = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5	-	-	75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5	-	-	-75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5	-	8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS (For Figures and Waveforms – See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Unit	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Clock Frequency	5.0	100	160	-	90	-	MHz	3-3
t _{PLH}	Propagation Delay CP to O _n	5.0	2.0	8.5	10	2.0	11.5	ns	3-6
t _{PHL}	Propagation Delay CP to O _n	5.0	2.0	8.0	9.5	1.5	11	ns	3-6
t _{PZH}	Output Enable Time	5.0	2.0	8.0	9.5	1.5	10.5	ns	3-7
t _{PZL}	Output Enable Time	5.0	1.5	8.0	9.0	1.5	10.5	ns	3-8
t _{PHZ}	Output Disable Time	5.0	1.5	8.5	11.5	1.0	12.5	ns	3-7
t _{PLZ}	Output Disable Time	5.0	1.5	7.0	8.5	1.0	10	ns	3-8

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

MC74AC374, MC74ACT374

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74ACT		74ACT		Unit	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Setup Time, HIGH or LOW D _n to CP	5.0	1.0	5.0	5.5	ns	3-9	
t _h	Hold Time, HIGH or LOW D _n to CP	5.0	0	1.5	1.5	ns	3-9	
t _w	CP Pulse Width HIGH or LOW	5.0	2.5	5.0	5.0	ns	3-6	

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

CAPACITANCE

Symbol	Parameter	Value Typ	Unit	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	80	pF	V _{CC} = 5.0 V

MC74AC374, MC74ACT374

MARKING DIAGRAMS

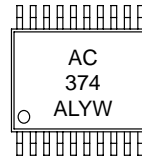
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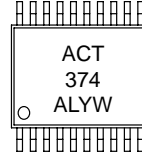
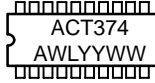
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TSSOP-20



EIAJ-20

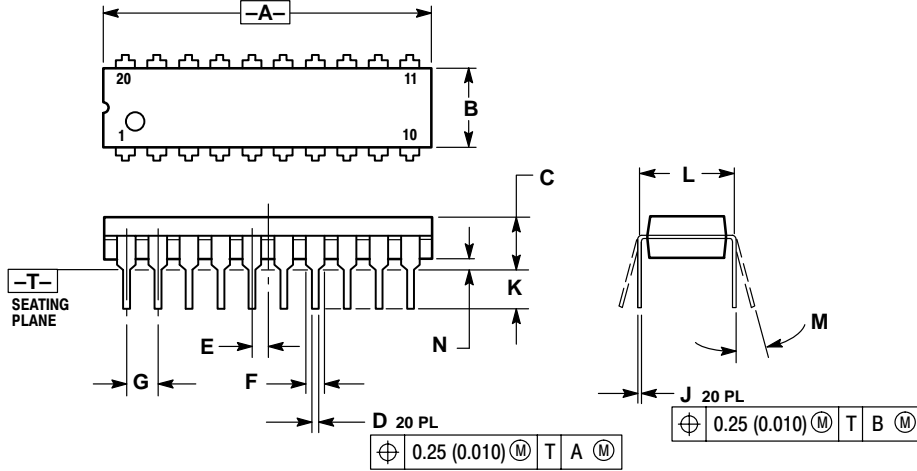


A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

MC74AC374, MC74ACT374

PACKAGE DIMENSIONS

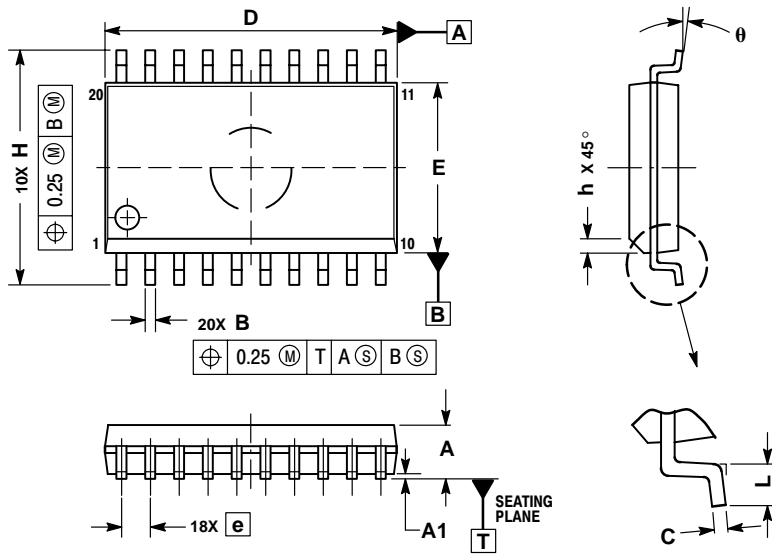
PDIP-20
N SUFFIX
 20 PIN PLASTIC DIP PACKAGE
 CASE 738-03
 ISSUE E



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

SO-20
DW SUFFIX
 20 PIN PLASTIC SOIC PACKAGE
 CASE 751D-05
 ISSUE F



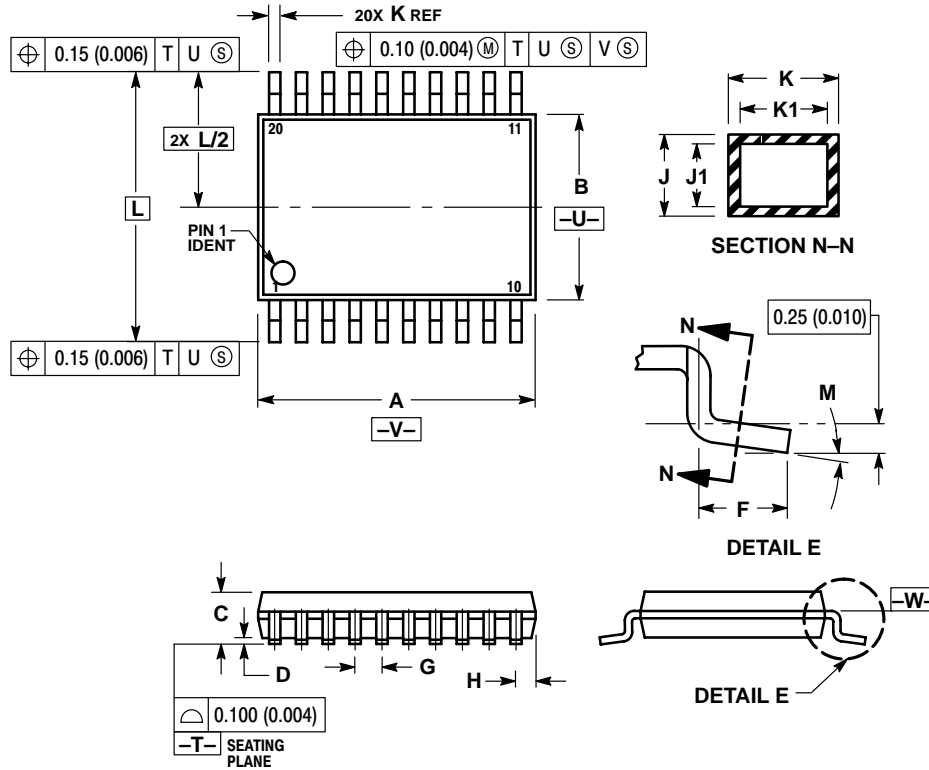
- NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
 3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
 5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

MC74AC374, MC74ACT374

PACKAGE DIMENSIONS

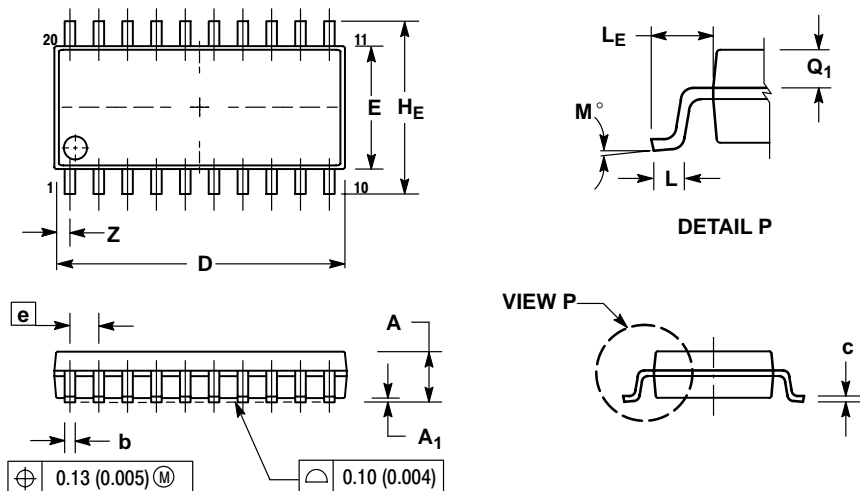
TSSOP-20
DT SUFFIX
 20 PIN PLASTIC TSSOP PACKAGE
 CASE 948E-02
 ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

EIAJ-20
M SUFFIX
 20 PIN PLASTIC EIAJ PACKAGE
 CASE 967-01
 ISSUE O




NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

Notes

Notes

MC74AC374, MC74ACT374

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