

December 1996

Fast CMOS Latched Transceivers

Features

- Advanced 0.8 micron CMOS Technology
- These Devices are Pin Compatible With Bipolar FAST™ Series at a Higher Speed and Lower Power Consumption
- 25Ω Series Resistor on All Outputs (CD74FCT2543T)
- TTL Input and Output Levels
- Low Ground Bounce Outputs
- Extremely Low Static Power
- Hysteresis on All Inputs

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT543ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT543ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT543CTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT543CTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT543DTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT543DTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT543TM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT543TQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT544ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT544ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT544CTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT544CTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT544TM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT544TQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT2543ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT2543ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT2543CTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT2543CTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT2543TM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT2543TQM	-40 to 85	24 Ld QSOP	M24.15-P

NOTE: QSOP is commonly known as SSOP.

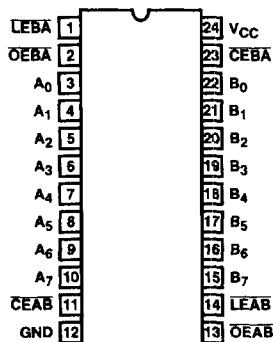
When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Description

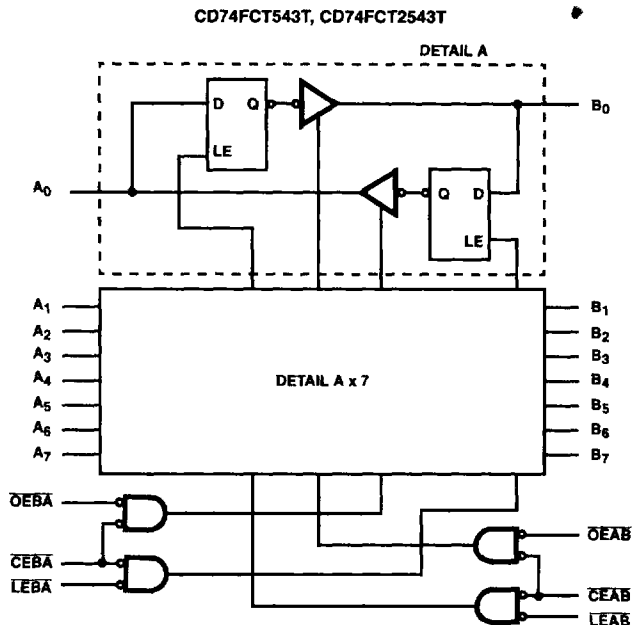
The devices are 8-bit wide non-inverting transceivers designed with two sets of eight D-type latches with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable (\overline{CEAB}) input must be LOW in order to enter data from A_0 - A_7 or to take data from B_0 - B_7 , as indicated in the Truth Table. With \overline{CEAB} LOW, a LOW signal makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the \overline{LEAB} signal puts the A latches in the storage mode and their outputs no longer change the A inputs. With \overline{CEAB} and \overline{OEAB} both LOW, the three-state B output buffers are active and reflect the data present at the output of the A latches. Control of data from B to A is similar, but uses the \overline{CEBA} , \overline{LEBA} , and \overline{OEBA} inputs. The CD74FCT543T is a non-inverting version of the CD74FCT544T.

Pinout

CD74FCT543T, CD74FCT544T, CD74FCT2543T
(QSOP, SOIC)
TOP VIEW



Functional Block Diagram



TRUTH TABLE (NON-INVERTING)
For A-to-B (Symmetric with B-to-A) (NOTES 1, 2)

INPUTS			LATCH STATUS	OUTPUT BUFFERS
CEAB	LEAB	OEAB	A-TO-B	B ₀ -B ₇
H	-	-	Storing	High-Z
-	H	-	Storing	-
-	-	H	-	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous A Inputs (Note 3)

NOTES:

- H = HIGH Voltage Level
L = LOW Voltage Level
- = Don't Care or Irrelevant
- A-to-B data flow shown; B-to-A flow control is the same, except using CEBA, LEBA and OEBA.
- Before LEAB LOW-to-HIGH Transition

Pin Descriptions

PIN NAME	DESCRIPTION
OEAB	A-to-B Output Enable Input (Active LOW)
OEBA	B-to-A Output Enable Input (Active LOW)
CEAB	A-to-B Enable Input (Active LOW)
CEBA	B-to-A Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input (Active LOW)
LEBA	B-to-A Latch Enable Input (Active LOW)
A ₀ -A ₇	A-to-B Data Inputs or B-to-A Three-State Outputs
B ₀ -B ₇	B-to-A Data Inputs or A-to-B Three-State Outputs
GND	Ground
VCC	Power

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OCTAL 5V FCT
5V FCT 25Ω

CD74FCT543T, CD74FCT544T, CD74FCT2543T

Absolute Maximum Ratings

DC Input Voltage	-0.5V to 7.0V
DC Output Current	120mA

Operating Conditions

Operating Temperature Range	-40°C to 85°C
Supply Voltage to Ground Potential	
Inputs and V _{CC} Only	-0.5V to 7.0V
Supply Voltage to Ground Potential	
Outputs and D/O Only	-0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 4)	θ_{JA} (°C/W)
SOIC Package	75
QSOP Package	100
Maximum Junction Temperature	150°C
Maximum Storage Temperature Range	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s)	300°C (Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

4. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 5) TEST CONDITIONS	MIN	(NOTE 6) TYP	MAX	UNITS	
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T _A = -40°C to 85°C, V _{CC} = 5.0V ±5%							
Output HIGH Voltage	V _{OH}	V _{CC} = Min, V _{IN} = V _{IH} or V _{IL}	I _{OH} = -15.0mA	2.4	3.0	-	V
Output LOW Voltage	V _{OL}	V _{CC} = Min, V _{IN} = V _{IH} or V _{IL}	I _{OL} = 64mA	-	0.3	0.50	V
Output LOW Voltage	V _{OL}	V _{CC} = Min, V _{IN} = V _{IH} or V _{IL}	I _{OL} = 12mA (25Ω Only)	-	0.3	0.50	V
Input HIGH Voltage	V _{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V _{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I _{IH}	V _{CC} = Max (Except I/O Pins)	V _{IN} = V _{CC}	-	-	1	μA
Input LOW Current	I _{IL}	V _{CC} = Max (Except I/O Pins)	V _{IN} = GND	-	-	-1	μA
Input HIGH Current	I _{IH}	(I/O Pins Only) V _{CC} = Max	V _{IN} = V _{CC}	-	-	1	μA
Input LOW Current	I _{IL}	(I/O Pins Only) V _{CC} = Max	V _{IN} = GND	-	-	-1	μA
High Impedance Output Current	I _{OZH}	V _{CC} = Max	V _{OUT} = 2.7V			1	μA
	I _{OZL}	V _{CC} = Max	V _{OUT} = 0.5V			-1	μA
Clamp Diode Voltage	V _{IK}	V _{CC} = Min, I _{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I _{OS}	V _{CC} = Max (Note 7), V _{OUT} = GND		-60	-120	-	mA
Power Down Disable	I _{OFF}	V _{CC} = GND, V _{OUT} = 4.5V		-	-	100	μA
Input Hysteresis	V _H			-	200	-	mV
CAPACITANCE T _A = 25°C, f = 1MHz							
Input Capacitance (Note 8)	C _{IN}	V _{IN} = 0V		-	6	10	pF
Output Capacitance (Note 8)	C _{OUT}	V _{OUT} = 0V		-	8	12	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I _{CC}	V _{CC} = Max	V _{IN} = GND or V _{CC}	-	0.1	500	μA
Supply Current per Input at TTL HIGH	ΔI _{CC}	V _{CC} = Max	V _{IN} = 3.4V (Note 9)	-	0.5	2.0	mA

CD74FCT543T, CD74FCT544T, CD74FCT2543T

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 5) TEST CONDITIONS		MIN	(NOTE 6)	MAX	UNITS
					TYP		
Supply Current per Input per MHz (Note 10)	I_{CCD}	$V_{CC} = \text{Max}$, Outputs Open \overline{CEAB} and $\overline{OEAB} = \text{GND}$ $\overline{CEBA} = V_{CC}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	-	0.15	0.25	mA/MHz
Total Power Supply Current (Note 12)	I_C	$V_{CC} = \text{Max}$, Outputs Open $f_{CP} = 10\text{MHz}$ (LEAB) 50% Duty Cycle \overline{CEAB} and $\overline{OEAB} = \text{GND}$ $\overline{CEBA} = V_{CC}$ $f_i = 5\text{MHz}$ One Bit Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	-	1.5	3.5 (Note 11)	mA
			$V_{IN} = 3.4\text{V}$ $V_{IN} = \text{GND}$	-	2.0	5.5 (Note 11)	mA
		$V_{CC} = \text{Max}$, Outputs Open $f_{CP} = 10\text{MHz}$ (LEAB) 50% Duty Cycle \overline{CEAB} and $\overline{OEAB} = \text{GND}$ $\overline{CEBA} = V_{CC}$ Eight Bits Toggling $f_i = 2.5\text{MHz}$, 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	-	3.8	7.3 (Note 11)	mA
			$V_{IN} = 3.4\text{V}$ $V_{IN} = \text{GND}$	-	6.0	16.3 (Note 11)	mA

Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 13) TEST CONDITIONS	T		AT		CT		DT		UNITS
			(NOTE 14) MIN	MAX	(NOTE 14) MIN	MAX	(NOTE 14) MIN	MAX	(NOTE 14) MIN	MAX	
			CD74FCT543T								
Propagation Delay Transparent Mode A_N to B_N or B_N to A_N	t_{PLH} , t_{PHL}	$C_L = 50\text{ pF}$ $R_L = 500\Omega$	2.5	8.5	2.5	6.5	2.5	5.3	2.5	4.4	ns
Propagation Delay \overline{LEBA} to A_N , \overline{LEAB} to B_N	t_{PLH} , t_{PHL}	$C_L = 50\text{ pF}$ $R_L = 500\Omega$	2.5	12.5	2.5	8.0	2.5	7.0	2.5	5.0	ns
Output Enable Time \overline{OEBA} or \overline{OEAB} to A_N or B_N \overline{CEBA} or \overline{CEAB} to A_N or B_N	t_{PZH} , t_{PZL}	$C_L = 50\text{ pF}$ $R_L = 500\Omega$	2.0	12.0	2.0	9.0	2.0	8.0	2.0	5.4	ns
Output Disable Time \overline{OEBA} or \overline{OEAB} to A_N or B_N \overline{CEBA} or \overline{CEAB} to A_N or B_N (Note 15)	t_{PZH} , t_{PZL}	$C_L = 50\text{ pF}$ $R_L = 500\Omega$	2.0	9.0	2.0	7.5	2.0	6.5	2.0	4.3	ns
Setup Time, HIGH or LOW A_N or B_N to \overline{LEBA} or \overline{LEAB}	t_{SU}	$C_L = 50\text{ pF}$ $R_L = 500\Omega$	3.0	-	2.0	-	2.0	-	1.5	-	ns
Hold Time, HIGH or LOW A_N or B_N to \overline{LEBA} or \overline{LEAB}	t_H	$C_L = 50\text{ pF}$ $R_L = 500\Omega$	2.0	-	2.0	-	2.0	-	1.5	-	ns
\overline{LEBA} or \overline{LEAB} Pulse Width LOW (Note 15)	t_W	$C_L = 50\text{ pF}$ $R_L = 500\Omega$	5.0	-	5.0	-	5.0	-	3.0	-	ns
CD74FCT544T, CD74FCT2543T											
Propagation Delay Transparent Mode A_N to B_N or B_N to A_N	t_{PLH} , t_{PHL}	$C_L = 50\text{ pF}$ $R_L = 500\Omega$	2.5	8.5	2.5	6.5	2.5	5.3	-	-	ns
Propagation Delay \overline{LEBA} to A_N , \overline{LEAB} to B_N	t_{PLH} , t_{PHL}	$C_L = 50\text{ pF}$ $R_L = 500\Omega$	2.5	12.5	2.5	8.0	2.5	7.0	-	-	ns

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**OCTAL 5V FCT
5V FCT 25Ω**

CD74FCT543T, CD74FCT544T, CD74FCT2543T

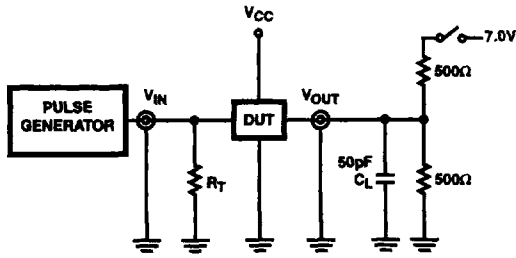
Switching Specifications Over Operating Range (Continued)

PARAMETER	SYM-BOL	(NOTE 13) TEST CONDITIONS	T		AT		CT		DT		UNITS
			(NOTE 14) MIN	MAX	(NOTE 14) MIN	MAX	(NOTE 14) MIN	MAX	(NOTE 14) MIN	MAX	
Output Enable Time OEBA or OEAB to An or Bn CEBA or CEAB to AN or BN	t _{PZH} , t _{PZL}	C _L = 50 pF R _L = 500Ω	2.0	12.0	2.0	9.0	2.0	8.0	-	-	ns
Output Disable Time OEBA or OEAB to AN or BN CEBA or CEAB to AN or BN (Note 15)	t _{PZH} , t _{PZL}	C _L = 50 pF R _L = 500Ω	2.0	9.0	2.0	7.5	2.0	6.5	-	-	ns
Setup Time, HIGH or LOW An or Bn to LEBA or LEAB	t _{SU}	C _L = 50 pF R _L = 500Ω	3.0	-	2.0	-	2.0	-	-	-	ns
Hold Time, HIGH or LOW An or Bn to LEBA or LEAB	t _H	C _L = 50 pF R _L = 500Ω	2.0	-	2.0	-	2.0	-	-	-	ns
LEBA or LEAB Pulse Width LOW (Note 15)	t _W	C _L = 50 pF R _L = 500Ω	5.0	-	5.0	-	5.0	-	-	-	ns

NOTES:

5. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
6. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
7. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
8. This parameter is determined by device characterization but is not production tested.
9. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
10. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
12. I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
 I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 f_I = Input Frequency
 N_I = Number of Inputs at f_I
 All currents are in milliamps and all frequencies are in megahertz.
13. See test circuit and wave forms.
14. Minimum limits are guaranteed but not tested on Propagation Delays.
15. This parameter is guaranteed but not production tested.

Test Circuits and Waveforms



SWITCH POSITION	
TEST	SWITCH
t_{PLZ} , t_{PZL}	Closed
t_{PHZ} , t_{PZH} , t_{PLH} , t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.
 R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

16. Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $Z_{OUT} \leq 50\Omega$;
 $t_r, t_f \leq 2.5\text{ns}$.

FIGURE 1. TEST CIRCUIT

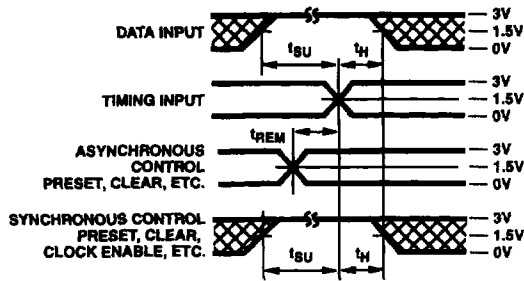


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

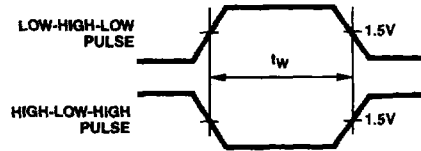


FIGURE 3. PULSE WIDTH

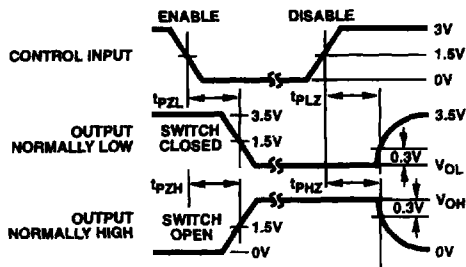


FIGURE 4. ENABLE AND DISABLE TIMING

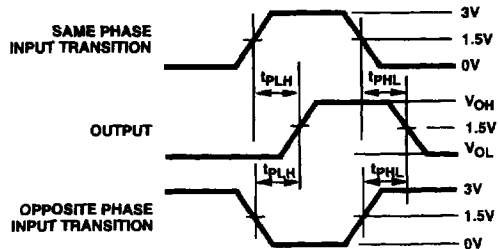


FIGURE 5. PROPAGATION DELAY