NLAS4717

Analog Switch, High Bandwidth, Dual SPDT

The NLAS4717 is an advanced CMOS analog switch fabricated in sub-micron silicon gate CMOS technology. The device is a dual independent Single Pole Double Throw (SPDT) switch featuring two low $R_{DS(on)}$ of 4.5 Ω at 3.0 V.

The device also features guaranteed Break-Before-Make (BBM) switching, assuring the switches never short the driver.

The NLAS4717 is available in two small size packages:
- ♦ Micro10:   3.0 x 5.0 mm
- ♦ Flip-Chip-10:   2.0 x 1.5 mm

Features

- Low $R_{DS(on)}$: 4.5 Ω @ 3.0 V
- Matching Between the Switches ±0.5 Ω
- Wide Low Voltage Range: 1.8 V to 5.5 V
- High Bandwidth > 40 MHz
- 1.65 V to 5.5 V Operating Range
- Low Threshold Voltages on Pins 4 and 8 (CTRL Pins)
- Ultra-Low Charge Injection ≤ 6.0 pC
- Low Standby Current – I_{CC} = 1.0 nA (Max) @ T_A = 25°C
- OVT* on Pins 4 and 8 (CTRL Logic Pins)
- Pb-Free Packages are Available

Typical Applications

- Cell Phones
- PDAs
- MP3s
- Digital Still Cameras

Important Information

- ESD Protection:
      HBM = 2000 V, MM = 200 V
- Latchup Max Rating: 200 mA (Per JEDEC EIA/JESD78)
- Pin-to-Pin Compatible with MAX4717

*OVT

- Overvoltage Tolerance (OVT) specific pins to operate higher than normal supply voltages, with no damage to the devices or to signal integrity.
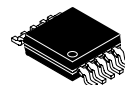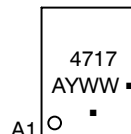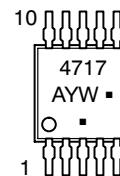
ON Semiconductor®

http://onsemi.com

FUNCTION TABLE

IN_	NO_	NC_
0	OFF	ON
1	ON	OFF

ORDERING INFORMATION

Device	Package	Shipping†
NLAS4717FCT1	Flip-Chip-10	3000 / Tape & Reel
NLAS4717FCT1G	Flip-Chip-10 (Pb-Free)	3000 / Tape & Reel
NLAS4717MR2	Micro10	4000 / Tape & Reel
NLAS4717MR2G	Micro10 (Pb-Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
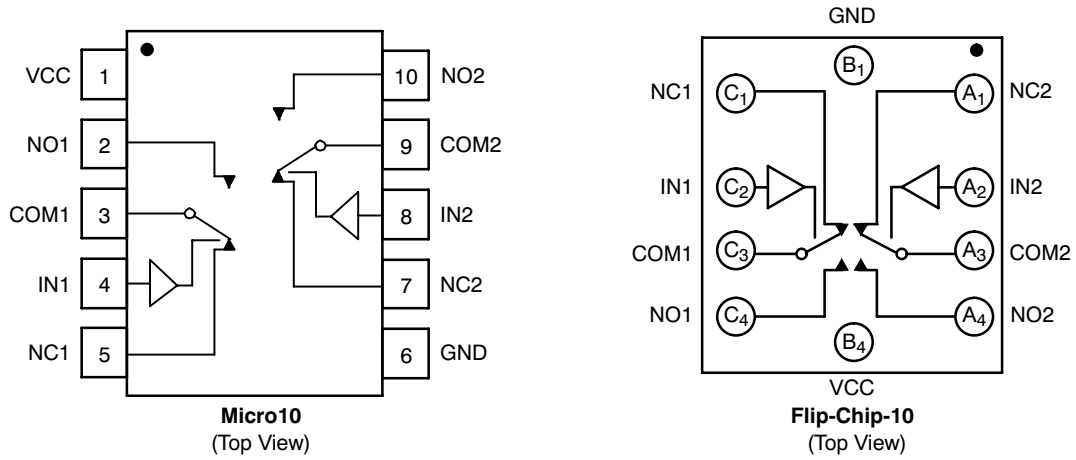
NLAS4717

Figure 1. Device Circuit Diagrams and Pin Configurations

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V+	Positive DC Supply Voltage	-0.5 to $+7.0$	V
V_{IS}	Analog Input Voltage (V_{NO}, V_{NC}, or V_{COM}) (Note 1)	$-0.5 \leq V_{IS} \leq V_{CC} +0.5$	V
V_{IN}	Digital Select Input Voltage	$-0.5 \leq V_I \leq +7.0$	V
I_{IK}	DC Current, Into or Out of Any Pin (Continuous)	± 100	mA
I_{PK}	Peak Current (10% Duty Cycle)	± 200	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.
1. Signal voltage on NC, NO, and COM exceeding VCC or GND are clamped by the internal diodes. Limit forward diode current to maximum current rating.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V+	DC Supply Voltage		1.8	5.5	V
V_{IN}	Digital Select Input Voltage		GND	5.5	V
V_{IS}	Analog Input Voltage (NC, NO, COM)		GND	V_{CC}	V
T_A	Operating Temperature Range		-40	+85	°C
t_r, t_f	Input Rise or Fall Time, SELECT	$V_{CC} = 3.3\ V \pm 0.3\ V$ $V_{CC} = 5.0\ V \pm 0.5\ V$	0 0	100 20	ns/V

ANALOG SWITCH DC CHARACTERISTICS

Symbol	Parameter	Condition	V_{CC} (V)	-40 °C to +85°C Min	Max	Unit
V_{IH}	Input Logic High Voltage	$V_{OUT} = 0.1\ V$ $I_{OUT} \leq 20\ \mu A$	1.65 to 2.2 2.7 to 3.6 4.5 to 5.5	V_{CC} x 0.55 V_{CC} x 0.5 2.0	- - -	V
V_{IL}	Input Logic Low Voltage	$V_{OUT} = -V_{CC} - 0.1\ V$ $I_{OUT} \leq 20\ \mu A$	1.65 to 2.2 2.7 to 3.6 4.5 to 5.5	- - -	V_{CC} x 0.2 V_{CC} x 0.2 0.8	V
I_{IN}	Input Leakage Current	$V_{IN} - V_{CC}$ or GND	5.0	-100	+100	nA
V_{CC}	Power Supply Range	All	-	1.65	5.5	V
I_{CC}	Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0\ \mu A$	1.8 3.3 5.0	- - -	1.0 1.0 1.0	μA
V_{IS}	Analog Signal Range	Key parameter	-	0	V_{CC}	V

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ANALOG SWITCH CHARACTERISTICS - Digital Section (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_{CC} (V)	-40 °C to +85°C			Unit
				Min	Typ	Max	
R_{ON}	ON Resistance (Note 2)	V_{CC} = 3.0 V I_{COM} = 10 mA V_{NO} or V_{NC} = V_{IH} or V_{IL}	3.0	-		4.5	Ω
		V_{CC} = 5.0 V I_{COM} = 10 mA V_{NO} or V_{NC} = V_{IH} or V_{IL}	5.0	-		3.5	
ΔR_{ON}	ON Resistance Match Between Channels (Note 2 and 3)	V_{CC} = 3.6 V I_{COM} = 10 mA V_{NO} or V_{NC} = V_{IH} or V_{IL}	3.6	-	0.1	0.4	Ω
		V_{CC} = 5.5 V I_{COM} = 10 mA V_{NO} or V_{NC} = V_{IH} or V_{IL}	5.5				
$R_{FLAT[ON]}$	ON Resistance Flatness (Note 4)	I_{COM} = 10 mA V_{IS} = 0 to V_{CC}	3.0	-		1.5	Ω
		I_{COM} = 10 mA V_{IS} = 0 to V_{CC}	5.5	-		1.36	
$I_{NO\_[OFF]}$ $I_{NC\_[OFF]}$	NO_, NC_ Off-Leakage Current (Note 5)	V_{CC} = 3.6 V V_{COM} = 0.3 V or 3.3 V V_{NO} or V_{NC} = 0.3 V or 3.3 V	3.6	-1.0	0.01	+1.0	nA
		V_{CC} = 5.5 V V_{COM} = 0 V or 5.0 V V_{NO} or V_{NC} = 0 V or 5.0 V	5.5	-1.0	0.01	+1.0	
$I_{COM\_[ON]}$	COM_ On-Leakage Current (Note 5)	V_{CC} = 3.6 V V_{COM} = 0.3 V or 3.3 V V_{NO} or V_{NC} = 0.3 V or 3.3 V	3.6	-2.0	0.01	+2.0	nA
		V_{CC} = 5.5 V V_{COM} = 0 V or 5.0 V V_{NO} or V_{NC} = 0 V or 5.0 V	5.5	-2.0	0.01	+2.0	

ANALOG SWITCH AC CHARACTERISTICS

Symbol	Parameter	Condition	V_{CC} (V)	-40 °C to +85°C			Unit
				Min	Typ	Max	
t_{ON}	Turn-On Time	$V_{NC\_}$, $V_{NO\_}$ = V_{IH} or V_{IL} R_L = 300 Ω, C_L = 35 pF $V_{IN[x]}$ = V_{IH} or V_{IL}	1.8 to 5.5	-	-	30	nS
t_{OFF}	Turn-Off Time	$V_{NC\_}$, $V_{NO\_}$ = V_{IH} or V_{IL} R_L = 300 Ω, C_L = 35 pF $V_{IN[x]}$ = V_{IH} or V_{IL}	1.8 to 5.5	-	-	40	nS
t_{BBM}	Break-Before-Make Time Delay (Note 5)	$V_{NC\_}$, $V_{NO\_}$ = 1.5 V R_L = 300 Ω, C_L = 35 pF	-	-	8.0	-	nS
t_{SKEW}	Skew (Note 5)	R_S = 39 Ω, C_L = 50 pF	-	-	0.15	2.0	nS

2. R_{ON} characterized for V_{CC} range (1.65 V to 5.5 V).
3. ΔR_{ON} = R_{ON}(MAX) - R_{ON}(MIN).
4. $R_{FLAT[ON]}$ = R_{ON}(MAX) - R_{ON}(MIN), measured over V_{CC} range.
5. Guaranteed by design.

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ANALOG SWITCH APPLICATION CHARACTERISTICS

Symbol	Parameter	Condition	V_{CC} (V)	-40 °C to +85°C			Unit
				Min	**Typ**	**Max**	
Q	Charge Injection	$V_{IN} = V_{CC}$ to GND $R_{In} = 0\ \Omega$, $C_L = 1.0$ nF $Q = C_L - \Delta V_{OUT}$	3.0 5.0		6.0 9.0		pC
VISO	Off-Isolation	f = 10 MHz $V_{NO\_}$, $V_{NC\_} = 1.0$ Vp-p $R_L = 50\ \Omega$, $C_L = 5.0$ pF	1.65 to 5.5		-50		dB
		f = 1.0 MHz $V_{NO\_}$, $V_{NC\_} = 1.0$ Vp-p $R_L = 50\ \Omega$, $C_L = 5.0$ pF			-75		
VCT	Cross-Talk	f = 10 MHz $V_{NO\_}$, $V_{NC\_} = 1.0$ Vp-p $R_L = 50\ \Omega$, $C_L = 5.0$ pF	1.65 to 5.5		-80		dB
		f = 1.0 MHz $V_{NO\_}$, $V_{NC\_} = 1.0$ Vp-p $R_L = 50\ \Omega$, $C_L = 5.0$ pF			-110		
BW	On-Channel -3.0 db Bandwidth	Signal = 0 dB $R_L = 50\ \Omega$, $C_L = 5.0$ pF	1.8 to 5.0		40		MHz
THD	Total Harmonic Distortion	$V_{COM} = 2.0$ Vp-p, RL = 600 Ω, $T_A = 25°C$	-		0.02		%
$C_{NO\_[OFF]}$ $C_{NC\_[OFF]}$	NO_, NC_ OFF-Capacitance	F = 10 MHz	-		30		pF
$C_{NO\_[ON]}$ $C_{NC\_[ON]}$	NO_, NC_ ON-Capacitance	F = 10 MHz	-		110		pF

NLAS4717
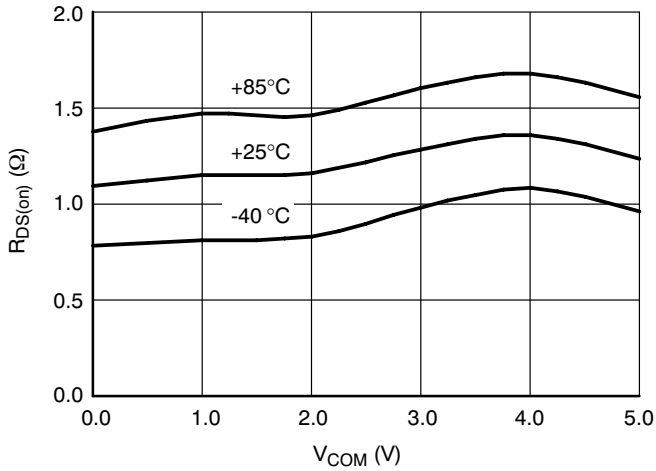
Figure 2. Low R$_{DS(on)}$ @ V$_{CC}$ = 5.0 V
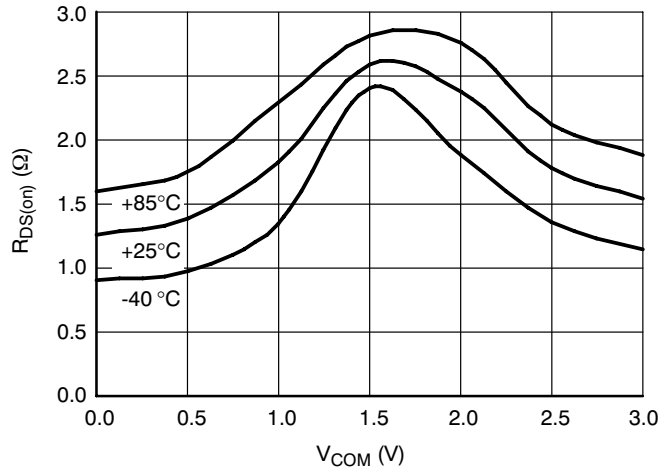
Figure 3. Low R$_{DS(on)}$ @ V$_{CC}$ = 3.0 V
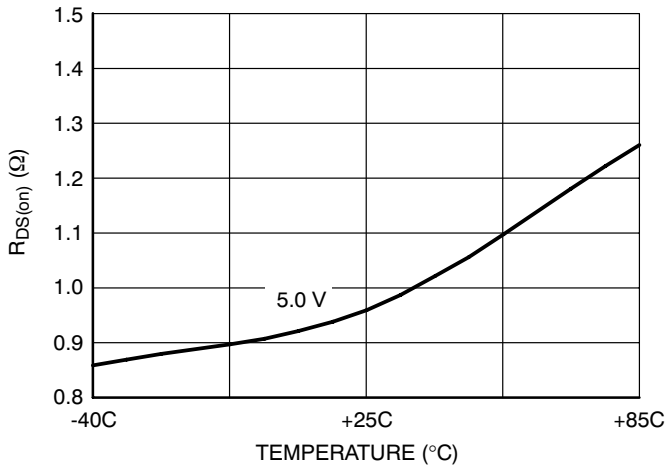
Figure 4. Delta R$_{DS(on)}$ @ V$_{CC}$ = 5.0 V
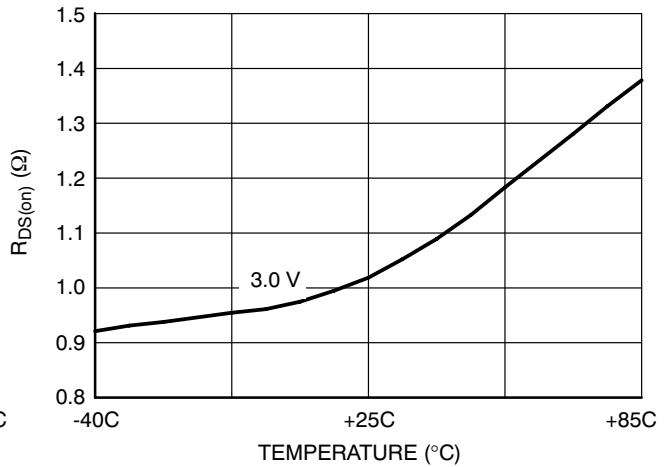
Figure 5. Delta R$_{DS(on)}$ @ V$_{CC}$ = 3.0 V
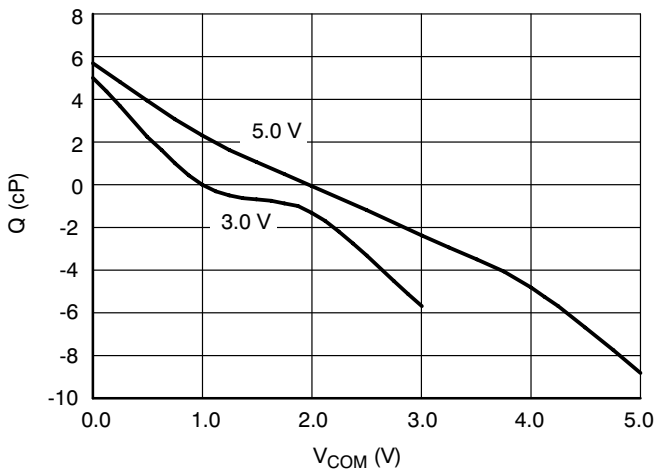
Figure 6. Charge Injection
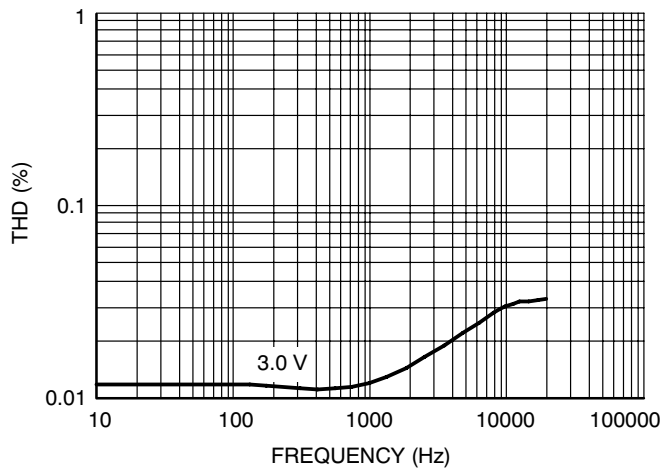
Figure 7. Total Harmonic Distortion
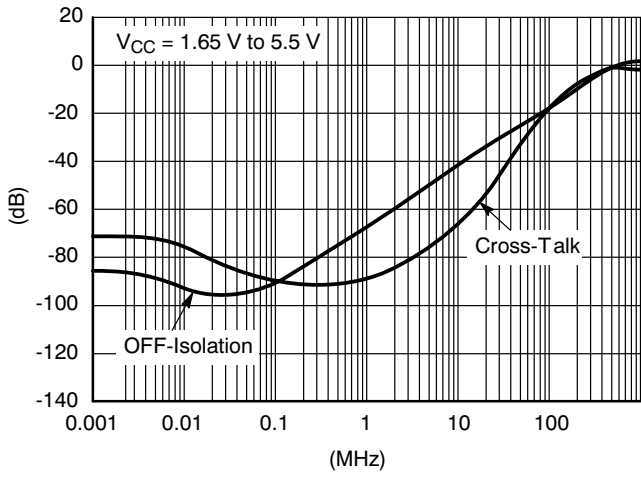
Figure 8. Frequency Response
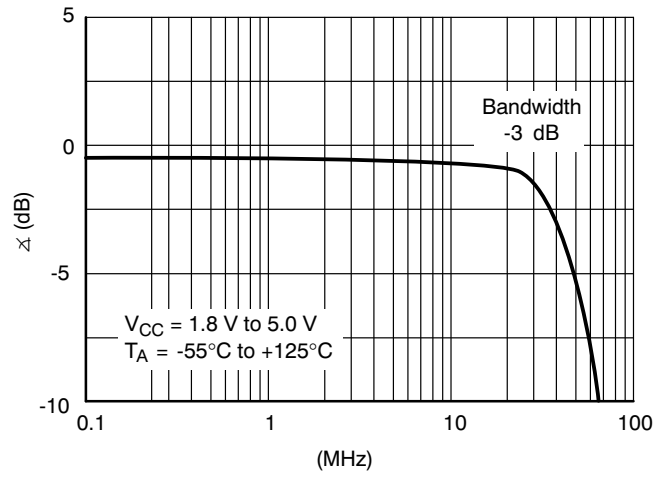
Figure 9. Bandwidth and Phase
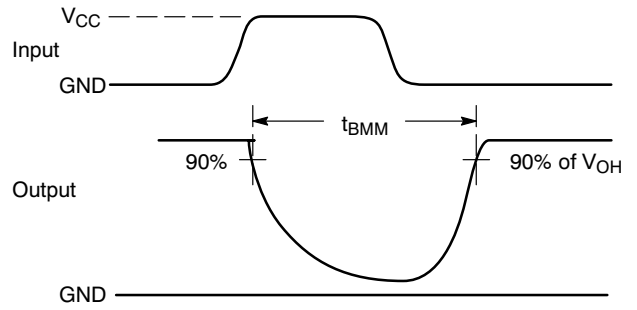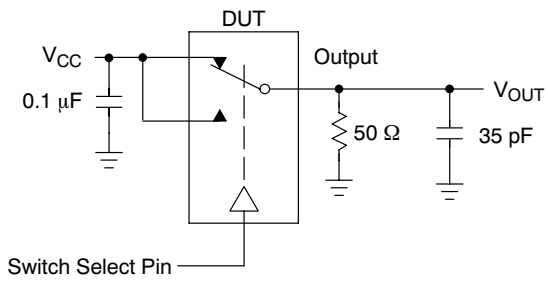
Figure 10. t_{BBM} (Time Break-Before-Make)
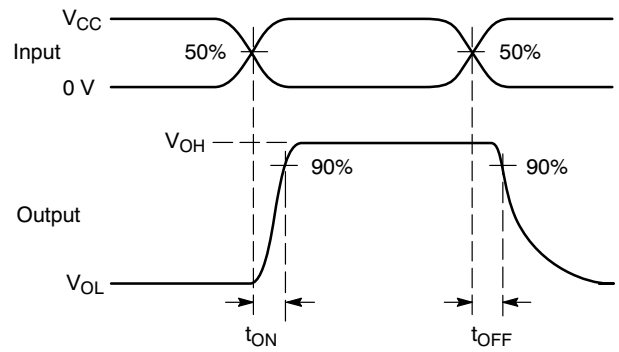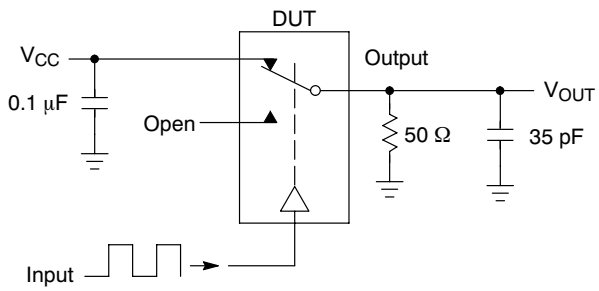
Figure 11. t_{ON}/t_{OFF}
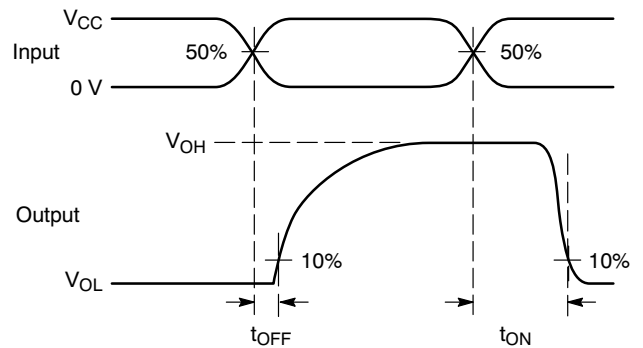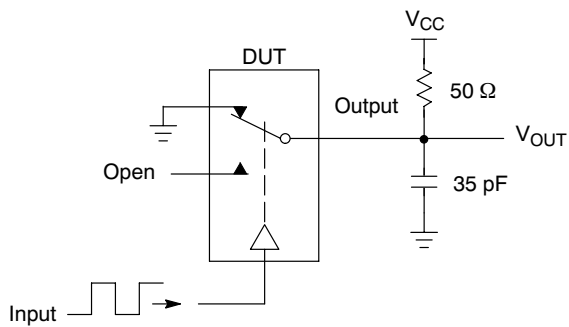
Figure 12. t_{ON}/t_{OFF}
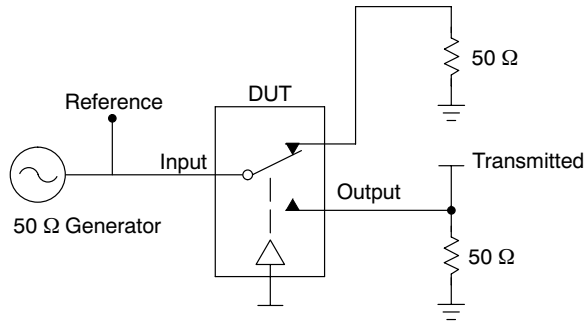
Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch. V_{ISO}, Bandwidth and V_{ONL} are independent of the input signal direction.

$$V_{ISO} = \text{Off Channel Isolation} = 20 \, \text{Log}\left(\frac{V_{OUT}}{V_{IN}}\right) \text{ for } V_{IN} \text{ at 100 kHz}$$

$$V_{ONL} = \text{On Channel Loss} = 20 \, \text{Log}\left(\frac{V_{OUT}}{V_{IN}}\right) \text{ for } V_{IN} \text{ at 100 kHz to 50 MHz}$$

Bandwidth (BW) = the frequency 3.0 dB below V_{ONL}
V_{CT} = Use V_{ISO} setup and test to all other switch analog input/outputs terminated with 50 Ω

**Figure 13. Off Channel Isolation/On Channel Loss (BW)/Crosstalk
(On Channel to Off Channel)/V_{ONL}**
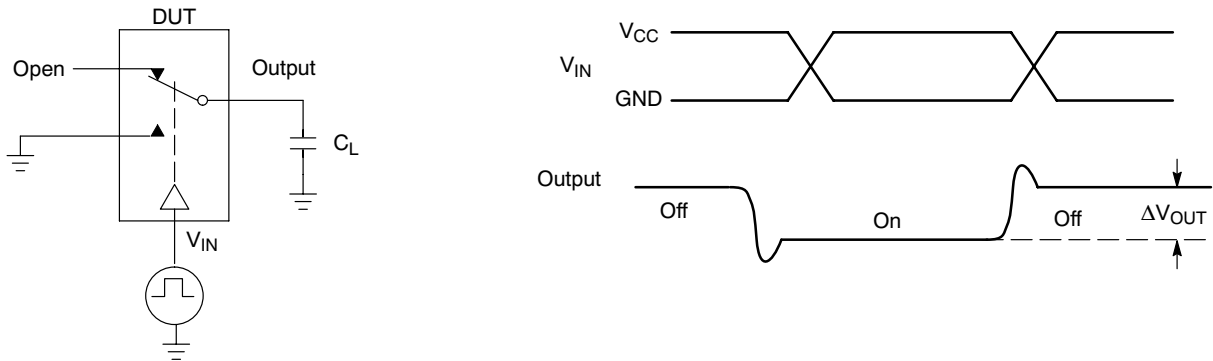
Figure 14. Charge Injection: (Q)

10 PIN FLIP−CHIP
CASE 489AA−01
ISSUE A

DATE 04 MAY 2004
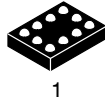
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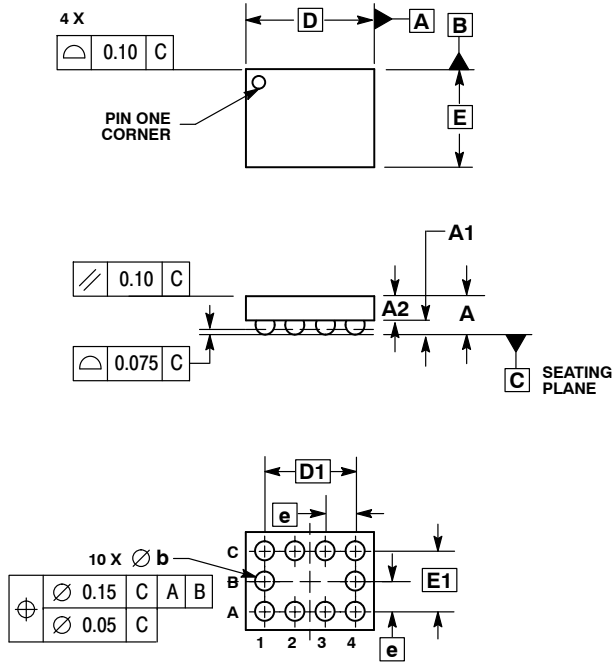
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

4 X

| ☐ | 0.10 | C |

PIN ONE CORNER

| // | 0.10 | C |

| ☐ | 0.075 | C |

A1

A2   A

SEATING PLANE

D1

e

10 X ⌀ b

| ⊕ | ⌀ 0.15 | C | A | B |
| | ⌀ 0.05 | C | | |

C
B
A

1 2 3 4

e

DIM	MILLIMETERS	
	MIN	MAX
A	−−−	0.650
A1	0.210	0.270
A2	0.280	0.380
D	1.965 BSC	
E	1.465 BSC	
b	0.250	0.350
e	0.500 BSC	
D1	1.500 BSC	
E1	1.000 BSC	

GENERIC MARKING DIAGRAM*

xxxx
YYWW

A1
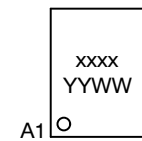
xxxx = Specific Device Code
YY = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪ ", may or may not be present.

| DOCUMENT NUMBER: | 98AON12946D | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. | |
| DESCRIPTION: | 10 PIN FLIP−CHIP | | PAGE 1 OF 1 |

Micro10
CASE 846B–03
ISSUE D

DATE 07 DEC 2004

SCALE 2:1

–A–

K

–B–

PIN 1 ID

G

D 8 PL

⊕ | 0.08 (0.003) Ⓜ | T | B Ⓢ | A Ⓢ

△ | 0.038 (0.0015)
–T– SEATING PLANE

C

H

J

L
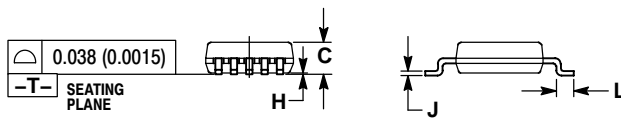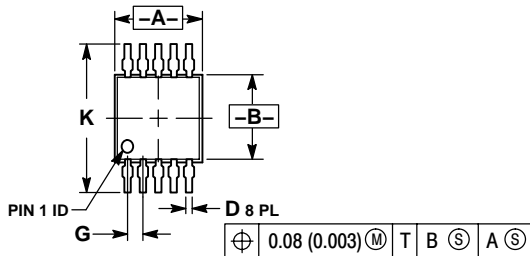
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION "A" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION "B" DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. 846B–01 OBSOLETE. NEW STANDARD 846B–02

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.95	1.10	0.037	0.043
D	0.20	0.30	0.008	0.012
G	0.50 BSC		0.020 BSC	
H	0.05	0.15	0.002	0.006
J	0.10	0.21	0.004	0.008
K	4.75	5.05	0.187	0.199
L	0.40	0.70	0.016	0.028

GENERIC MARKING DIAGRAM*

XXXX
AYW

xxxx	= Device Code
A	= Assembly Location
Y	= Year
W	= Work Week
▪	= Pb–Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, "G" or microdot " ▪ ", may or may not be present.

SOLDERING FOOTPRINT

10X 1.04 / 0.041

0.32 / 0.0126 **10X**

3.20 / 0.126

4.24 / 0.167

5.28 / 0.208

8X 0.50 / 0.0196

SCALE 8:1   (mm / inches)
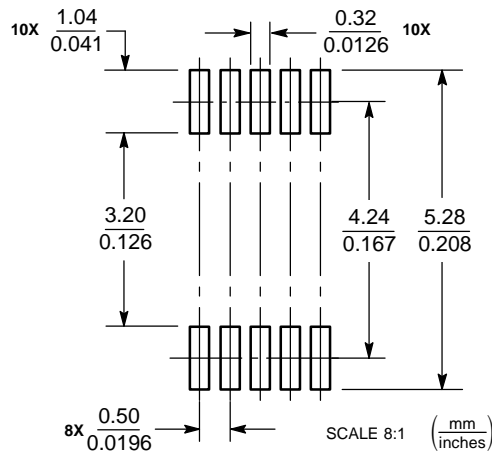
Micro10

DOCUMENT NUMBER:	**98AON03799D**
STATUS:	**ON SEMICONDUCTOR STANDARD**
NEW STANDARD:	
DESCRIPTION:	**Micro10**

ISSUE	REVISION	DATE
O	RELEASED FOR PRODUCTION. REQ BY J. HOSKINS.	09 NOV 2000
A	DIM "D" WAS 0.25–0.4MM/0.10–0.016IN. ADDED NOTE 5. USED ON: WAS 10 LEAD TSSOP, PITCH 0.65 REQ BY J. HOSKINS.	13 NOV 2000
B	CHANGED "USED ON" WAS: 10 LEAD TSSOP, PITCH 0.50MM. REQ BY A. HAMID.	11 JUL 2001
C	CHANGED "D" DIMENSION MAX FROM 0.35 TO 0.30MM AND 0.014 TO 0.012IN. REQ BY D. TRUHITTE.	31 JUL 2003
D	ADDED FOOTPRINT INFORMATION. REQ. BY K. OPPEN.	07 DEC 2004

PUBLICATION ORDERING INFORMATION

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