

# 74AHC273-Q100; 74AHCT273-Q100

Octal D-type flip-flop with reset; positive-edge trigger

Rev. 2 — 23 September 2020

Product data sheet

## 1. General description

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The 74AHC273-Q100; 74AHCT273-Q100 is a high-speed Si-gate CMOS device and is pin compatible with Low-power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard No. 7-A.

The 74AHC273-Q100; 74AHCT273-Q100 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common clock (CP) and master reset ( $\overline{MR}$ ) inputs, load and reset (clear) all flip-flops simultaneously. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding output (Qn) of the flip-flop. All outputs will be forced LOW, independent of clock or data inputs, by a LOW on the  $\overline{MR}$  input.

The device is useful for applications where only the true output is required and the clock and master reset are common to all storage elements.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

## 2. Features

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- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Balanced propagation delays
- All inputs have Schmitt-trigger actions
- Inputs accept voltages higher than  $V_{CC}$
- Ideal buffer for MOS microcontroller or memory
- Common clock and master reset
- Input levels:
  - For 74AHC273-Q100: CMOS level
  - For 74AHCT273-Q100: TTL level
- ESD protection:
  - MIL-STD-883, method 3015 exceeds 2000 V
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V (C = 200 pf, R = 0  $\Omega$ )
- DHVQFN package with Side-Wettable Flanks enabling Automatic Optical Inspection (AOI) of solder joints

### 3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AHC273D-Q100	-40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74AHCT273D-Q100				
74AHC273PW-Q100	-40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74AHCT273PW-Q100				
74AHC273BQ-Q100	-40 °C to +125 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1
74AHCT273BQ-Q100				

### 4. Functional diagram

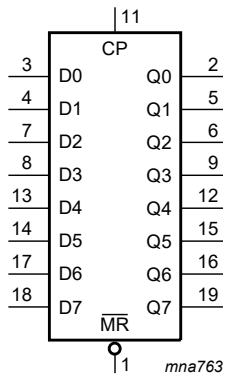


Fig. 1. Logic symbol

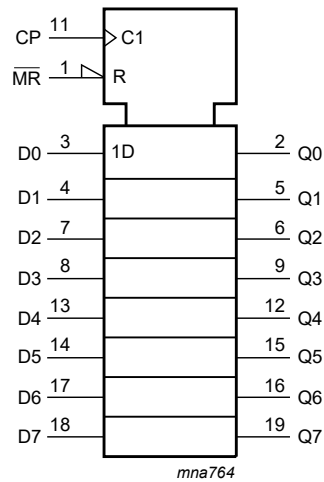


Fig. 2. IEC logic symbol

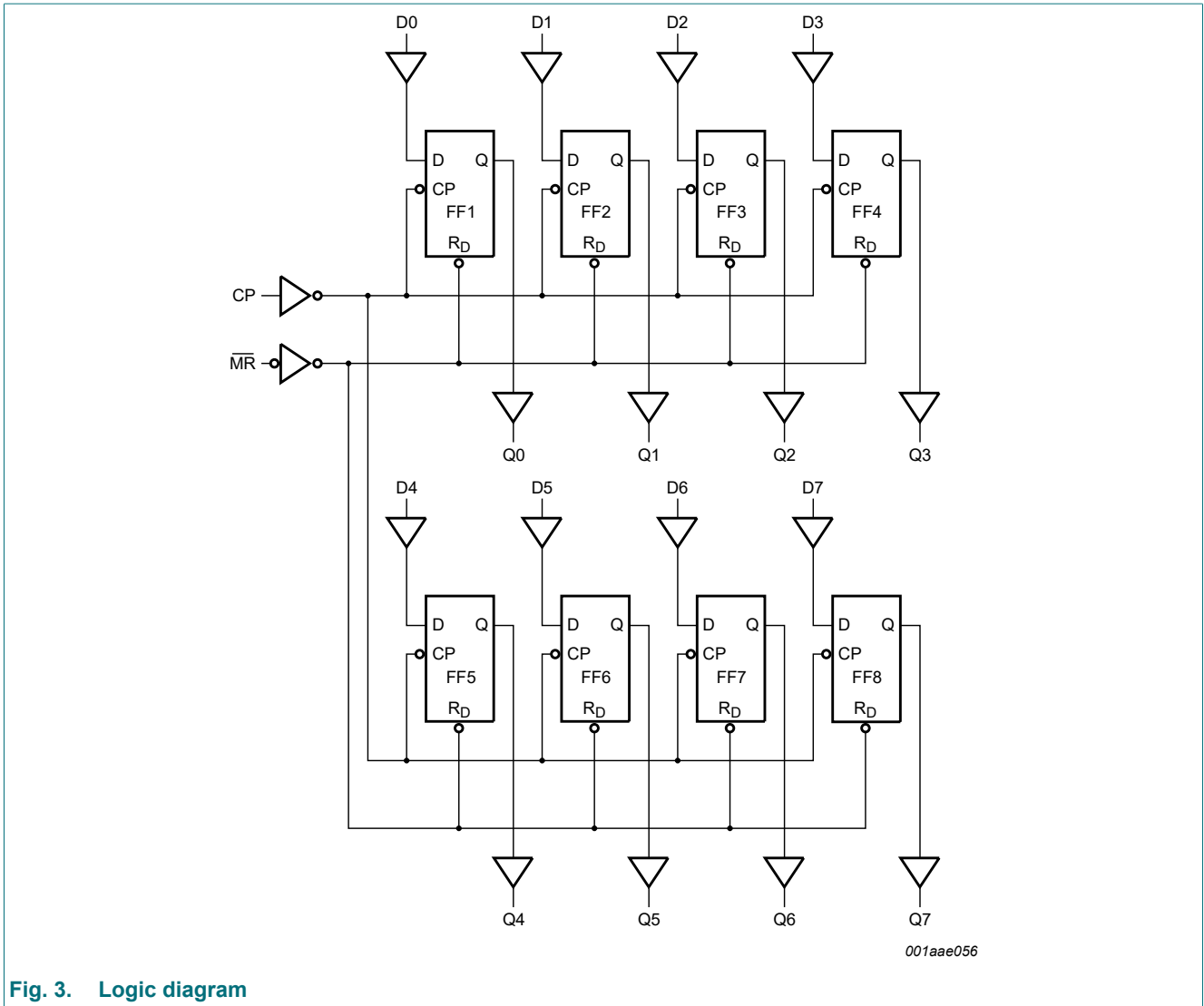


Fig. 3. Logic diagram

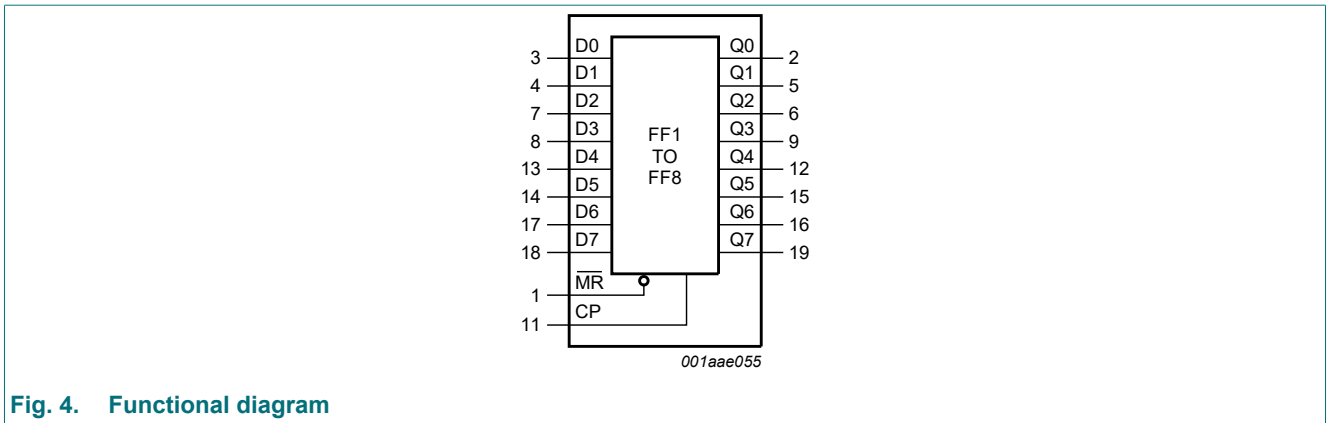
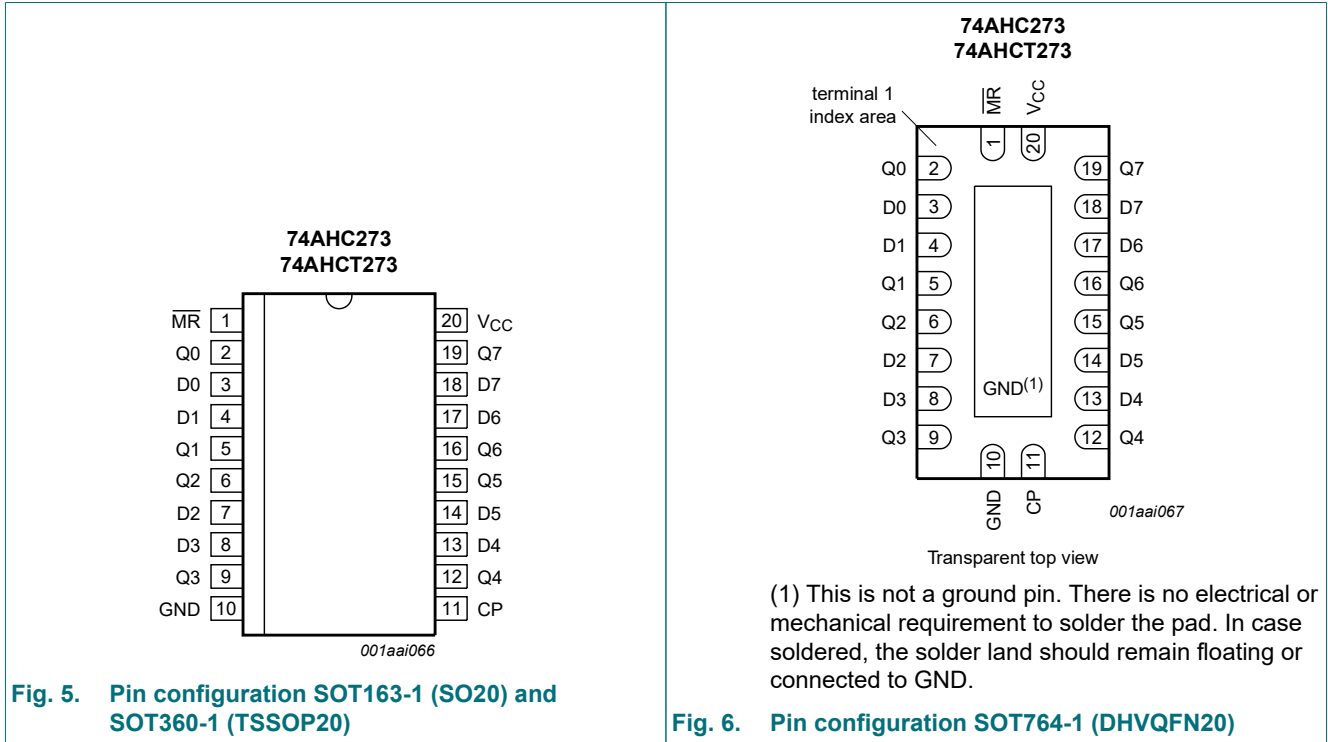


Fig. 4. Functional diagram

## 5. Pinning information

### 5.1. Pinning



### 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
MR	1	master reset input (active LOW)
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	2, 5, 6, 9, 12, 15, 16, 19	flip-flop output
D0, D1, D2, D3, D4, D5, D6, D7	3, 4, 7, 8, 13, 14, 17, 18	data input
GND	10	ground (0 V)
CP	11	clock input (LOW-to-HIGH edge-triggered)
VCC	20	supply voltage

## 6. Functional description

**Table 3. Function table**

*H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition;  
L = LOW voltage level; l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition;  
↑ = LOW-to-HIGH; X = don't care.*

Operating mode	Control		Input	Output
	MR	CP	Dn	Qn
Reset (clear)	L	X	X	L
Load '1'	H	↑	h	H
Load '0'	H	↑	l	L

## 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$V_I$	input voltage		-0.5	+7.0	V
$I_{IK}$	input clamping current	$V_I < -0.5\text{ V}$ [1]	-20	-	mA
$I_{OK}$	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$ [1]	-20	+20	mA
$I_O$	output current	$V_O = -0.5\text{ V}$ to $(V_{CC} + 0.5\text{ V})$	-25	+25	mA
$I_{CC}$	supply current		-	+75	mA
$I_{GND}$	ground current		-75	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$ [2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT163-1 (SO20) package:  $P_{tot}$  derates linearly with 12.3 mW/K above 109 °C.  
For SOT360-1 (TSSOP20) package:  $P_{tot}$  derates linearly with 10.0 mW/K above 100 °C.  
For SOT764-1 (DHVQFN20) package:  $P_{tot}$  derates linearly with 12.9 mW/K above 111 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

*Voltages are referenced to GND (ground = 0 V).*

Symbol	Parameter	Conditions	74AHC273-Q100			74AHCT273-Q100			Unit
			Min	Typ	Max	Min	Typ	Max	
$V_{CC}$	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
$V_I$	input voltage		0	-	5.5	0	-	5.5	V
$V_O$	output voltage		0	-	$V_{CC}$	0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	-	-	100	-	-	-	ns/V
		$V_{CC} = 5.0\text{ V} \pm 0.5\text{ V}$	-	-	20	-	-	20	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74AHC273-Q100</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
		V <sub>CC</sub> = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V <sub>CC</sub> = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
		V <sub>CC</sub> = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V <sub>CC</sub> = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = -50 µA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I <sub>O</sub> = -50 µA; V <sub>CC</sub> = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I <sub>O</sub> = -50 µA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 3.0 V	2.58	-	-	2.48	-	2.40	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = 50 µA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 50 µA; V <sub>CC</sub> = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 50 µA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	µA
		V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	4.0	-	40	-	80	µA
C <sub>I</sub>	input capacitance		-	3	10	-	10	-	10	pF
C <sub>O</sub>	output capacitance		-	4	-	-	-	-	-	pF

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74AHCT273-Q100</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = -50 µA	4.4	-	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -8.0 mA	3.94	-	-	3.80	-	3.70	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = 50 µA	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 8.0 mA	-	-	0.36	-	0.44	-	0.55	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	µA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	4.0	-	40	-	80	µA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>I</sub> = V <sub>CC</sub> - 2.1 V; other pins at V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
C <sub>I</sub>	input capacitance		-	3	10	-	10	-	10	pF
C <sub>O</sub>	output capacitance		-	4	-	-	-	-	-	pF

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 10.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
<b>74AHC273-Q100</b>										
t <sub>pd</sub>	propagation delay	CP to Qn; see Fig. 7 [2]								
		V <sub>CC</sub> = 3.0 V to 3.6 V								
		C <sub>L</sub> = 15 pF	-	6.0	13.6	1.0	16.0	1.0	17.0	ns
		C <sub>L</sub> = 50 pF	-	8.6	17.1	1.0	19.5	1.0	21.5	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V								
		C <sub>L</sub> = 15 pF	-	4.2	9	1.0	10.5	1.0	11.5	ns
		C <sub>L</sub> = 50 pF	-	6.0	11.0	1.0	12.5	1.0	14.0	ns
		MR to Qn; see Fig. 8 [3]								
		V <sub>CC</sub> = 3.0 V to 3.6 V								
		C <sub>L</sub> = 15 pF	-	5.1	13.6	1.0	16.0	1.0	17.0	ns
		C <sub>L</sub> = 50 pF	-	7.3	17.1	1.0	19.5	1.0	21.5	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V								
		C <sub>L</sub> = 15 pF	-	3.7	8.5	1.0	10.0	1.0	11.0	ns
		C <sub>L</sub> = 50 pF	-	5.3	10.5	1.0	12.0	1.0	13.5	ns

## Octal D-type flip-flop with reset; positive-edge trigger

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
f <sub>max</sub>	maximum frequency	see <a href="#">Fig. 7</a>								
		V <sub>CC</sub> = 3.0 V to 3.6 V								
		C <sub>L</sub> = 15 pF	75	120	-	65	-	65	-	MHz
		C <sub>L</sub> = 50 pF	50	75	-	45	-	45	-	MHz
		V <sub>CC</sub> = 4.5 V to 5.5 V								
t <sub>w</sub>	pulse width	CP HIGH or LOW; see <a href="#">Fig. 7</a>								
		V <sub>CC</sub> = 3.0 V to 3.6 V	5.0	-	-	6.5	-	6.5	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	5.0	-	-	5.0	-	5.0	-	ns
		MR LOW; see <a href="#">Fig. 8</a>								
		V <sub>CC</sub> = 3.0 V to 3.6 V	5.0	-	-	6.0	-	6.0	-	ns
t <sub>su</sub>	set-up time	Dn to CP; see <a href="#">Fig. 9</a>								
		V <sub>CC</sub> = 3.0 V to 3.6 V	3.0	-	-	3.0	-	3.0	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	3.0	-	-	3.0	-	3.0	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	-	-	1.0	-	1.0	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	1.0	-	-	1.0	-	1.0	-	ns
t <sub>h</sub>	hold time	Dn to CP; see <a href="#">Fig. 9</a>								
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	-	-	1.0	-	1.0	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	1.0	-	-	1.0	-	1.0	-	ns
t <sub>rec</sub>	recovery time	MR to CP; see <a href="#">Fig. 8</a>								
		V <sub>CC</sub> = 3.0 V to 3.6 V	2.5	-	-	2.5	-	2.5	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	ns
C <sub>PD</sub>	power dissipation capacitance	f <sub>i</sub> = 1 MHz; V <sub>I</sub> = GND to V <sub>CC</sub> [4]	-	14	-	-	-	-	-	pF



Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
<b>74AHCT273-Q100; V<sub>CC</sub> = 4.5 V to 5.5 V</b>										
t <sub>pd</sub>	propagation delay	CP to Qn; see Fig. 7 [2]								
		C <sub>L</sub> = 15 pF	-	4.0	7.5	1.0	8.8	1.0	9.5	ns
		C <sub>L</sub> = 50 pF	-	5.8	9.2	1.0	10.5	1.0	11.5	ns
		MR to Qn; see Fig. 8 [3]								
		C <sub>L</sub> = 50 pF	-	5.6	11.0	1.0	12.6	1.0	14.0	ns
f <sub>max</sub>	maximum frequency	see Fig. 7								
		C <sub>L</sub> = 15 pF	75	120	-	65	-	65	-	MHz
		C <sub>L</sub> = 50 pF	50	75	-	45	-	45	-	MHz
t <sub>w</sub>	pulse width	CP HIGH or LOW; see Fig. 7	5.0	-	-	6.5	-	6.5	-	ns
		MR LOW; see Fig. 8	5.0	-	-	6.0	-	6.0	-	ns
t <sub>su</sub>	set-up time	Dn to CP; see Fig. 9	3.0	-	-	3.0	-	3.0	-	ns
t <sub>h</sub>	hold time	Dn to CP; see Fig. 9	1.0	-	-	1.0	-	1.0	-	ns
t <sub>rec</sub>	recovery time	MR to CP; see Fig. 8	2.5	-	-	2.5	-	2.5	-	ns
C <sub>PD</sub>	power dissipation capacitance	f <sub>i</sub> = 1 MHz; V <sub>I</sub> = GND to V <sub>CC</sub> [4]	-	18	-	-	-	-	-	pF

[1] Typical values are measured at nominal supply voltage (V<sub>CC</sub> = 3.3 V and V<sub>CC</sub> = 5.0 V).

[2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.

[3] t<sub>pd</sub> is the same as t<sub>PHL</sub> only.

[4] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$$

where:

f<sub>i</sub> = input frequency in MHz;

f<sub>o</sub> = output frequency in MHz;

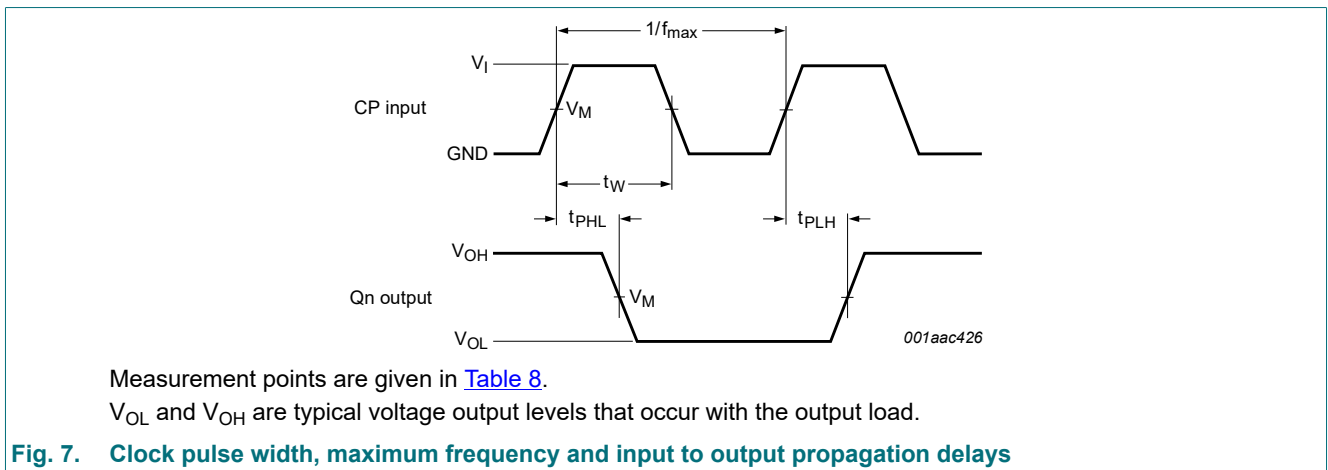
C<sub>L</sub> = output load capacitance in pF;

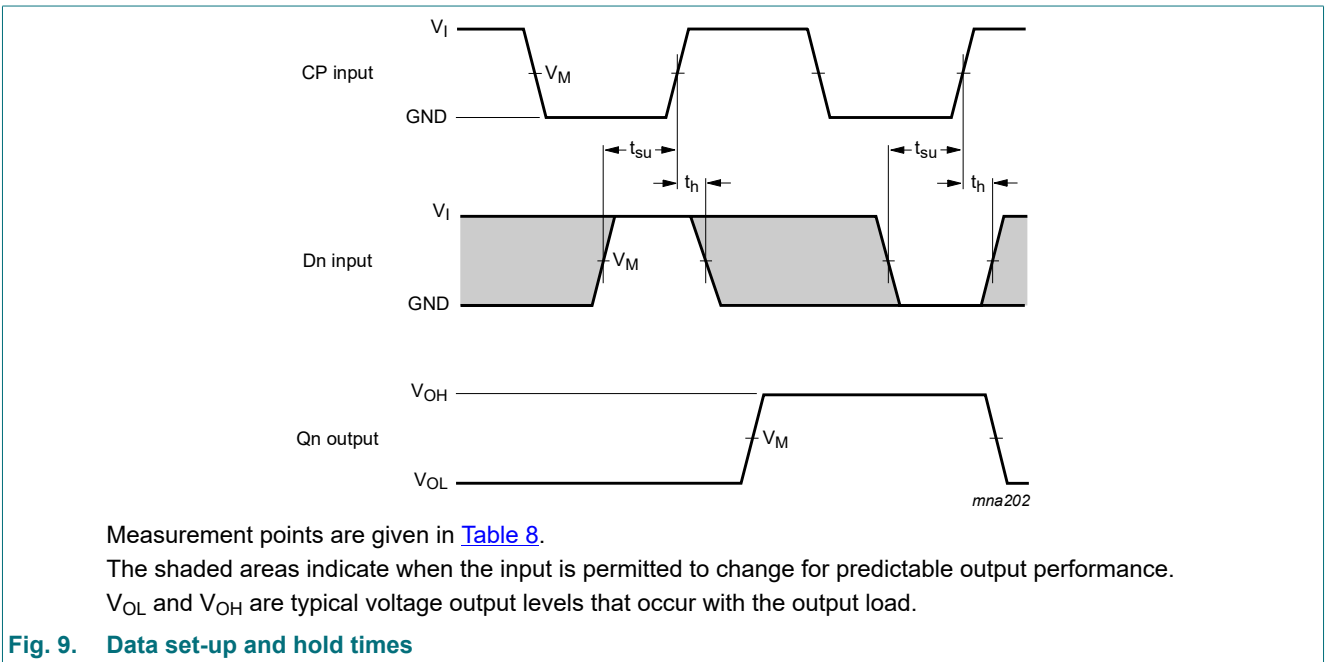
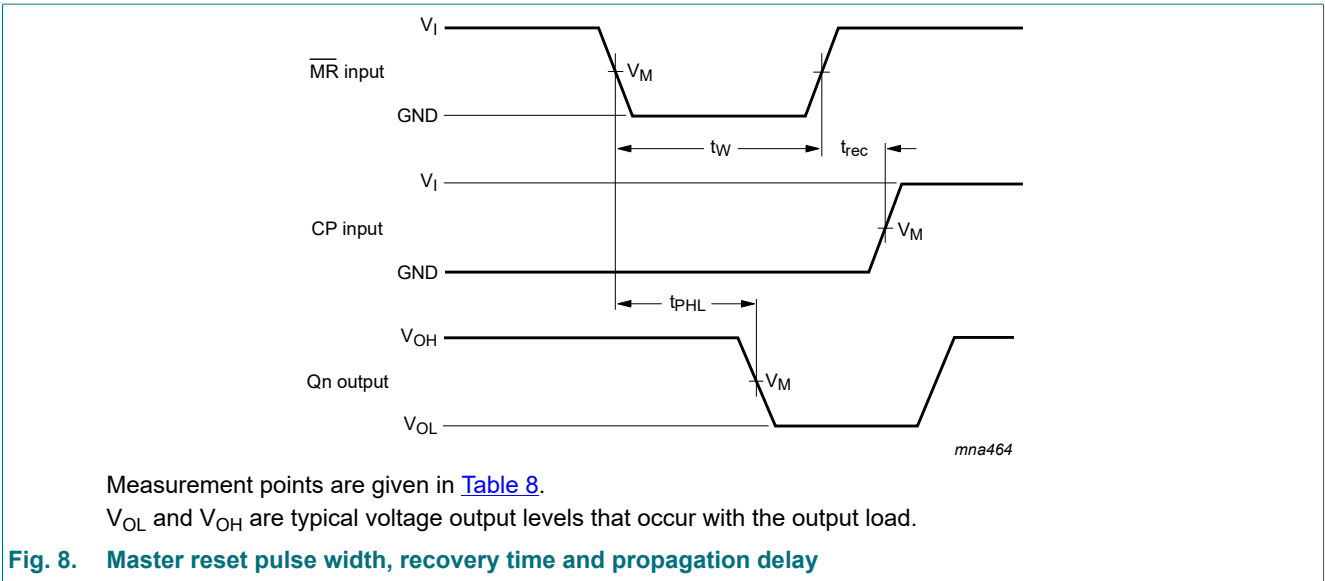
V<sub>CC</sub> = supply voltage in V;

N = number of inputs switching;

∑(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of the outputs.

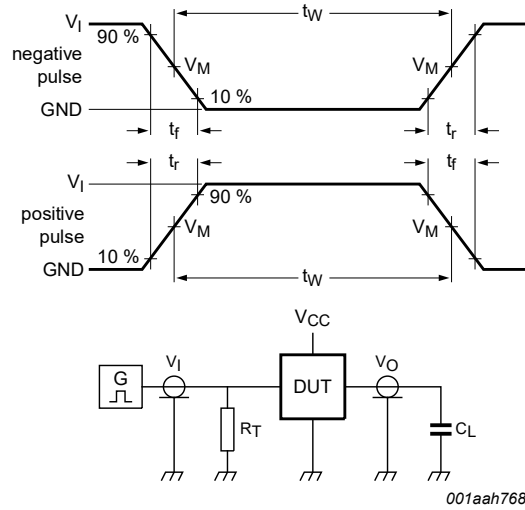
### 10.1. Waveforms and test circuit





**Table 8. Measurement points**

Type	Input	Output
	$V_M$	$V_M$
74AHC273-Q100	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
74AHCT273-Q100	1.5 V	$0.5 \times V_{CC}$



001aah768

Test data is given in [Table 9](#).

Definitions test circuit:

$R_T$  = termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$C_L$  = load capacitance including jig and probe capacitance.

**Fig. 10. Test circuit for measuring switching times**

**Table 9. Test data**

Type	Input		Load	Test
	$V_I$	$t_r, t_f$	$C_L$	
74AHC273-Q100	$V_{CC}$	$\leq 3.0$ ns	15 pF, 50 pF	$t_{PLH}, t_{PHL}$
74AHCT273-Q100	3.0 V	$\leq 3.0$ ns	15 pF, 50 pF	$t_{PLH}, t_{PHL}$

### 11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

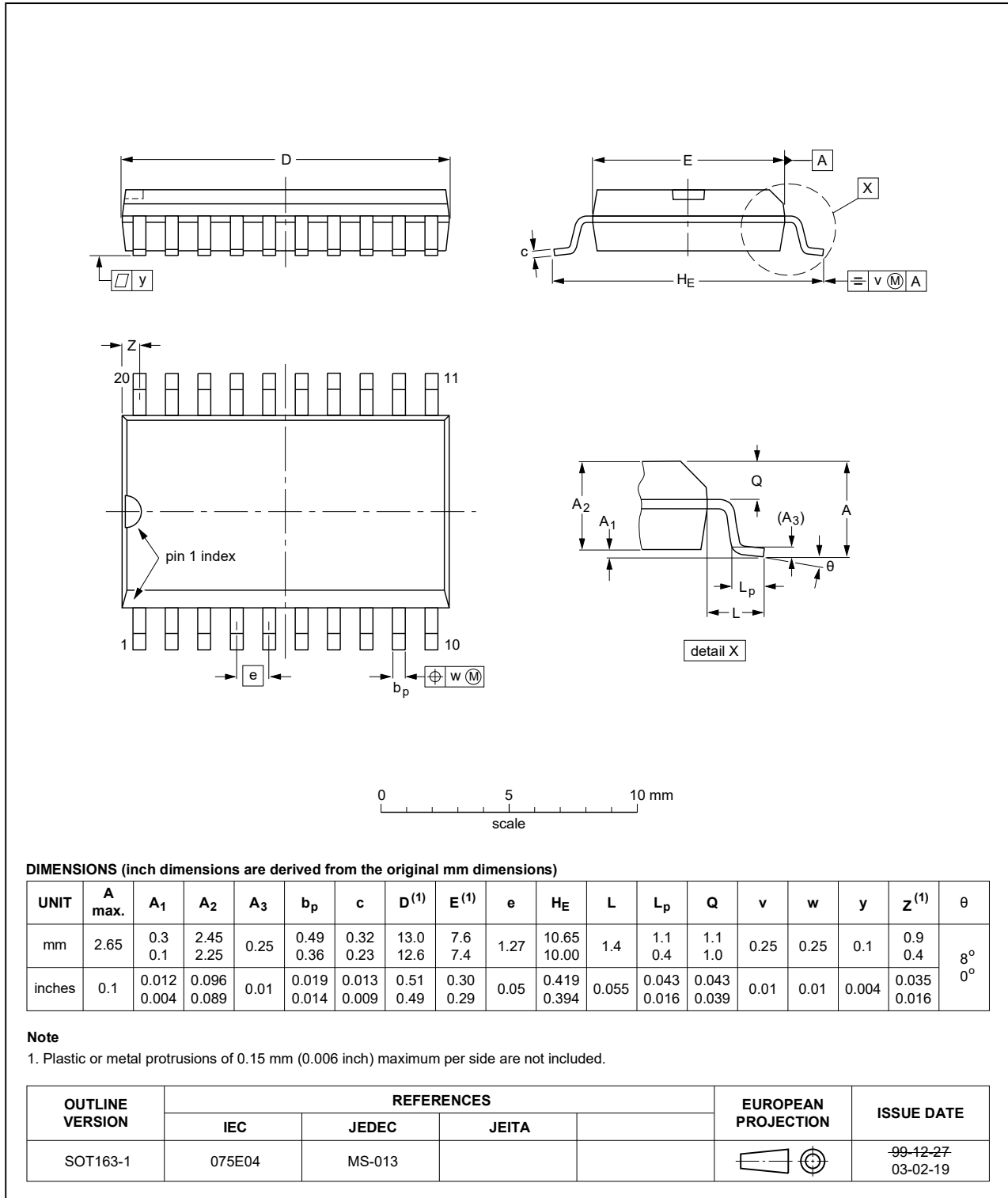


Fig. 11. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

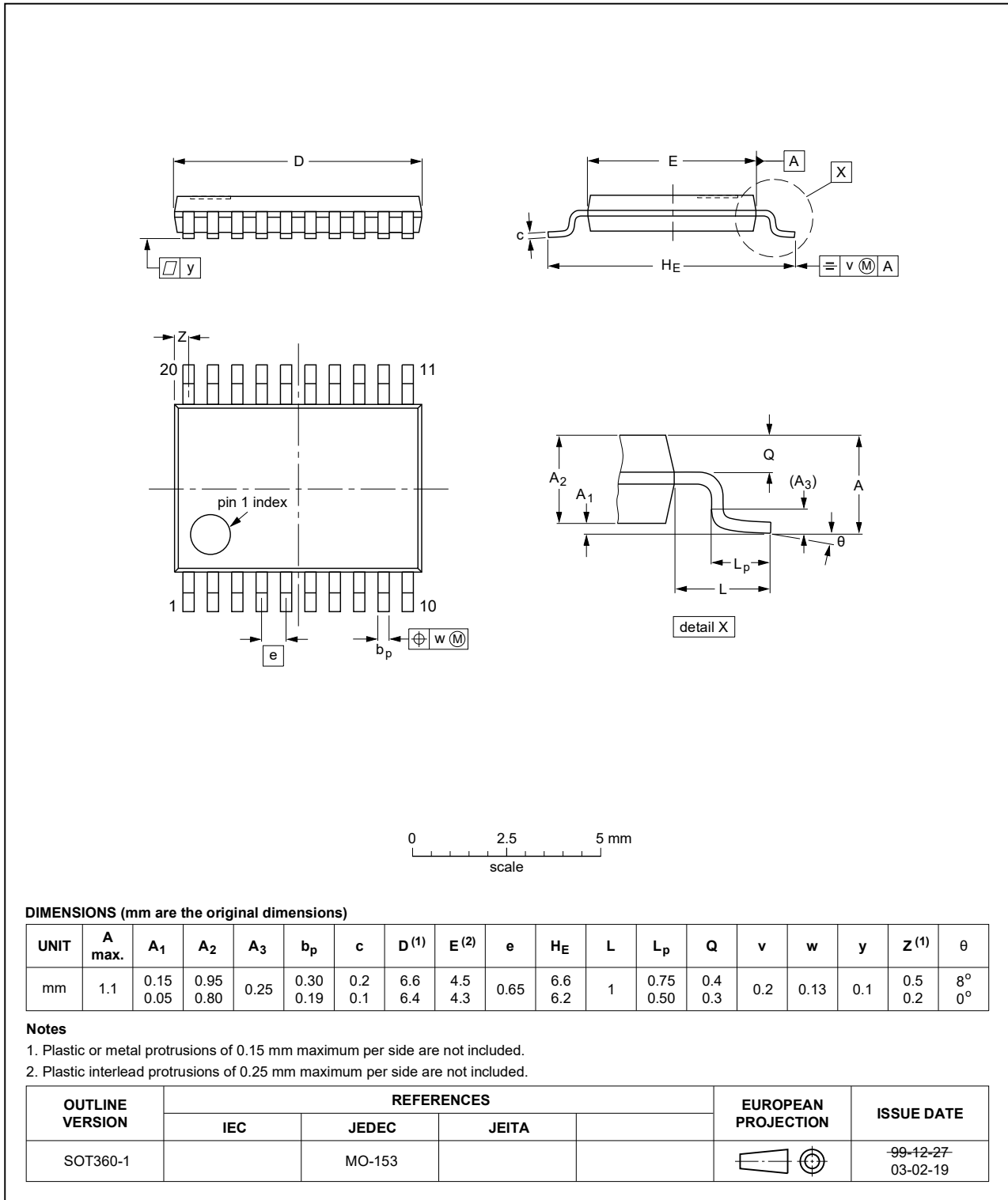


Fig. 12. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1

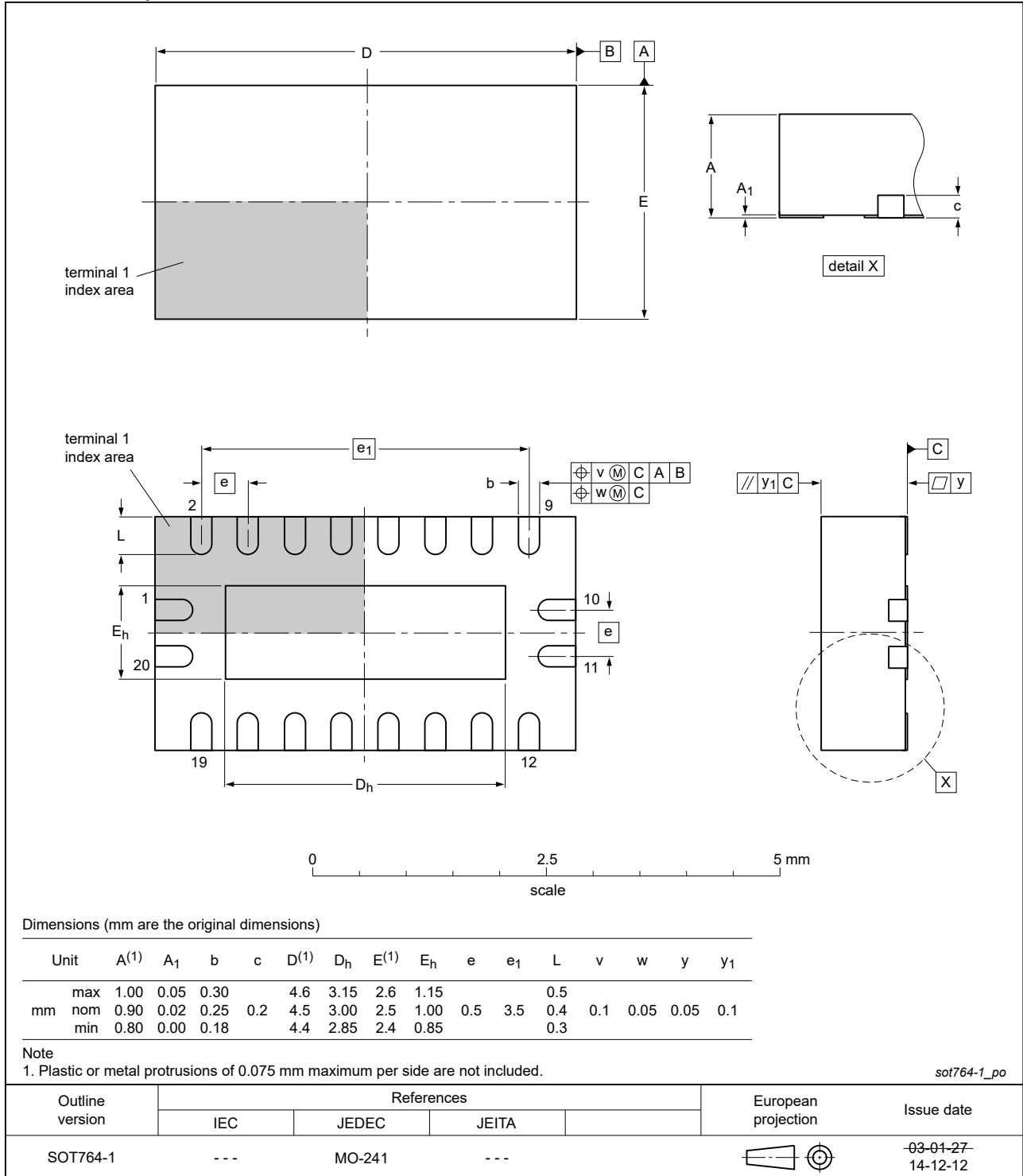


Fig. 13. Package outline SOT764-1 (DHVQFN20)

## 12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
MIL	Military
MM	Machine Model
MOS	Metal-Oxide Semiconductor

## 13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT273_Q100 v.2	20200923	Product data sheet	-	74AHC_AHCT273_Q100 v.1
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Section 2</a> updated.</li> <li><a href="#">Table 4</a>: Derating values for <math>P_{tot}</math> total power dissipation have been updated.</li> <li>Package outline drawing of SOT764-1 (<a href="#">Fig. 13</a>) updated.</li> </ul>			
74AHC_AHCT273_Q100 v.1	20130327	Product data sheet	-	-

## 14. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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## Contents

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<b>1. General description</b> .....	<b>1</b>
<b>2. Features</b> .....	<b>1</b>
<b>3. Ordering information</b> .....	<b>2</b>
<b>4. Functional diagram</b> .....	<b>2</b>
<b>5. Pinning information</b> .....	<b>4</b>
5.1. Pinning.....	4
5.2. Pin description.....	4
<b>6. Functional description</b> .....	<b>5</b>
<b>7. Limiting values</b> .....	<b>5</b>
<b>8. Recommended operating conditions</b> .....	<b>5</b>
<b>9. Static characteristics</b> .....	<b>6</b>
<b>10. Dynamic characteristics</b> .....	<b>7</b>
10.1. Waveforms and test circuit.....	9
<b>11. Package outline</b> .....	<b>12</b>
<b>12. Abbreviations</b> .....	<b>15</b>
<b>13. Revision history</b> .....	<b>15</b>
<b>14. Legal information</b> .....	<b>16</b>

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