74LVX16244

16-BIT BUS BUFFER (NON INVERTED) WITH 3-STATE OUTPUTS, 5V TOLERANT INPUT

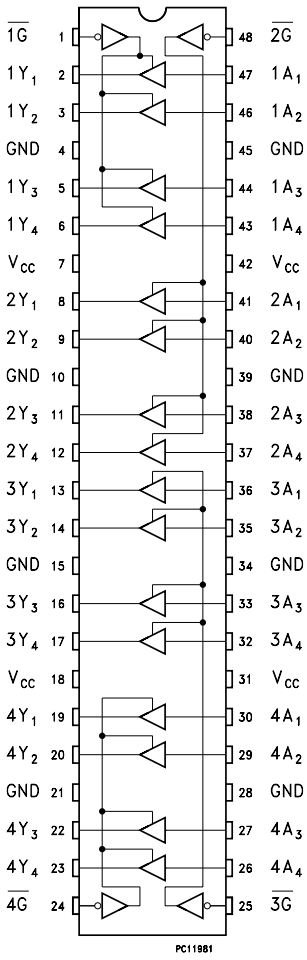
- HIGH SPEED: t_{PD} = 5.3 ns (TYP.) at V_{CC} = 3V
- 5V TOLERANT INPUT
- LOW POWER DISSIPATION: I_{CC} = 4 µA (MAX.) at T_A=25°C
- INPUT VOLTAGE LEVEL : V_{IL}= 0.8, V_{IH}=2V AT V_{CC}=3V
- POWER DOWN PROTECTION ON INPUTS & OUTPUTS
- SYMMETRICAL OUTPUT IMPEDANCE: $|I_{OH}| = I_{OL}$ = 4 mA (MIN)
- BALANCED PROPAGATION DELAYS: $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE: V_{CC}(OPR) = 2V to 3.6V (1.2V Data Retention)
- IMPROVED LATCH-UP IMMUNITY
- LOW NOISE: V_{OLP} = 0.3V (TYP.) AT V_{CC}=3V

TSSOP

ORDER CODES

PACKAGE	TUBE	T & R
TSSOP		74LVX16244TTR

PIN CONNECTION



DESCRIPTION

The 74LVX16244 is an advanced high speed CMOS 16-BIT BUS BUFFER (3-STATE) fabricated with sub-micron silicon gate and double-layer metal wiring C^2MOS technology.

Any $\overline{nG}$ output control governs four BUS BUFFERS. Output Enable inputs ($\overline{nG}$) tied together give full 16 bit operation.

When $\overline{nG}$ is LOW, the outputs are enabled. When $\overline{nG}$ is HIGH, the output are in high impedance state.

The device is designed to be used with 3-state memory address drivers, etc.

Power down protection is provided on all inputs and outputs and 0 to 7V can be accepted on inputs with no regard to the supply voltage. This device can be used to interface 5V to 3V.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

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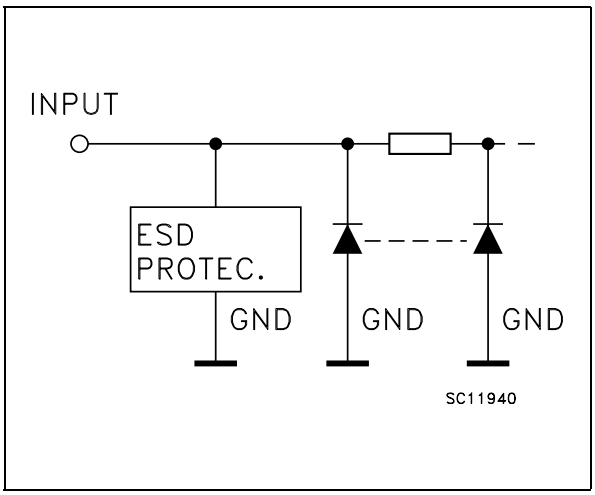
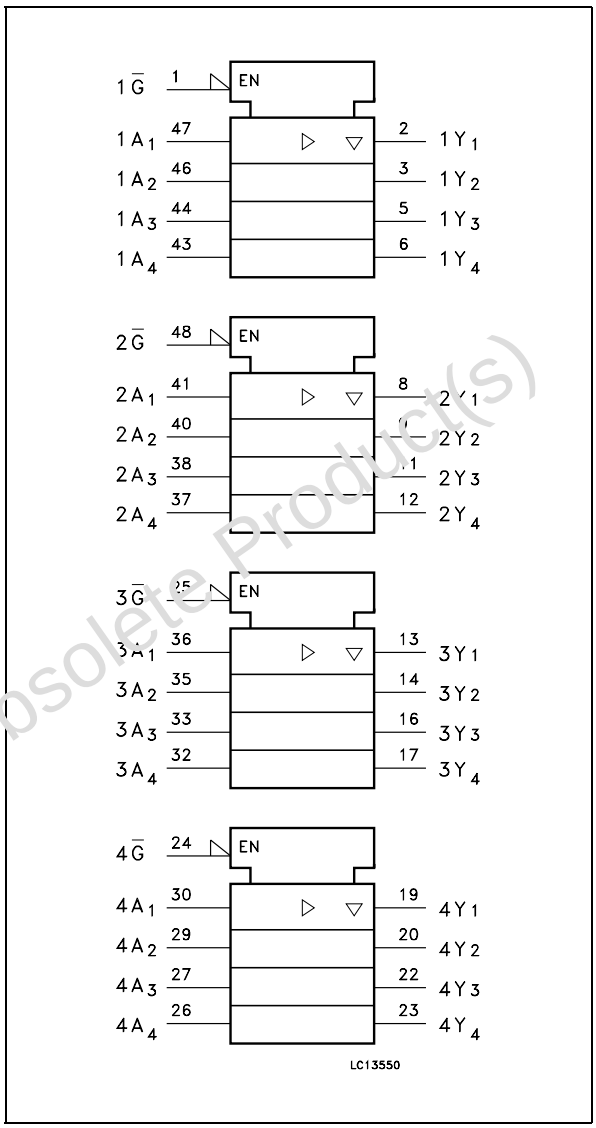
INPUT EQUIVALENT CIRCUIT



IEC LOGIC SYMBOLS



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	$1\overline{G}$	Output Enable Input
2, 3, 5, 6	1Y1 to 1Y4	Data Outputs
8, 9, 11, 12	2Y1 to 2Y4	Data Outputs
13, 14, 16, 17	3Y1 to 3Y4	Data Outputs
19, 20, 22, 23	4Y1 to 4Y4	Data Outputs
24	$4\overline{G}$	Output Enable Input
25	$3\overline{G}$	Output Enable Input
30, 29, 27, 26	4A1 to 4A4	Data Outputs
36, 35, 33, 32	3A1 to 3A4	Data Outputs
41, 40, 38, 37	2A1 to 2A4	Data Outputs
47, 46, 44, 43	1A1 to 1A4	Data Outputs
48	$2\overline{G}$	Output Enable Input
4, 10, 15, 21 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive Supply Voltage

TRUTH TABLE

INPUTS		OUTPUT
$\overline{G}$	An	Yn
L	L	L
L	H	H
H	X	Z

X : Don't Care
Z : High Impedance

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7.0	V
V_I	DC Input Voltage	-0.5 to +7.0	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	- 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (note 1)	2 to 3.6	V
V_I	Input Voltage	0 to 5.5	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature	-55 to 125	°C
dt/dv	Input Rise and Fall Time (note 2) (V_{CC} = 3.0)	0 to 100	ns/V

1) Truth Table guaranteed: 1.2 to 3.6V

2) V_{IN} from 0.8 to 2.0V

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DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0		1.5			1.5		1.5		V
		3.0		2.0			2.0		2.0		
		3.6		2.4			2.4		2.4		
V_{IL}	Low Level Input Voltage	2.0				0.5		0.5		0.5	V
		3.0				0.8		0.8		0.8	
		3.6				0.8		0.8		0.8	
V_{OH}	High Level Output Voltage	2.0	I_O=-50 µA	1.9	2.0		1.9		1.9		V
		3.0	I_O=-50 µA	2.9	3.0		2.9		2.9		
		3.0	I_O=-4 mA	2.58	4.5		2.48		2.4		
V_{OL}	Low Level Output Voltage	2.0	I_O=50 µA		0.0	0.1		0.1		0.1	V
		3.0	I_O=50 µA		0.0	0.1		0.1		0.1	
		3.0	I_O=4 mA			0.36		0.44		0.55	
Ioz	High Impedance Output Leakage Current	3.6	$V_I = V_{IH}$ or V_{IL} $V_O = V_{CC}$ or GND			± 0.25		± 2.5		± 2.5	µA
I_I	Input Leakage Current	3.6	V_I = 5V or GND			± 0.1		± 1		± 1	µA
I_{CC}	Quiescent Supply Current	3.6	$V_I = V_{CC}$ or GND			4		40		40	µA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3ns)

Symbol	Parameter	Test Condition			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time	2.7	15			6.1	11.4	1.0	13.5	1.0	15.0	ns
		2.7	50			8.6	14.9	1.0	17.0	1.0	18.0	
		3.3(*)	15			5.3	8.4	1.0	10.0	1.0	10.0	
		3.3(*)	50			7.8	11.9	1.0	13.5	1.0	13.5	
t_{PZL} t_{PZH}	Output Enable Time	2.7	15	R_L = 1KΩ		7.1	13.8	1.0	16.5	1.0	17.5	ns
		2.7	50	R_L = 1KΩ		9.6	17.3	1.0	20.0	1.0	21.0	
		3.3(*)	15	R_L = 1KΩ		6.6	10.6	1.0	12.5	1.0	12.5	
		3.3(*)	50	R_L = 1KΩ		9.1	14.1	1.0	16.0	1.0	16.0	
t_{PLZ} t_{PHZ}	Output Disable Time	2.7	50	R_L = 1KΩ		11.6	16.0	1.0	19.0	1.0	20.5	ns
		3.3(*)	50	R_L = 1KΩ		10.3	14.0	1.0	16.0	1.0	16.0	
t_{OSLH} t_{OSHL}	Output to Output Skew Time (note 1,2)	2.7	50			0.5	1.0		1.5		1.5	ns
		3.3(*)	50			0.5	1.0		1.5		1.5	

(*) Voltage range is 3.3V ± 0.3V

Note 1 : Parameter guaranteed by design. $t_{soLH} = |t_{pLHm} - t_{pLHn}|$, $t_{soHL} = |t_{pHLm} - t_{pHLn}|$

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CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition			Value							Unit
		V_{CC} (V)			T_A = 25°C			-40 to 85°C		-55 to 125°C		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
C_{IN}	Input Capacitance					6	10		10		10	pF
C_{OUT}	Output Capacitance					8						pF
C_{PD}	Power Dissipation Capacitance (note 1)	3.0	f_{IN} = 10MHz			20						pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/16$(per circuit)

DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{OLP}	Dynamic Low Voltage Quiet Output (note 1, 2)	3.3	C_L = 50 pF		0.3	0.8					V
V_{OLV}				-0.8	-0.3						V
V_{IHD}	Dynamic High Voltage Input (note 1, 3)	3.3		2.0							V
V_{ILD}	Dynamic Low Voltage Input (note 1, 3)	3.3				0.8					V

1) Worst case package.
2) Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V, (n-1) outputs switching and one output at GND.
3) Max number of data inputs (n) switching. (n-1) switching 0V to 3.3V. Inputs under test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f=1MHz.

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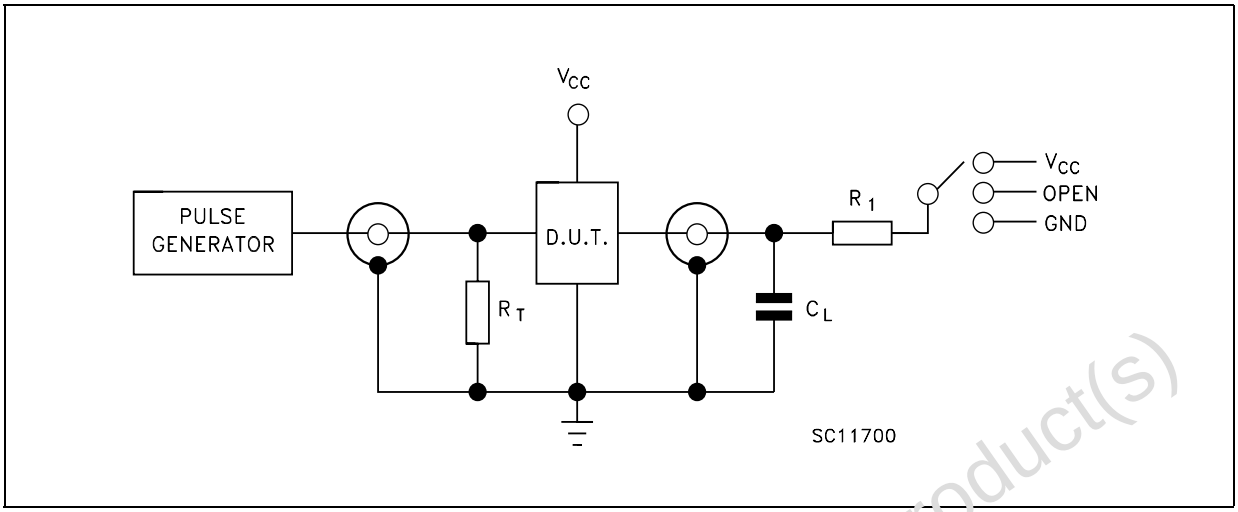
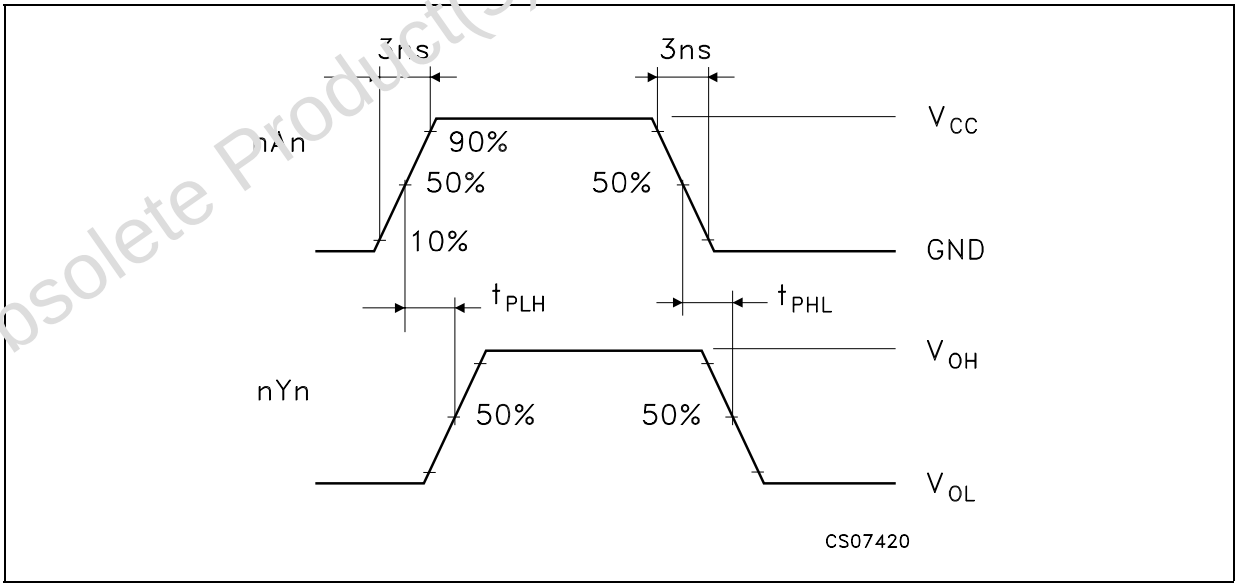
TEST CIRCUIT



TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	V_{CC}
t_{PZH}, t_{PHZ}	GND

C_L =15/ 50pF or equivalent (includes jig and probe capacitance)
$R_L = R_1$ = 1KΩ or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

WAVEFORM 1: PROPAGATION DELAYS (f=1MHz; 50% duty cycle)



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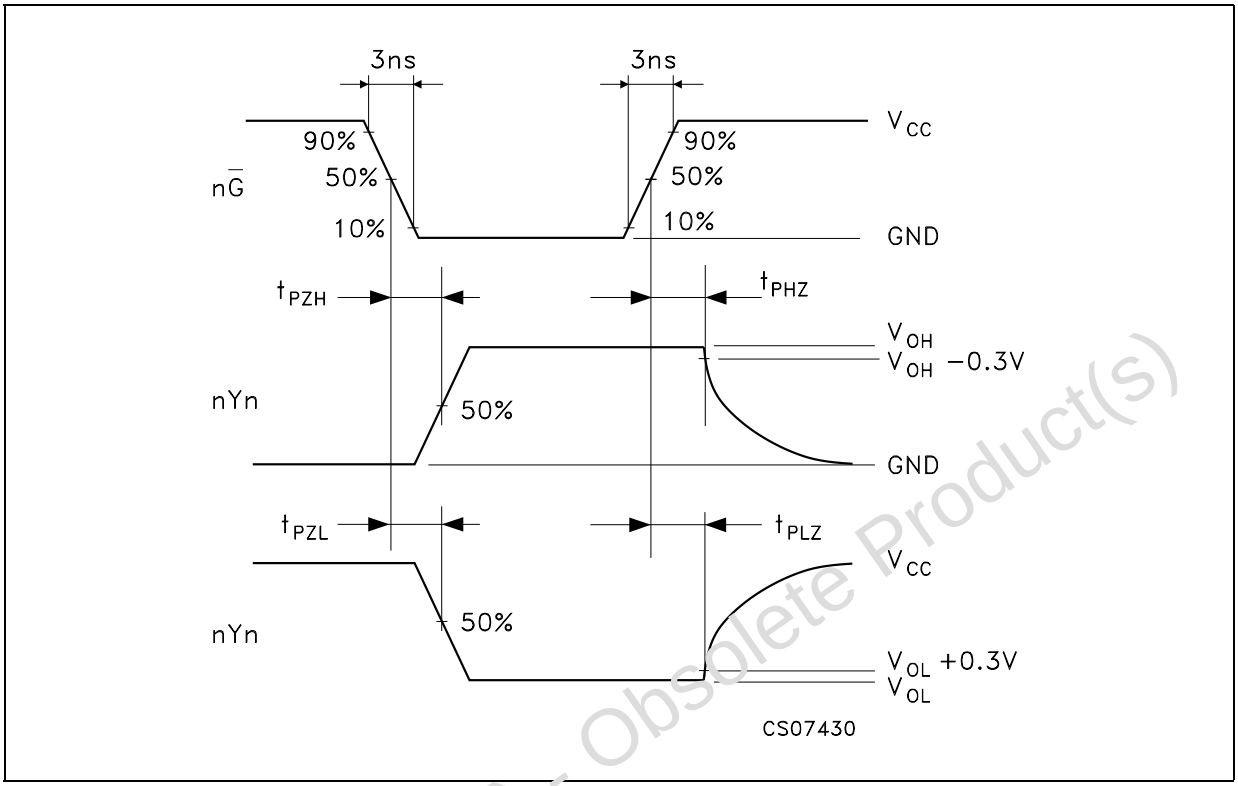
WAVEFORM 2: OUTPUT ENABLE AND DISABLE TIME (f=1MHz; 50% duty cycle)



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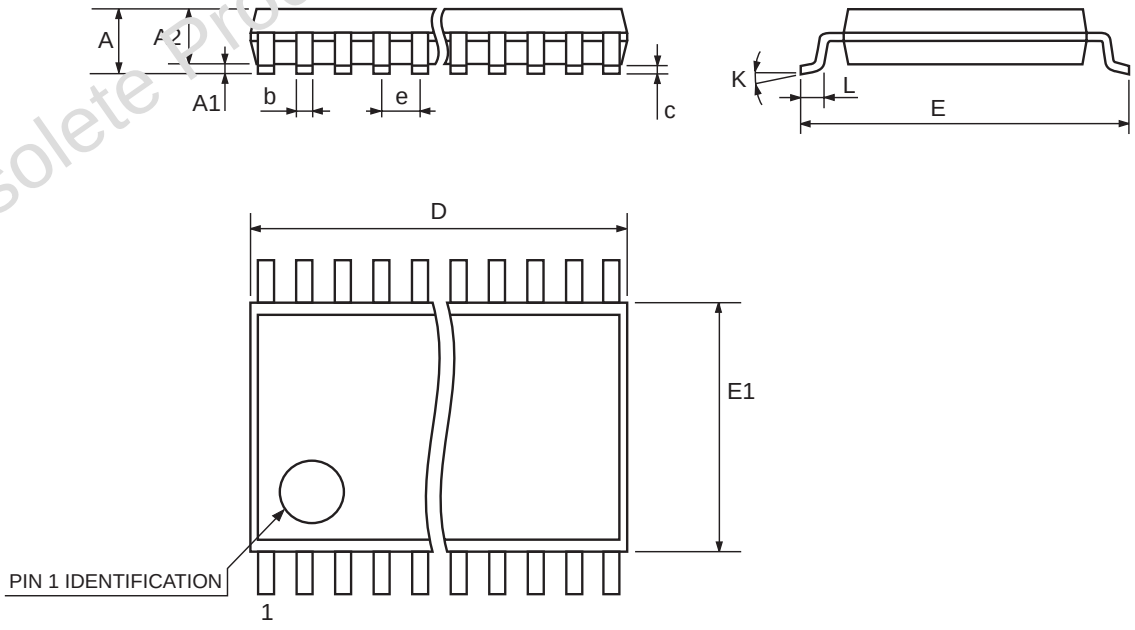
TSSOP48 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002		0.006
A2		0.9			0.035	
b	0.17		0.27	0.0067		0.011
c	0.09		0.20	0.0035		0.0079
D	12.4		12.6	0.488		0.496
E		8.1 BSC			0.318 BSC	
E1	6.0		6.2	0.236		0.244
e		0.5 BSC			0.0197 BSC	
K	0°		8°	0°		8°
L	0.50		0.75	0.020		0.030



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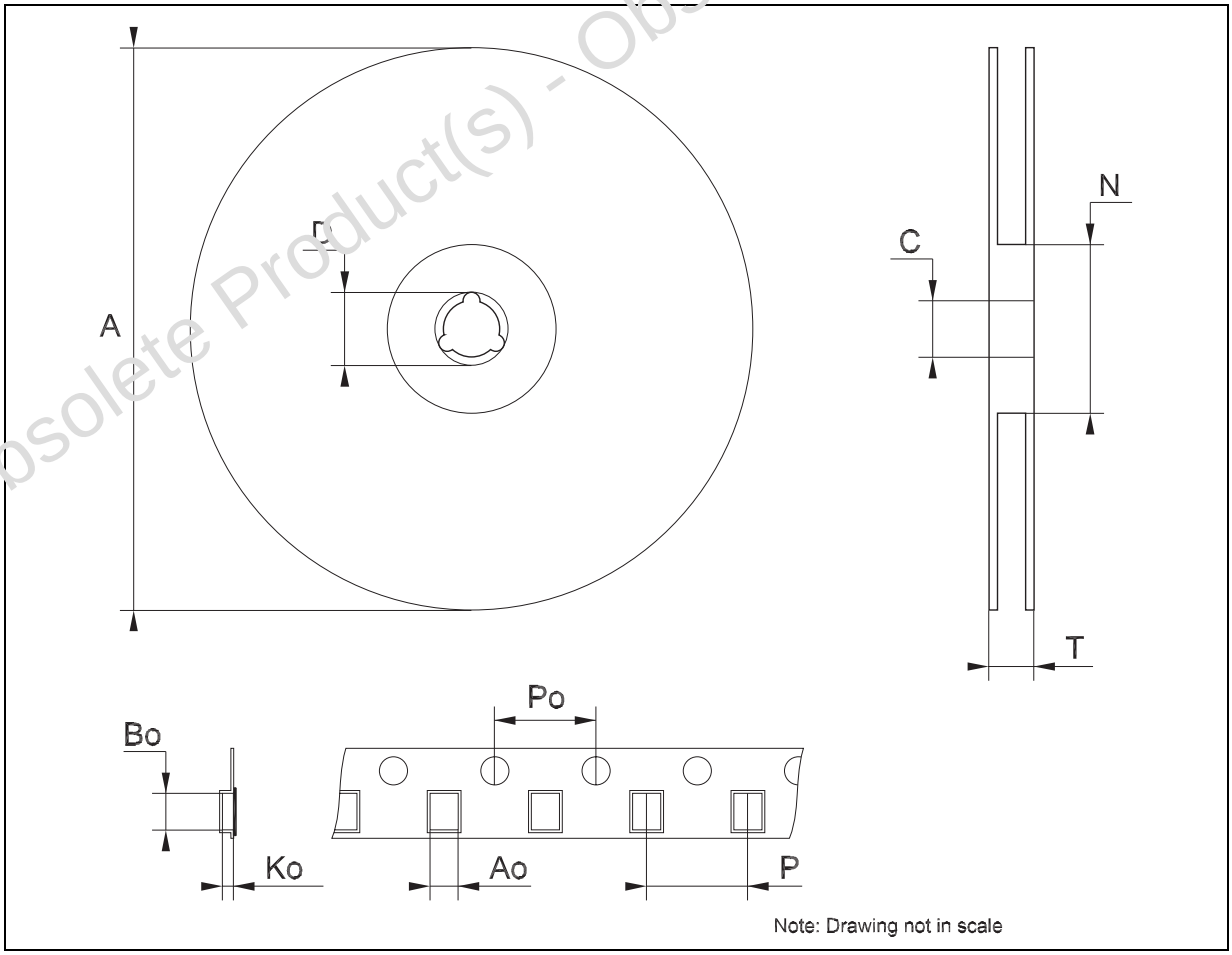
Tape & Reel TSSOP48 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			30.4			1.197
Ao	8.7		8.9	0.343		0.350
Bo	13.1		13.3	0.516		0.524
Ko	1.5		1.7	0.059		0.067
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476



Note: Drawing not in scale

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