

DATA SHEET

PDTC124T series

**NPN resistor-equipped transistors;
R1 = 22 k Ω , R2 = open**

Product specification
Supersedes data of 2004 Apr 06

2004 Aug 13

NPN resistor-equipped transistors; R1 = 22 k Ω , R2 = open

PDTC124T series

FEATURES

- Built-in bias resistors
- Simplified circuit design
- Reduction of component count
- Reduced pick and place costs.

APPLICATIONS

- General purpose switching and amplification
- Inverter and interface circuits
- Circuit driver.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V _{CEO}	collector-emitter voltage	–	50	V
I _O	output current (DC)	–	100	mA
R1	bias resistor	22	–	k Ω
R2	open	–	–	–

DESCRIPTION

NPN resistor-equipped transistor (see “Simplified outline, symbol and pinning” for package details).

PRODUCT OVERVIEW

TYPE NUMBER	PACKAGE		MARKING CODE	PNP COMPLEMENT
	PHILIPS	EIAJ		
PDTC124TE	SOT416	SC-75	41	PDTA124TE
PDTC124TEF	SOT490	SC-89	35	PDTA124TEF
PDTC124TK	SOT346	SC-59	50	PDTA124TK
PDTC124TM	SOT883	SC-101	DY	PDTA124TM
PDTC124TS	SOT54 (TO-92)	SC-43	TC124T	PDTA124TS
PDTC124TT	SOT23	–	*45 ⁽¹⁾	PDTA124TT
PDTC124TU	SOT323	SC-70	*50 ⁽¹⁾	PDTA124TU

Note

- * = p: Made in Hong Kong.
* = t: Made in Malaysia.
* = W: Made in China.

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SIMPLIFIED OUTLINE, SYMBOL AND PINNING

TYPE NUMBER	SIMPLIFIED OUTLINE AND SYMBOL	PINNING	
		PIN	DESCRIPTION
PDTC124TS		1	base
		2	collector
		3	emitter
PDTC124TE PDTC124TEF PDTC124TK PDTC124TT PDTC124TU		1	base
		2	emitter
		3	collector
PDTC124TM		1	base
		2	emitter
		3	collector

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ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PDTC124TE	–	plastic surface mounted package; 3 leads	SOT416
PDTC124TEF	–	plastic surface mounted package; 3 leads	SOT490
PDTC124TK	–	plastic surface mounted package; 3 leads	SOT346
PDTC124TM	–	leadless ultra small plastic package; 3 solder lands; body 1.0 × 0.6 × 0.5 mm	SOT883
PDTC124TS	–	plastic single-ended leaded (through hole) package; 3 leads	SOT54
PDTC124TT	–	plastic surface mounted package; 3 leads	SOT23
PDTC124TU	–	plastic surface mounted package; 3 leads	SOT323

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{CBO}	collector-base voltage	open emitter	–	50	V
V _{CEO}	collector-emitter voltage	open base	–	50	V
V _{EBO}	emitter-base voltage	open collector	–	5	V
I _O	output current (DC)		–	100	mA
I _{CM}	peak collector current		–	100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C			
	SOT54	note 1	–	500	mW
	SOT23	note 1	–	250	mW
	SOT346	note 1	–	250	mW
	SOT323	note 1	–	200	mW
	SOT490	notes 1 and 2	–	250	mW
	SOT883	notes 2 and 3	–	250	mW
	SOT416	note 1	–	150	mW
T _{stg}	storage temperature		–65	+150	°C
T _j	junction temperature		–	150	°C
T _{amb}	operating ambient temperature		–65	+150	°C

Notes

1. Refer to standard mounting conditions.
2. Reflow soldering is the only recommended soldering method.
3. Refer to SOT883 standard mounting conditions; FR4 with 60 μ m copper strip line.

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R _{th(j-a)}	thermal resistance from junction to ambient	in free air		
	SOT54	note 1	250	K/W
	SOT23	note 1	500	K/W
	SOT346	note 1	500	K/W
	SOT323	note 1	625	K/W
	SOT490	notes 1 and 2	500	K/W
	SOT883	notes 2 and 3	500	K/W
SOT416	note 1	833	K/W	

Notes

1. Refer to standard mounting conditions.
2. Reflow soldering is the only recommended soldering method.
3. Refer to SOT883 standard mounting conditions; FR4 with 60 μ m copper strip line.

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I _{CBO}	collector-base cut-off current	V _{CB} = 50 V; I _E = 0 A	–	–	100	nA
I _{CEO}	collector-emitter cut-off current	V _{CE} = 30 V; I _B = 0 A	–	–	1	μ A
		V _{CE} = 30 V; I _B = 0 A; T _j = 150 °C	–	–	50	μ A
I _{EBO}	emitter-base cut-off current	V _{EB} = 5 V; I _C = 0 A	–	–	100	nA
h _{FE}	DC current gain	V _{CE} = 5 V; I _C = 1 mA	100	–	–	
V _{CEsat}	collector-emitter saturation voltage	I _C = 10 mA; I _B = 0.5 mA	–	–	150	mV
R1	input resistor		15.4	22	28.6	k Ω
C _c	collector capacitance	I _E = i _e = 0 A; V _{CB} = 10 V; f = 1 MHz	–	–	2.5	pF

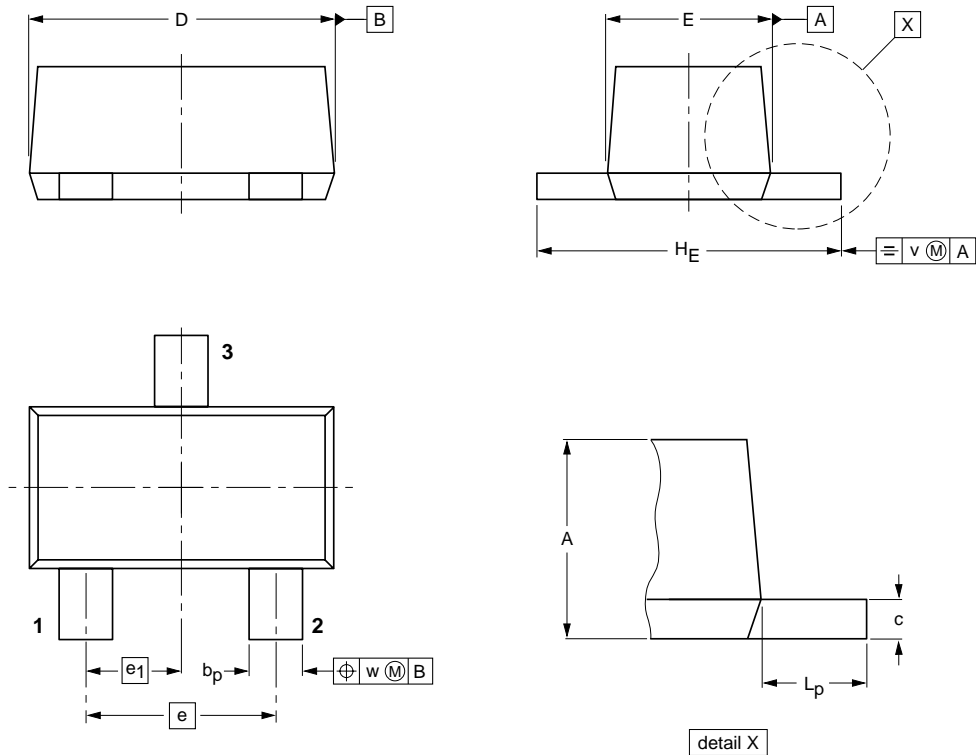
NPN resistor-equipped transistors;
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PACKAGE OUTLINES

Plastic surface mounted package; 3 leads

SOT490



DIMENSIONS (mm are the original dimensions)

UNIT	A	b _p	c	D	E	e	e ₁	H _E	L _p	v	w
mm	0.8 0.6	0.33 0.23	0.2 0.1	1.7 1.5	0.95 0.75	1.0	0.5	1.7 1.5	0.5 0.3	0.1	0.1

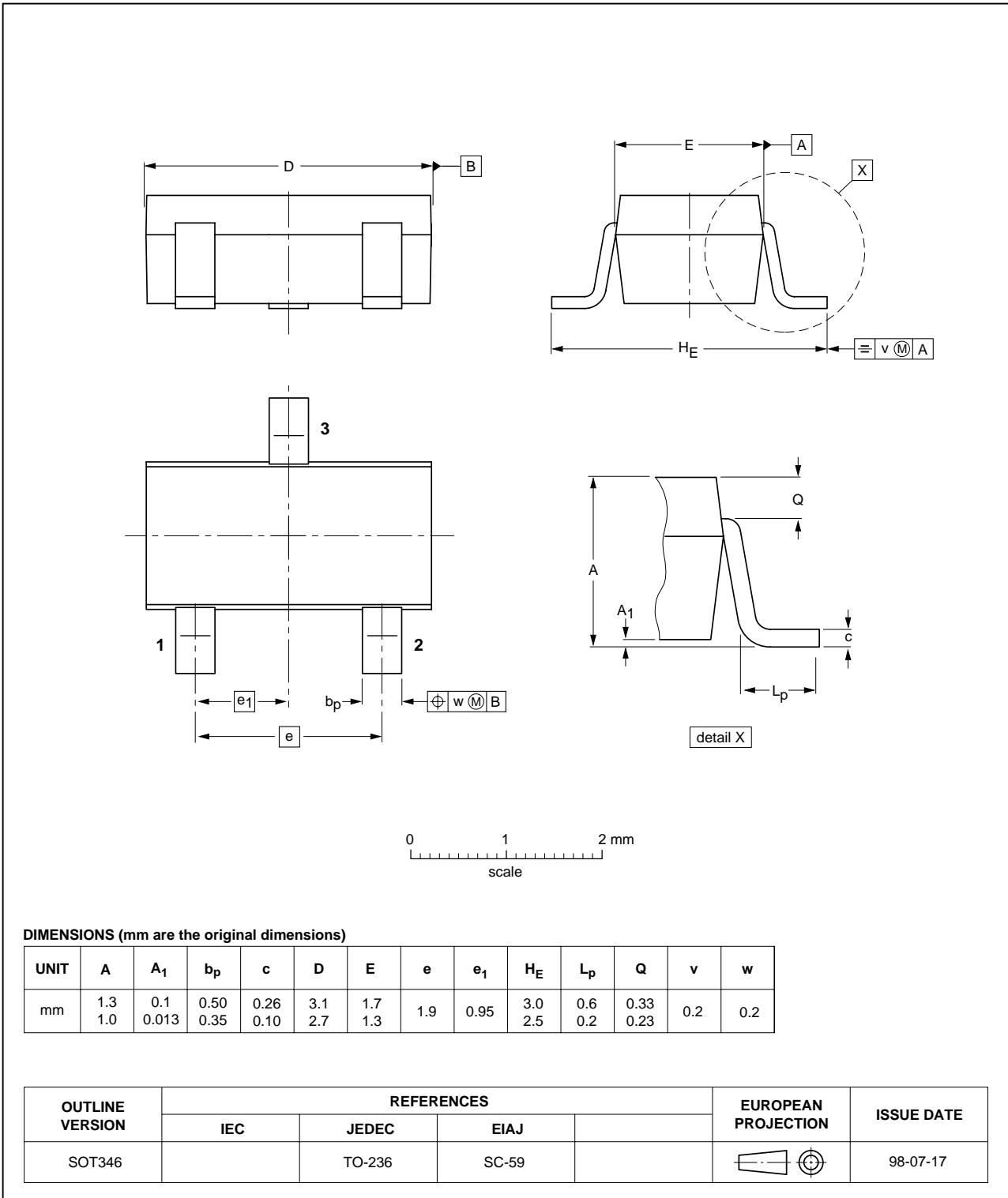
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT490			SC-89		98-10-23

NPN resistor-equipped transistors;
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PDTC124T series

Plastic surface mounted package; 3 leads

SOT346

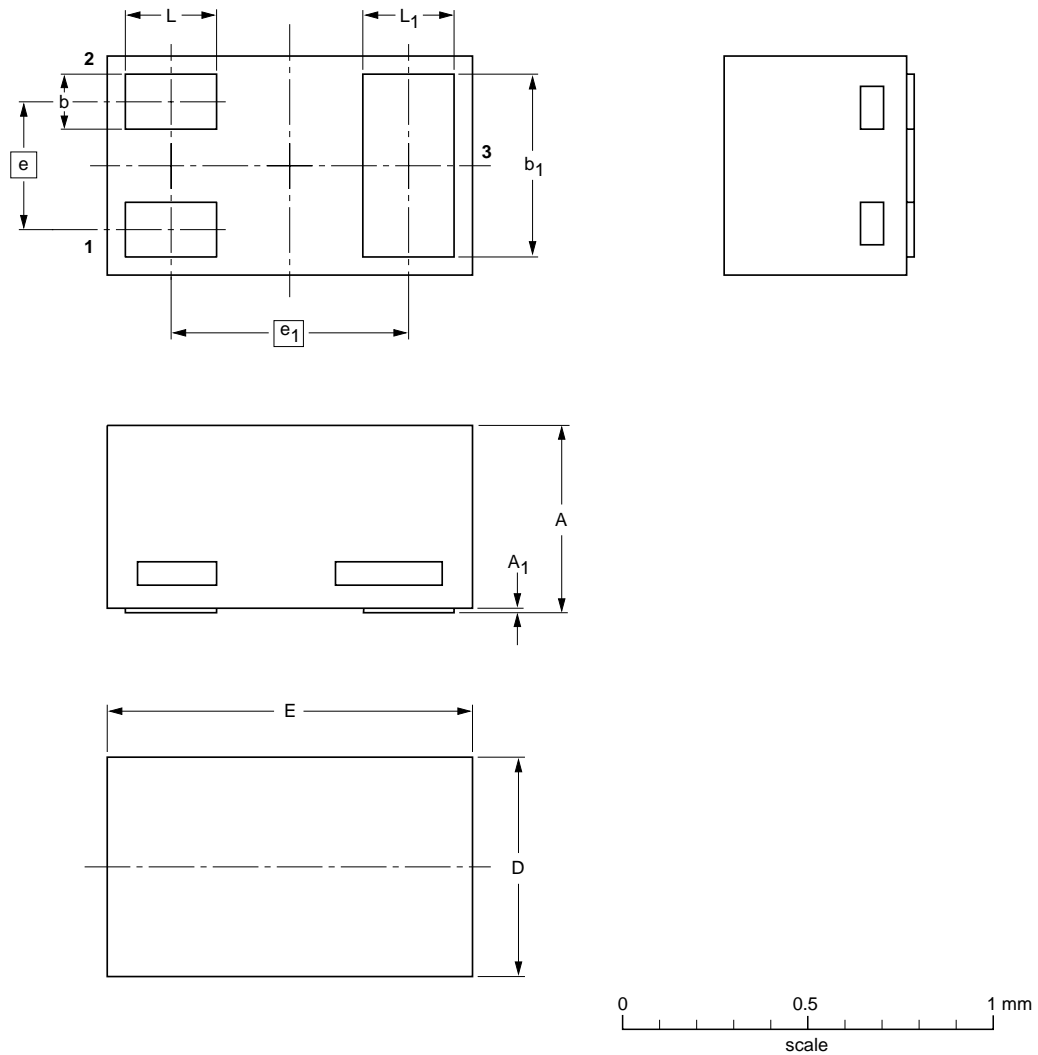


NPN resistor-equipped transistors;
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PDTC124T series

Leadless ultra small plastic package; 3 solder lands; body 1.0 x 0.6 x 0.5 mm

SOT883



DIMENSIONS (mm are the original dimensions)

UNIT	A ⁽¹⁾	A ₁ max.	b	b ₁	D	E	e	e ₁	L	L ₁
mm	0.50 0.46	0.03	0.20 0.12	0.55 0.47	0.62 0.55	1.02 0.95	0.35	0.65	0.30 0.22	0.30 0.22

Note

1. Including plating thickness

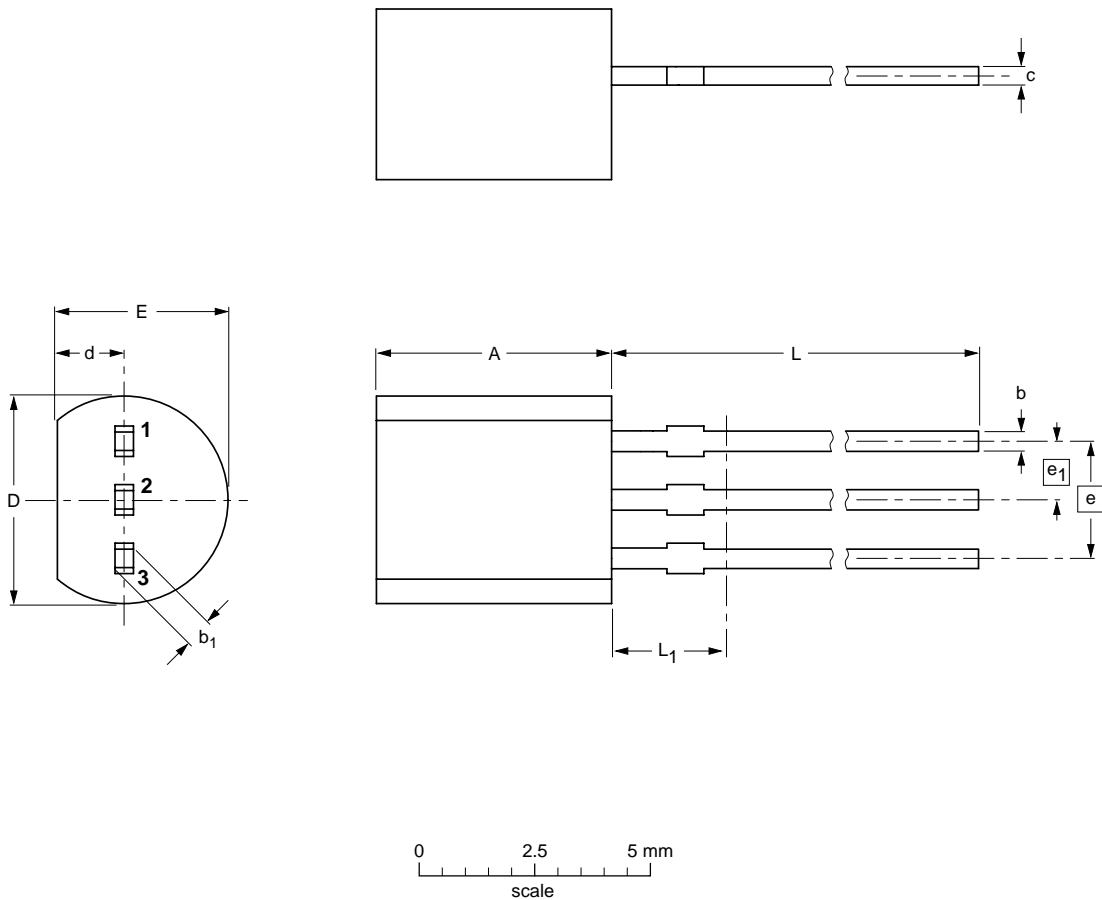
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT883			SC-101		03-02-05 03-04-03

NPN resistor-equipped transistors;
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PDTC124T series

Plastic single-ended leaded (through hole) package; 3 leads

SOT54



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b ₁	c	D	d	E	e	e ₁	L	L ₁ ⁽¹⁾ max.
mm	5.2 5.0	0.48 0.40	0.66 0.55	0.45 0.38	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

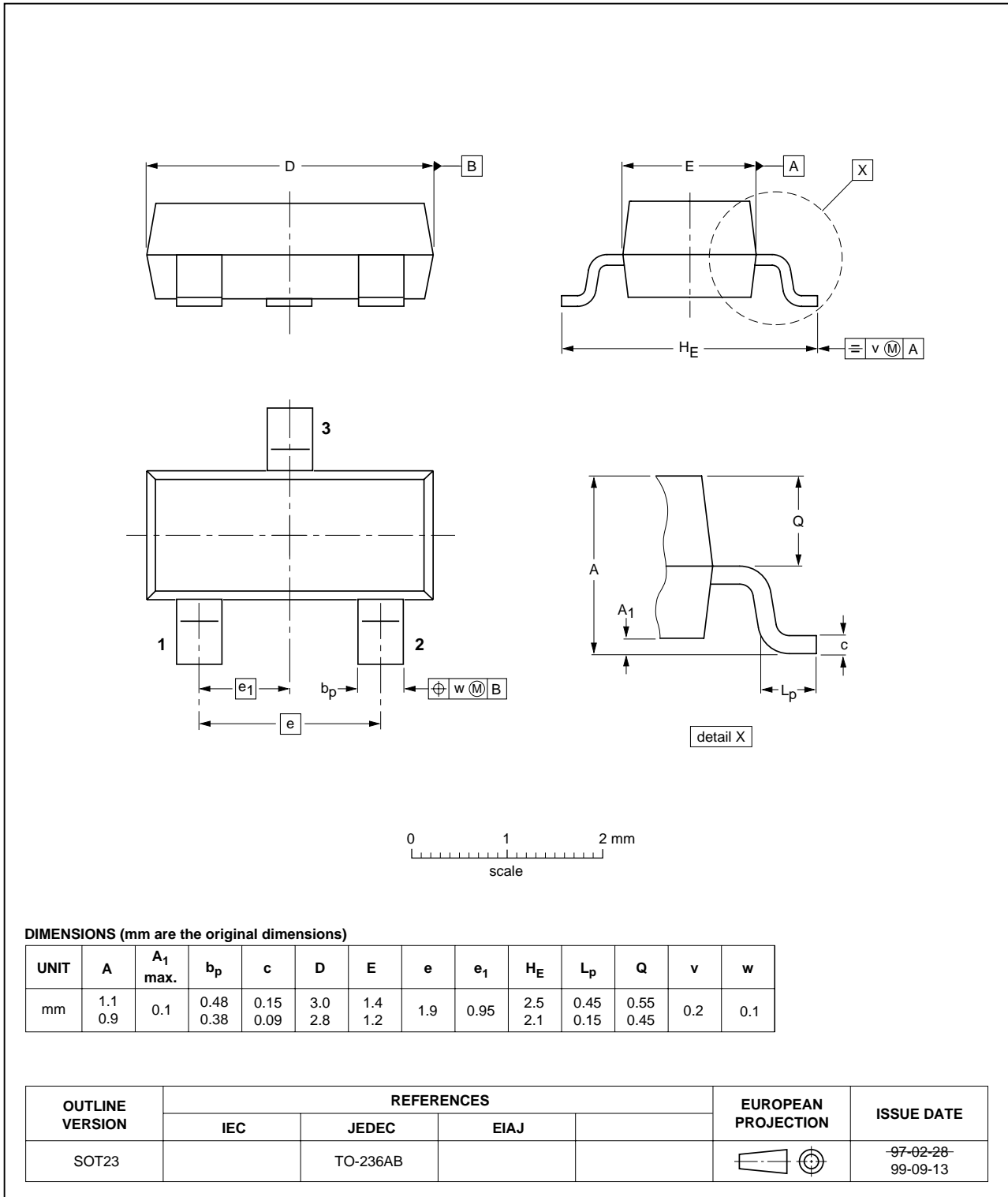
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT54		TO-92	SC-43A		-97-02-28 04-06-28

NPN resistor-equipped transistors;
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Plastic surface mounted package; 3 leads

SOT23

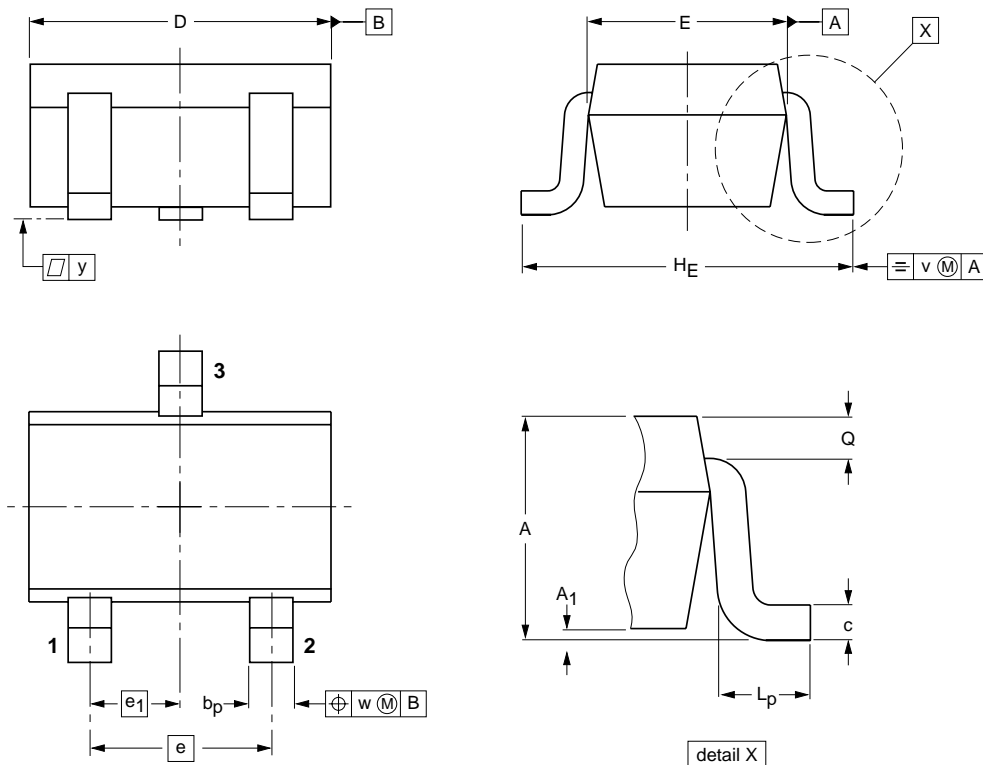


NPN resistor-equipped transistors;
R1 = 22 kΩ, R2 = open

PDTC124T series

Plastic surface mounted package; 3 leads

SOT323



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max	b _p	c	D	E	e	e ₁	H _E	L _p	Q	v	w
mm	1.1 0.8	0.1	0.4 0.3	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2

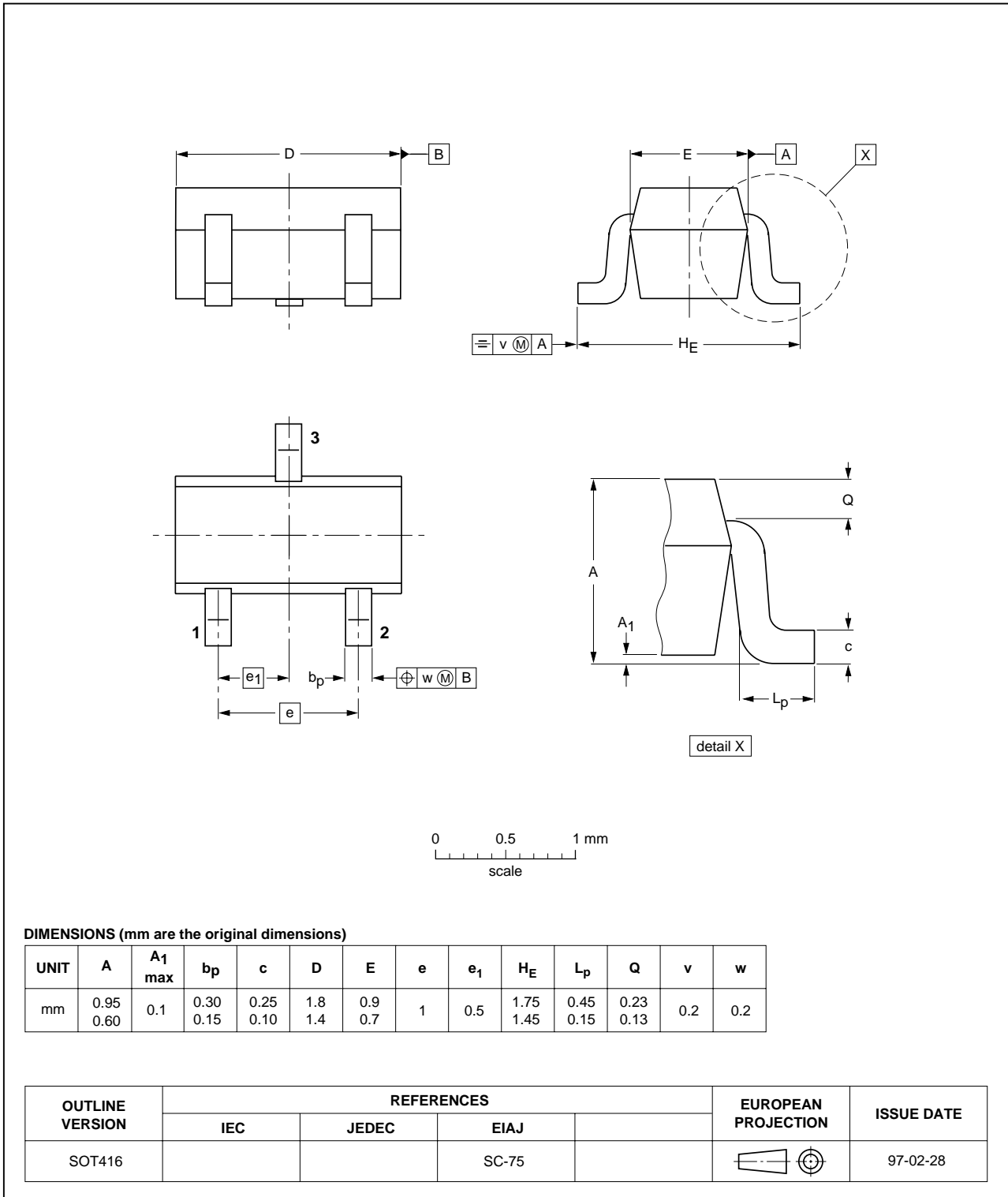
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT323			SC-70			97-02-28

NPN resistor-equipped transistors;
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Plastic surface mounted package; 3 leads

SOT416



NPN resistor-equipped transistors;
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DATA SHEET STATUS

LEVEL	DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾⁽³⁾	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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Notes

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3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Contact information

For additional information please visit <http://www.semiconductors.philips.com>. Fax: +31 40 27 24825

For sales offices addresses send e-mail to: sales.addresses@www.semiconductors.philips.com.

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