Low-Voltage, 0.8 Ω R_{ON}, Dual SPST Analog Switch

DESCRIPTION

The DG2741, DG2742, DG2743 are low voltage, single supply, dual SPST analog switches. Designed for high performance switching of analog signals, the DG2741, DG2742, DG2743 provide low on-resistance (0.8 Ω at + 2.7 V), fast speed (t_{ON}, t_{OFF} at 35 ns and 33 ns) and the ability to handle signals over the entire analog voltage range.

When operated on a + 3 V supply, control pins are compatible with 1.8 V digital logic. Additionally, on-resistance flatness and matching (0.18 Ω and 0.08 Ω, respectively) offer high accuracy between channels.

The DG2741 contains two normally open (NO) switches, the DG2742 contains two normally closed (NC) switches, and the DG2743 contains one normally open and one normally closed switch. Break-before-make is guaranteed.

Built on Vishay Siliconix's low voltage submicron CMOS process, the DG2741, DG2742, DG2743 were designed to offer solutions that extend beyond audio/video functions, to providing the performance required for today's demanding mixed-signal switching in portable applications.

FEATURES

- Low voltage operation (1.6 V to 3.6 V)
- Low on-resistance - $R_{DS(on)}$: 0.8 Ω at 2.7 V
- High current handling capacity: 150 mA continuous
- Off-isolation: - 56 dB at 1 MHz
- Fast switching: 25 ns t_{ON}
- Low charge injection - Q_{INJ}: 5.8 pC
- Low power consumption: < 1 µW
- ESD protection > 2 000 V

BENEFITS

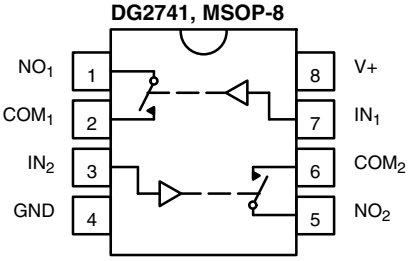
- High accuracy
- High bandwidth
- TTL and low voltage logic compatibility
- Low power consumption
- Reduced PCB space (SOT23-8 and MSOP-8)

APPLICATIONS

- Mixed signal routing
- Portable and battery operated systems
- Low voltage data acquisition
- Modems
- PCMCIA cards

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION (DG2741)

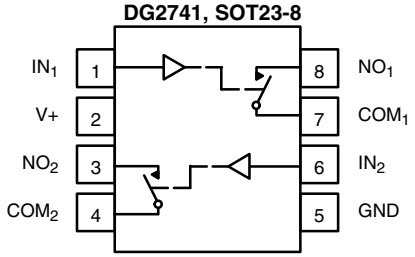
DG2741, MSOP-8



Top View

Device Marking: 2741

DG2741, SOT23-8



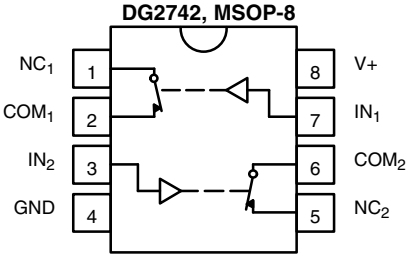
Top View

Device Marking: F3

TRUTH TABLE (DG2741)	
Logic	**Switch**
0	Off
1	On

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION (DG2742, DG2743)

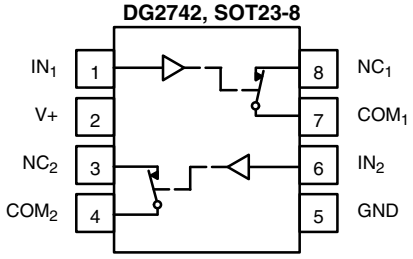
DG2742, MSOP-8



Top View

Device Marking: 2742

DG2742, SOT23-8

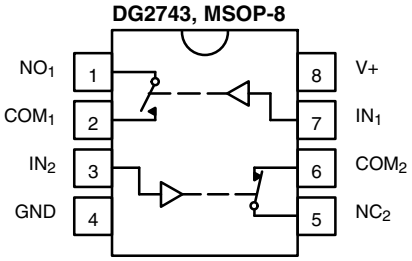


Top View

Device Marking: F4

TRUTH TABLE (DG2742)	
Logic	**Switch**
0	On
1	Off

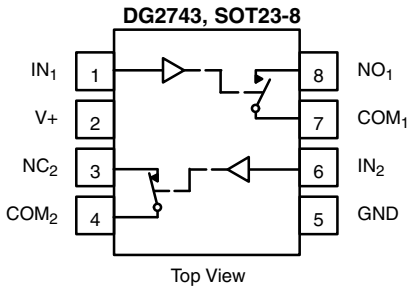
DG2743, MSOP-8



Top View

Device Marking: 2743

DG2743, SOT23-8



Top View

Device Marking: F5

TRUTH TABLE (DG2743)		
Logic	**Switch-1**	**Switch-2**
0	Off	On
1	On	Off

ORDERING INFORMATION		
Temp. Range	**Package**	**Part Number**
- 40 °C to 85 °C	MSOP-8	DG2741DQ-T1
		DG2742DQ-T1
		DG2743DQ-T1
	SOT23-8	DG2741DS-T1
		DG2742DS-T1
		DG2743DS-T1

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)			
Parameter		**Limit**	**Unit**
Referenced V+ to GND		- 0.3 to + 4 V	V
IN, COM, NC, NO[a]		- 0.3 V to (V+ + 0.3 V)	
Continuous Current (NO, NC and COM Pins)		± 200	mA
Peak Current (Pulsed at 1 ms, 10 % duty cycle)		± 300	
ESD per Method 3015.7		> 2	kV
Storage Temperature (D Suffix)		- 65 to 150	°C
Power Dissipation (Packages)[c]	6-Pin SC-70[c]	250	mW

Notes:
a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC board.
c. Derate 3.1 mW/°C above 70 °C.

SPECIFICATIONS (V+ = 1.8 V)							
Parameter	**Symbol**	**Test Conditions Otherwise Unless Specified** V+ = 1.8 V, ± 10 %, V_{IN} = 0.4 or 1.0 V[e]	**Temp.[a]**	**Limits** - 40 °C to 85 °C **Min.[b]**	**Typ.[c]**	**Max.[b]**	**Unit**
Analog Switch							
Analog Signal Range[d]	V_{NO}, V_{NC} V_{COM}		Full	0		V+	V
On-Resistance	R_{ON}	V+ = 1.8 V, V_{COM} = 0.9 V I_{NO}, I_{NC} = 10 mA	Room Full[d]		0.9	2.5 4.0	Ω
R_{ON} Flatness[d]	R_{ON} Flatness	V+ = 1.8 V, V_{COM} = 0 to V+, I_{NO}, I_{NC} = 10 mA	Room		0.25		
R_{ON} Match[d]	ΔR_{ON}		Room		0.05		
Switch Off Leakage Current[f]	$I_{NO(off)}$ $I_{NC(off)}$	V+ = 1.8 V V_{NO}, V_{NC} = 0.2 V/2.0 V, V_{COM} = 1.5 V/0.3 V	Room Full[d]	- 1 - 10		1 10	nA
	$I_{COM(off)}$		Room Full[d]	- 1 - 10		1 10	
Channel-On Leakage Current[f]	$I_{COM(on)}$	V+ = 1.8 V, V_{NO}, V_{NC} = V_{COM} = 0.3 V/1.5 V	Room Full[d]	- 1 - 10		1 10	
Digital Control							
Input High Voltage	V_{INH}		Full	1.0			V
Input Low Voltage	V_{INL}		Full			0.4	
Input Capacitance[d]	C_{in}		Full		5.5		pF
Input Current[f]	I_{INL} or I_{INH}	V_{IN} = 0 or V+	Full	- 1		1	µA
Dynamic Characteristics							
Turn-On Time[d]	t_{ON}	V_{NO} or V_{NC} = 1.5 V, R_L = 50 Ω, C_L = 35 pF figures 1 and 2	Room Full[d]		33	45 50	ns
Turn-Off Time[d]	t_{OFF}		Room Full[d]		27	40 45	
Break-Before-Make Time[d]	t_d		Room	3			
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω, figure 3	Room		20		pC
Off-Isolation[d]	OIRR	R_L = 1 kΩ, C_L = 5 pF, f = 1 MHz	Room		55		dB
Crosstalk[d]	X_{TALK}		Room		91		
NO, NC Off Capacitance[d]	$C_{NO(off)}$ $C_{NC(off)}$	V_{IN} = 0 or V+, f = 1 MHz	Room		88		pF
Channel-On Capacitance[d]	C_{ON}		Room		105		

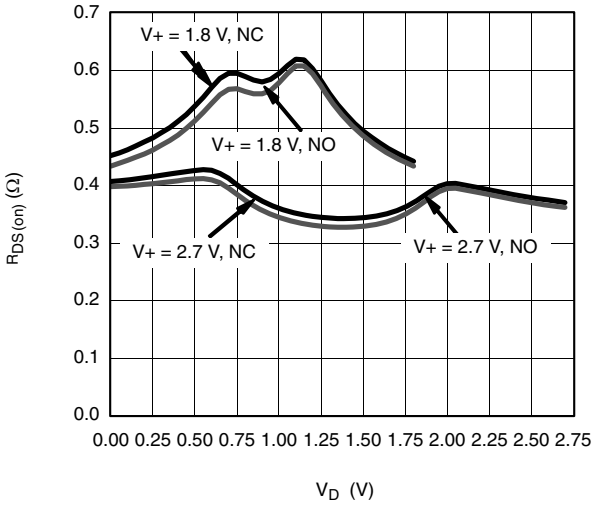
SPECIFICATIONS (V+ = 3.0 V)

Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ± 10 %, V_{IN} = 0.5 or 1.4 V[e]	Temp.[a]	Limits - 40 °C to 85 °C Min.[b]	Typ.[c]	Max.[b]	Unit
Analog Switch							
Analog Signal Range[d]	V_{NO}, V_{NC} V_{COM}		Full	0		V+	V
On-Resistance	R_{ON}	V+ = 2.7 V, V_{COM} = 0.2 V/1.5 V, I_{NO} I_{NC} = 100 mA	Room Full		0.4	0.8 0.9	Ω
R_{ON} Flatness	R_{ON} Flatness	V+ = 2.7 V, V_{COM} = 1.5, 2 V, I_{NO}, I_{NC} = 100 mA	Room		0.8	0.18	
R_{ON} MatchFlat	ΔR_{ON}		Room		0.05	0.08	
Switch Off Leakage Current	$I_{NO(off)}$ $I_{NC(off)}$	V+ = 3.3 V V_{NO}, V_{NC} = 0.3 V/3 V, V_{COM} = 3 V/0.3 V	Room Full	- 1 - 10		1 10	nA
	$I_{COM(off)}$		Room Full	- 1 - 10		1 10	
Channel-On Leakage Current	$I_{COM(on)}$	V+ = 3.3 V, V_{NO}, V_{NC} = V_{COM} = 0.3 V/3 V	Room Full	- 1 - 10		1 10	
Digital Control							
Input High Voltage	V_{INH}		Full	1.4			V
Input Low Voltage	V_{INL}		Full			0.5	
Input Capacitance[d]	C_{in}		Full		5.5		pF
Input Current[f]	I_{INL} or I_{INH}	V_{IN} = 0 or V+	Full	- 1		1	µA
Dynamic Characteristics							
Turn-On Time	t_{ON}	V_{NO} or V_{NC} = 1.5 V, R_L = 50 Ω, C_L = 35 pF V+ = 2.7 V, figures 1 and 2	Room Full		20	30 35	ns
Turn-Off Time	t_{OFF}		Room Full		18	28 33	
Break-Before-Make Time	t_d		Room	1			
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω, figure 3	Room		5.8		pC
Off-Isolation[d]	OIRR	R_L = 1 kΩ, C_L = 5 pF, f = 1 MHz	Room		- 56		dB
Crosstalk[d]	X_{TALK}		Room		- 89		
NO, NC Off Capacitance[d]	$C_{NO(off)}$ $C_{NC(off)}$	V+ = 3.6 V, V_{IN} = 0 or V+, f = 1 MHz	Room		81		pF
Channel-On Capacitance[d]	C_{ON}		Room		103		
Power Supply							
Power Supply Range	V+			1.5		3.6	V
Power Supply Current	I+	V+ = 3.6 V, V_{IN} = 0 or V+			0.01	1.0	µA

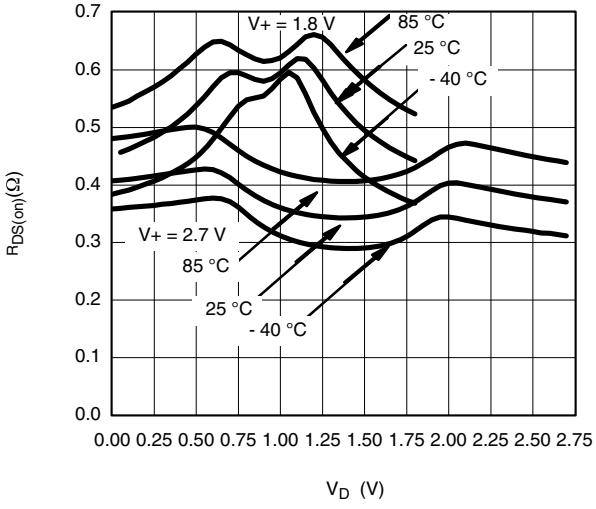
Notes:
a. Room = 25 °C, Full = as determined by the operating suffix.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Typical values are for design aid only, not guaranteed nor subject to production testing.
d. Guarantee by design, nor subjected to production test.
e. V_{IN} = input voltage to perform proper function.
f. Guaranteed by 3 V leakage testing, not production tested.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

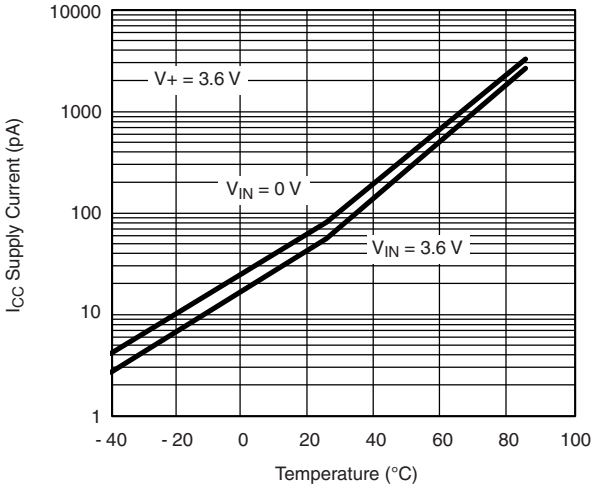
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



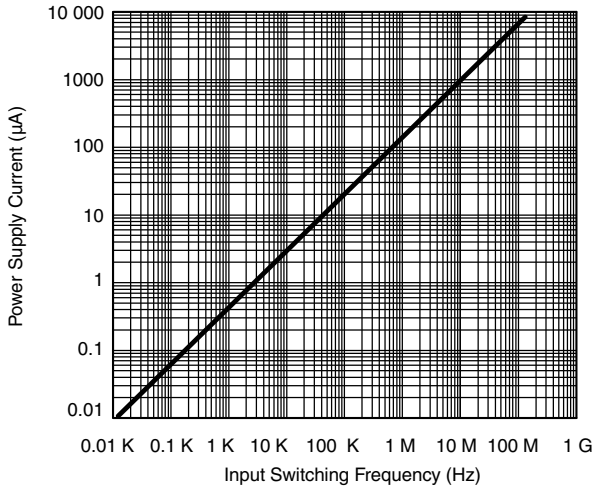
$R_{DS(on)}$ vs. V_{COM} vs. 1 V_{CC}



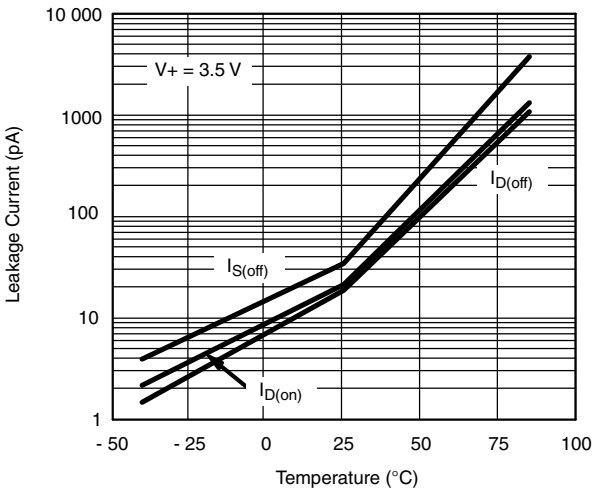
$R_{DS(on)}$ vs. V_D, V_{CC} and Temperature



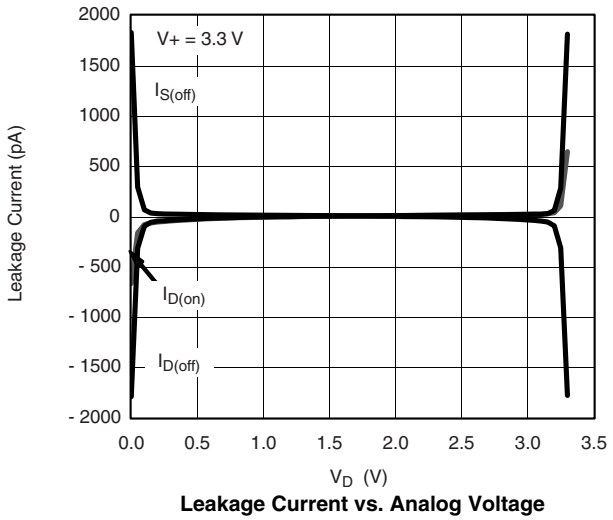
Supply Current vs. Temperature



Switching Frequency vs. Supply Current

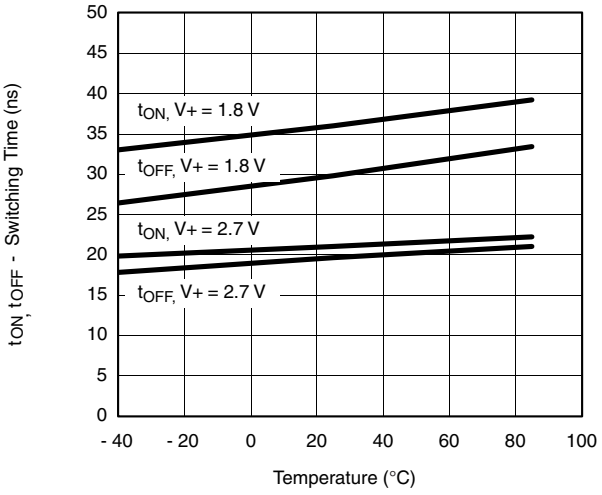


Leakage Current vs. Temperature

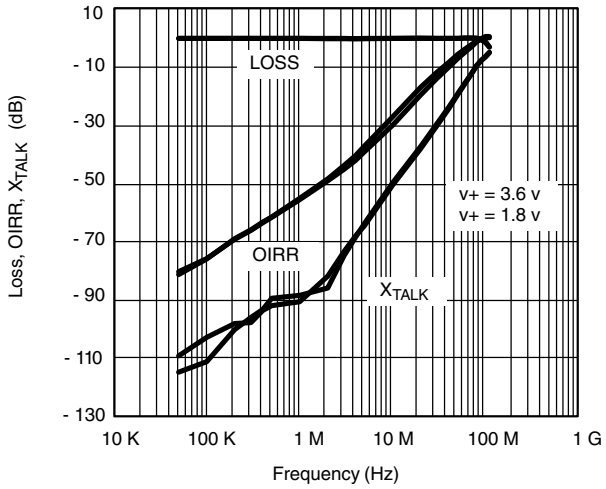


Leakage Current vs. Analog Voltage

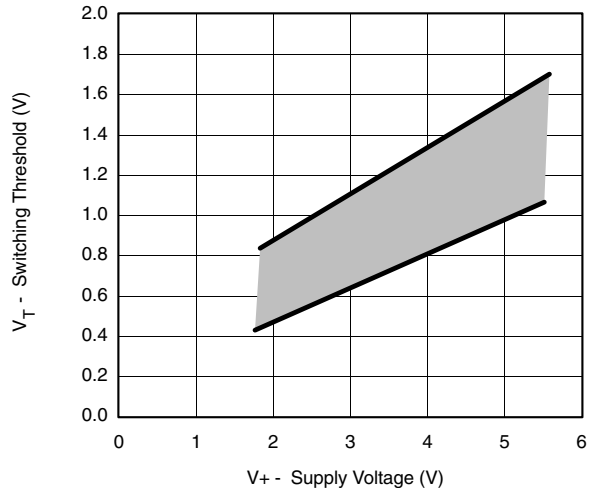
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



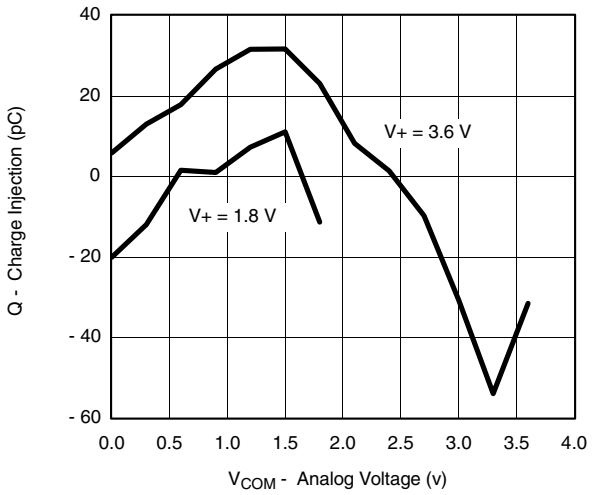
Switching Time vs. V_{CC} and Temperature



Insertion Loss, Off -Isolation Crosstalk vs. Frequency

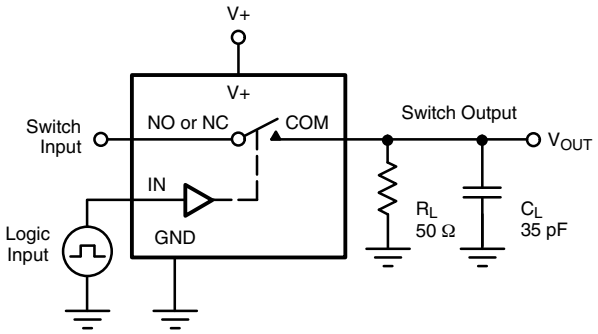


Switching Threshold vs. Supply Voltage



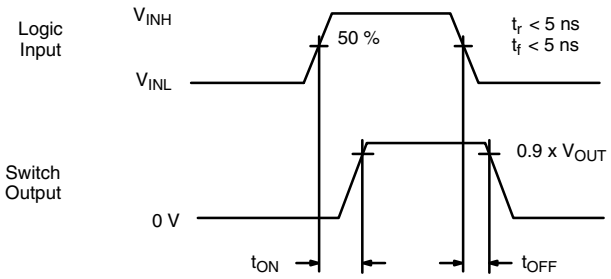
Charge Injection vs. Analog Voltage

TEST CIRCUITS



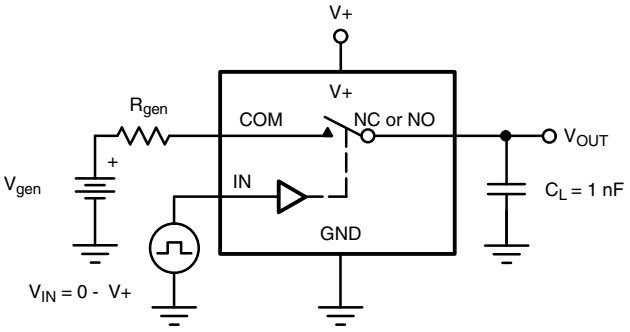
C_L (includes fixture and stray capacitance)

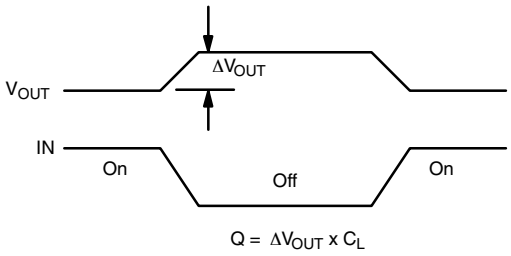
$$V_{OUT} = V_{COM}\left(\frac{R_L}{R_L + R_{ON}}\right)$$



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

Figure 1. Switching Time

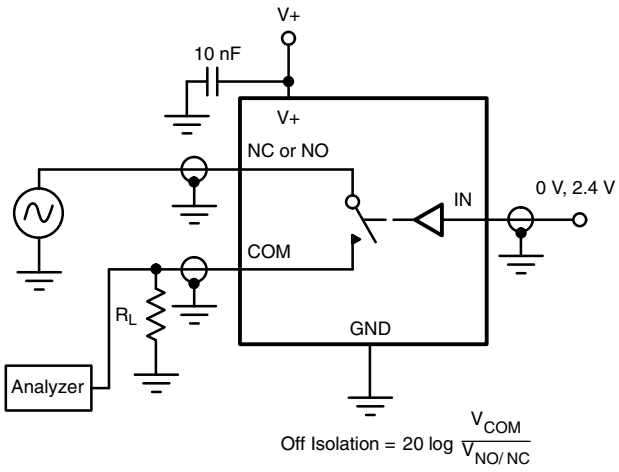




$Q = \Delta V_{OUT} \times C_L$

IN depends on switch configuration: input polarity determined by sense of switch.

Figure 2.Charge Injection



Off Isolation = 20 log $\frac{V_{COM}}{V_{NO/NC}}$

Figure 3. Off-Isolation

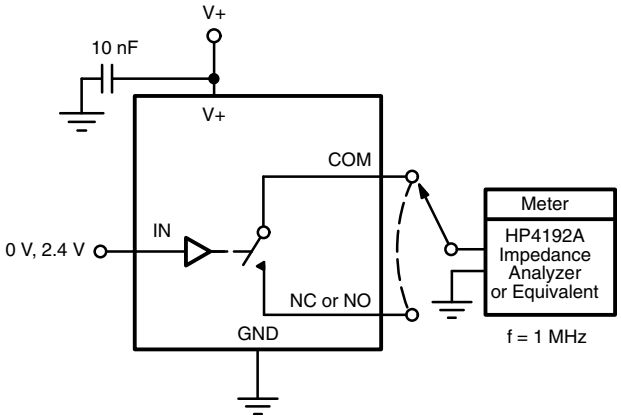
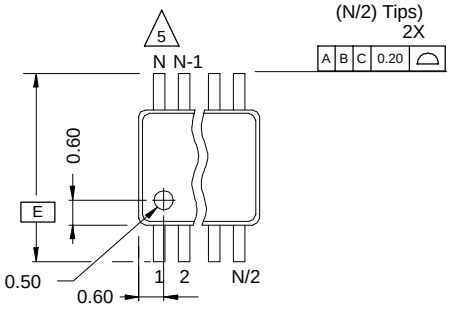


Figure 4. Channel Off/On Capacitance

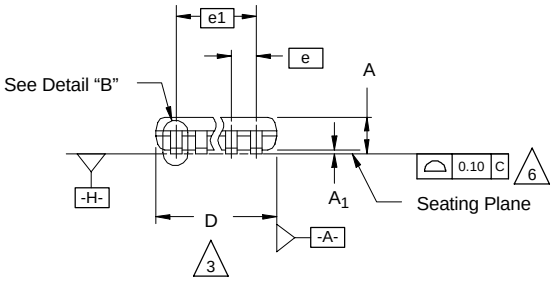
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?72708.

MSOP: 8-LEADS

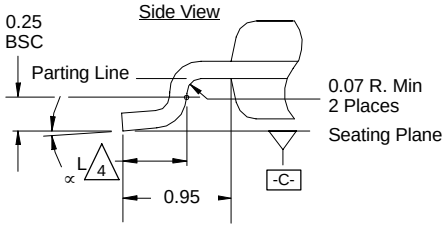
JEDEC Part Number: MO-187, (Variation AA and BA)



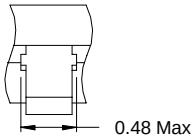
Top View



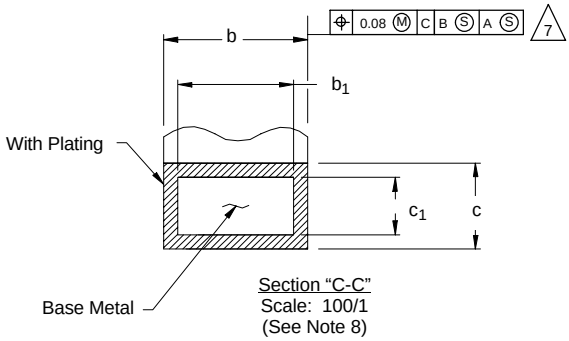
Side View



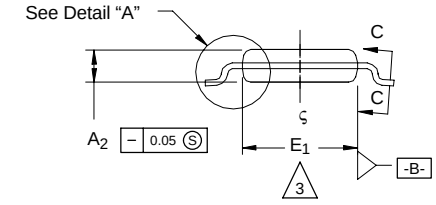
Detail "A"
(Scale: 30/1)



Detail "B"
(Scale: 30/1)
Dambar Protrusion



Section "C-C"
Scale: 100/1
(See Note 8)



End View

NOTES:

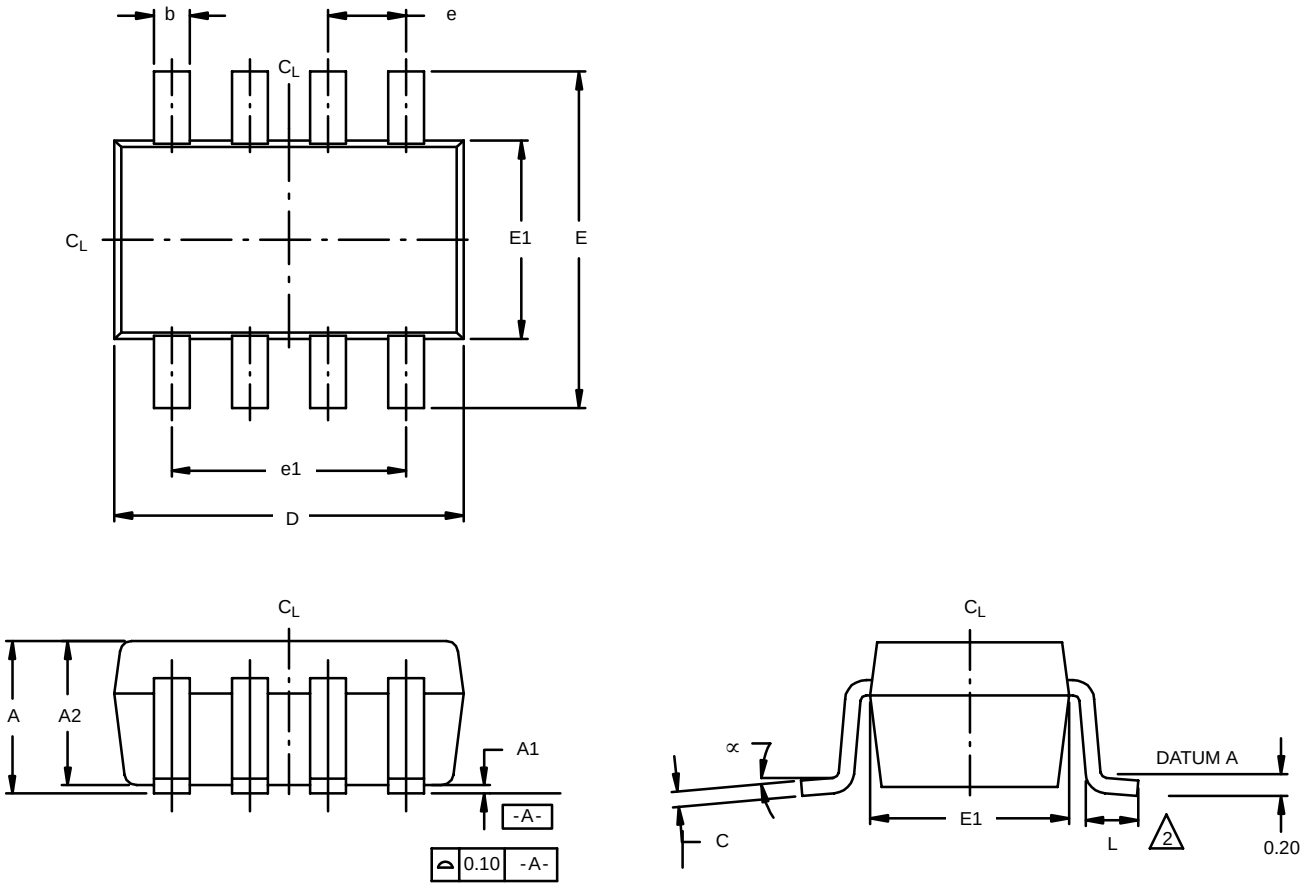
1. Die thickness allowable is 0.203 ± 0.0127.
2. Dimensioning and tolerances per ANSI.Y14.5M-1994.
3. Dimensions "D" and "E_1" do not include mold flash or protrusions, and are measured at Datum plane -H- , mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimension is the length of terminal for soldering to a substrate.
5. Terminal positions are shown for reference only.
6. Formed leads shall be planar with respect to one another within 0.10 mm at seating plane.
7. The lead width dimension does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the lead width dimension at maximum material condition. Dambar cannot be located on the lower radius or the lead foot. Minimum space between protrusions and an adjacent lead to be 0.14 mm. See detail "B" and Section "C-C".
8. Section "C-C" to be determined at 0.10 mm to 0.25 mm from the lead tip.
9. Controlling dimension: millimeters.
10. This part is compliant with JEDEC registration MO-187, variation AA and BA.
11. Datums -A- and -B- to be determined Datum plane -H- .
12. Exposed pad area in bottom side is the same as teh leadframe pad size.

N = 8L

Dim	MILLIMETERS			Note
	Min	Nom	Max	
A	-	-	1.10	
A_1	0.05	0.10	0.15	
A_2	0.75	0.85	0.95	
b	0.25	-	0.38	8
b_1	0.25	0.30	0.33	8
c	0.13	-	0.23	
c_1	0.13	0.15	0.18	
D	3.00 BSC			3
E	4.90 BSC			
E_1	2.90	3.00	3.10	3
e	0.65 BSC			
e_1	1.95 BSC			
L	0.40	0.55	0.70	4
N	8			5
∝	0°	4°	6°	

ECN: T-02080—Rev. C, 15-Jul-02
DWG: 5867

SOT-23 : 8-LEAD



NOTES:

1. All dimensions are in millimeters.
2. Foot length measured at intercept point between Datum A and lead surface.
3. Package outline exclusive of mold flash and metal burr.
4. Package outline inclusive of solder plating.
5. No molding flash allowed on the top and bottom lead surface.

Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.90	1.27	1.45	0.035	0.05	0.057
A1	0.00	0.0762	0.15	0.000	0.003	0.006
A2	0.90	1.20	1.30	0.035	0.047	0.051
b	0.22	0.30	0.38	0.009	0.012	0.015
C	0.09	0.152	0.20	0.004	0.006	0.008
D	2.80	2.9	3.00	0.11	0.114	0.118
E	2.60	2.8	23.00	0.102	0.11	0.118
E1	1.50	1.65	1.75	0.059	0.065	0.069
e	0.65 REF			0.026 REF		
e1	1.95 REF			0.077 REF		
L	0.35	0.45	0.55	0.014	0.018	0.022
∝	0°	4°	8°	0°	4°	8°

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