

SN54ALS74A, SN54AS74A, SN74ALS74A, SN74AS74A DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

SDAS143C – APRIL 1982 – REVISED AUGUST 1995

- Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

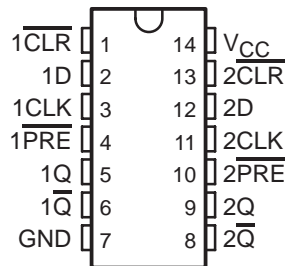
TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY ($C_L = 50$ pF) (MHz)	TYPICAL POWER DISSIPATION PER FLIP-FLOP (mW)
'ALS74A	50	6
'AS74A	134	26

description

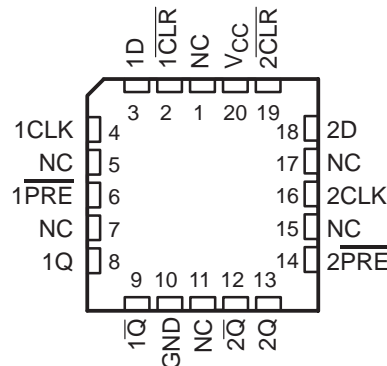
These devices contain two independent positive-edge-triggered D-type flip-flops. A low level at the preset (\overline{PRE}) or clear (\overline{CLR}) inputs sets or resets the outputs regardless of the levels of the other inputs. When \overline{PRE} and \overline{CLR} are inactive (high), data at the data (D) input meeting the setup-time requirements are transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of CLK. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

The SN54ALS74A and SN54AS74A are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS74A and SN74AS74A are characterized for operation from 0°C to 70°C .

SN54ALS74A, SN54AS74A . . . J PACKAGE
SN74ALS74A, SN74AS74A . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS74A, SN54AS74A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE

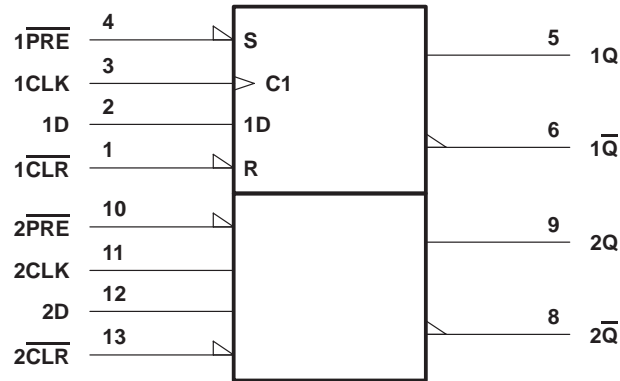
INPUTS				OUTPUTS	
\overline{PRE}	\overline{CLR}	CLK	D	Q	\overline{Q}
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H [†]	H [†]
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q ₀	\overline{Q}_0

[†]The output levels in this configuration are not specified to meet the minimum levels for V_{OH} if the lows at \overline{PRE} and \overline{CLR} are near V_{IL} maximum. Furthermore, this configuration is nonstable; that is, it does not persist when \overline{PRE} or \overline{CLR} returns to its inactive (high) level.

SN54ALS74A, SN54AS74A, SN74ALS74A, SN74AS74A DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

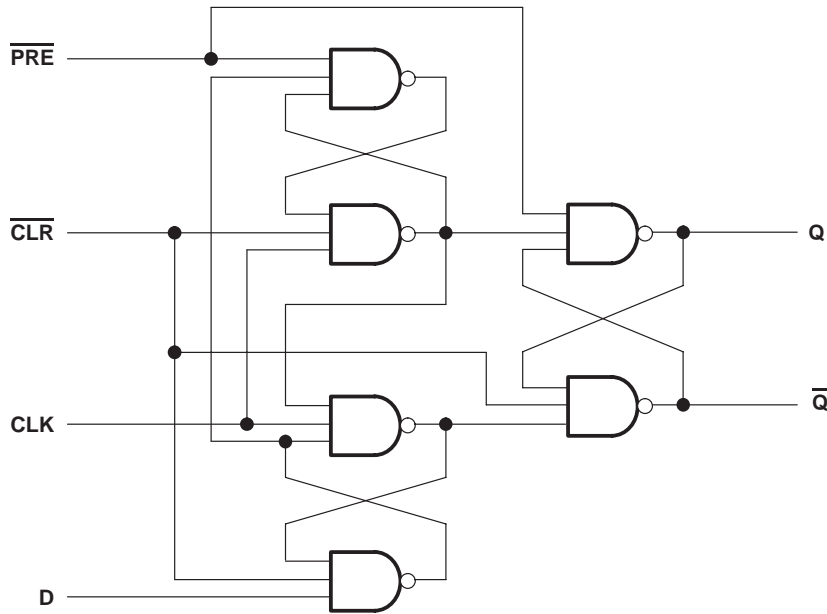
SDAS143C – APRIL 1982 – REVISED AUGUST 1995

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, J, and N packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Operating free-air temperature range, T_A : SN54ALS74A	-55°C to 125°C
SN74ALS74A	0°C to 70°C
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

SN54ALS74A, SN54AS74A, SN74ALS74A, SN74AS74A DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

SDAS143C – APRIL 1982 – REVISED AUGUST 1995

recommended operating conditions

		SN54ALS74A			SN74ALS74A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			-0.4			-0.4	mA
I_{OL}	Low-level output current			4			8	mA
f_{clock}	Clock frequency	0		25	0		34	MHz
t_w	Pulse duration	\overline{PRE} or \overline{CLR} low		15	15		ns	
		CLK high		17.5	14.5			
		CLK low		17.5	14.5			
t_{su}	Setup time before CLK \uparrow	Data		16	15		ns	
		\overline{PRE} or \overline{CLR} inactive		10	10			
t_h	Hold time after CLK \uparrow	Data		2	0		ns	
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS74A		SN74ALS74A		UNIT
				MIN	TYP \dagger	MAX	MIN	
V_{IK}		$V_{CC} = 4.5\text{ V}$,	$I_I = -18\text{ mA}$		-1.5		-1.5	V
V_{OH}		$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$,	$I_{OH} = -2\text{ mA}$	$V_{CC}-2$		$V_{CC}-2$		V
V_{OL}		$V_{CC} = 4.5\text{ V}$	$I_{OL} = 4\text{ mA}$	0.25	0.4	0.25	0.4	V
			$I_{OL} = 8\text{ mA}$			0.35	0.5	
I_I	CLK or D	$V_{CC} = 4.5\text{ V}$,	$V_I = 7\text{ V}$		0.1		0.1	mA
	\overline{PRE} or \overline{CLR}				0.2		0.2	
I_{IH}	CLK or D	$V_{CC} = 4.5\text{ V}$,	$V_I = 2.7\text{ V}$		20		20	μA
	\overline{PRE} or \overline{CLR}				40		40	
I_{IL}	CLK or D	$V_{CC} = 4.5\text{ V}$,	$V_I = 0.4\text{ V}$		-0.2		-0.2	mA
	\overline{PRE} or \overline{CLR}				-0.4		-0.4	
$I_{O\ddagger}$		$V_{CC} = 5.5\text{ V}$,	$V_O = 2.25\text{ V}$	-20	-112	-30	-112	mA
I_{CC}		$V_{CC} = 5.5\text{ V}$,	See Note 1	2.4	4	2.4	4	mA

\dagger All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

\ddagger The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

NOTE 1: I_{CC} is measured with D, CLK, and \overline{PRE} grounded, then with D, CLK, and \overline{CLR} grounded.



SN54ALS74A, SN54AS74A, SN74ALS74A, SN74AS74A DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

SDAS143C – APRIL 1982 – REVISED AUGUST 1995

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX†				UNIT
			SN54ALS74A		SN74ALS74A		
			MIN	MAX	MIN	MAX	
f _{max}			25		34		MHz
t _{PLH}	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$	3	18	3	13	ns
t _{PHL}			5	17	5	15	
t _{PLH}	CLK	Q or $\overline{\text{Q}}$	5	23	5	16	ns
t _{PHL}			5	20	5	18	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V _{CC}	7 V
Input voltage, V _I	7 V
Operating free-air temperature range, T _A : SN54AS74A	-55°C to 125°C
SN74AS74A	0°C to 70°C
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54AS74A			SN74AS74A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
I _{OH}	High-level output current			-2			-2	mA
I _{OL}	Low-level output current			20			20	mA
f _{clock} *	Clock frequency	0		90	0		105	MHz
t _w *	Pulse duration	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low		4		4		ns
		CLK high		4		4		
		CLK low		5.5		5.5		
t _{su} *	Setup time before CLK↑	Data		4.5		4.5		ns
		$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive		2		2		
t _h *	Hold time after CLK↑	Data		0		0		ns
T _A	Operating free-air temperature	-55		125	0		70	°C

* On products compliant to MIL-STD-833, Class B, this parameter is based on characterization data but is not production tested.



SN54ALS74A, SN54AS74A, SN74ALS74A, SN74AS74A DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

SDAS143C – APRIL 1982 – REVISED AUGUST 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54AS74A		SN74AS74A		UNIT	
			MIN	TYP†	MAX	MIN		TYP†
V _{IK}		V _{CC} = 4.5 V, I _I = -18 mA			-1.2		-1.2	V
V _{OH}		V _{CC} = 4.5 V to 5.5 V, I _{OH} = -2 mA	V _{CC} -2		V _{CC} -2			V
V _{OL}		V _{CC} = 4.5 V, I _{OL} = 20 mA	0.25	0.5	0.25	0.5		V
I _I		V _{CC} = 5.5 V, V _I = 7 V		0.1		0.1		mA
I _{IH}	CLK or D	V _{CC} = 5.5 V, V _I = 2.7 V		20		20		μA
	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$			40		40		
I _{IL}	CLK or D	V _{CC} = 5.5 V, V _I = 0.4 V		-0.5		-0.5		mA
	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$			-1.8		-1.8		
I _O ‡		V _{CC} = 5.5 V, V _O = 2.25 V	-30	-112	-30	-112		mA
I _{CC}		V _{CC} = 5.5 V, See Note 1	10.5	16	10.5	16		mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

NOTE 1: I_{CC} is measured with D, CLK, and $\overline{\text{PRE}}$ grounded, then with D, CLK, and $\overline{\text{CLR}}$ grounded.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX§				UNIT
			SN54AS74A		SN74AS74A		
			MIN	MAX	MIN	MAX	
f _{max} *			90		105	MHz	
t _{PLH}	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$	2	9	2	7.5	ns
t _{PHL}			2.5	11.5	2.5	10.5	
t _{PLH}	CLK	Q or $\overline{\text{Q}}$	2.5	10	3	8	ns
t _{PHL}			3.5	10.5	3	9	

* On products compliant to MIL-STD-833, Class B, this parameter is based on characterization data but is not production tested.

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



SN54ALS74A, SN54AS74A, SN74ALS74A, SN74AS74A DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

SDAS143C – APRIL 1982 – REVISED AUGUST 1995

PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9862701QCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-9862701QC A SNJ54AS74AJ	Samples
84011012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	84011012A SNJ54ALS 74AFK	Samples
8401101CA	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	8401101CA SNJ54ALS74AJ	Samples
8401101DA	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	8401101DA SNJ54ALS74AW	Samples
JM38510/37101B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 37101B2A	Samples
JM38510/37101BCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	JM38510/ 37101BCA	Samples
M38510/37101B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 37101B2A	Samples
M38510/37101BCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	JM38510/ 37101BCA	Samples
SN54ALS74AJ	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	SN54ALS74AJ	Samples
SN54AS74AJ	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	SN54AS74AJ	Samples
SN74ALS74AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS74A	Samples
SN74ALS74ADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS74A	Samples
SN74ALS74ADRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS74A	Samples
SN74ALS74AN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS74AN	Samples
SN74ALS74ANSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS74A	Samples
SN74AS74AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	AS74A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AS74ADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	AS74A	Samples
SN74AS74AN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	SN74AS74AN	Samples
SN74AS74ANSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	74AS74A	Samples
SNJ54ALS74AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	84011012A SNJ54ALS 74AFK	Samples
SNJ54ALS74AJ	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	8401101CA SNJ54ALS74AJ	Samples
SNJ54ALS74AW	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	8401101DA SNJ54ALS74AW	Samples
SNJ54AS74AJ	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-9862701QC A SNJ54AS74AJ	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54ALS74A, SN54AS74A, SN74ALS74A, SN74AS74A :

- Catalog: [SN74ALS74A](#), [SN74AS74A](#)

- Military: [SN54ALS74A](#), [SN54AS74A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS74ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74ALS74ANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74AS74ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AS74ANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS74ADR	SOIC	D	14	2500	367.0	367.0	38.0
SN74ALS74ANSR	SO	NS	14	2000	367.0	367.0	38.0
SN74AS74ADR	SOIC	D	14	2500	367.0	367.0	38.0
SN74AS74ANSR	SO	NS	14	2000	367.0	367.0	38.0

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J 14

GENERIC PACKAGE VIEW
CDIP - 5.08 mm max height
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

J0014A



PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211283-3/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - (C) Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - (D) The 20 pin end lead shoulder width is a vendor option, either half or full width.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated