

HEF4021B-Q100

8-bit static shift register

Rev. 5 — 1 December 2021

Product data sheet

1. General description

The HEF4021B-Q100 is an 8-bit static shift register (parallel-to-serial converter). It has a synchronous serial data input (DS), a clock input (CP) and an asynchronous active HIGH parallel load input (PL). The HEF4021B-Q100 also has eight asynchronous parallel data inputs (D0 to D7) and buffered parallel outputs from the last three stages (Q5 to Q7). Each register stage is a D-type master-slave flip-flop with a set direct (SD) and clear direct (CD) input. Information on D0 to D7 is asynchronously loaded into the register while PL is HIGH, independent of CP and DS. When PL is LOW, data on DS is shifted into the first register position. All the data in the register is shifted one position to the right on the LOW-to-HIGH transition of CP. Schmitt trigger action makes the clock input highly tolerant of slower rise and fall times.

The device operates over a recommended V_{DD} power supply range of 3 V to 15 V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD} , V_{SS} , or another input.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 3.0 V to 15.0 V
- CMOS low power dissipation
- High noise immunity
- Tolerant of slower rise and fall times
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- ESD protection:
 - MIL-STD-883, method 3015 exceeds 2000 V
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)
- Complies with JEDEC standard JESD 13-B

3. Ordering information

Table 1. Ordering information

| Type number | Package | | | |
|-----------------|-------------------|---------|--|----------|
| | Temperature range | Name | Description | Version |
| HEF4021BT-Q100 | -40 °C to +125 °C | SO16 | plastic small outline package; 16 leads; body width 3.9 mm | SOT109-1 |
| HEF4021BTT-Q100 | -40 °C to +125 °C | TSSOP16 | plastic thin shrink small outline package; 16 leads; body width 4.4 mm | SOT403-1 |

4. Functional diagram

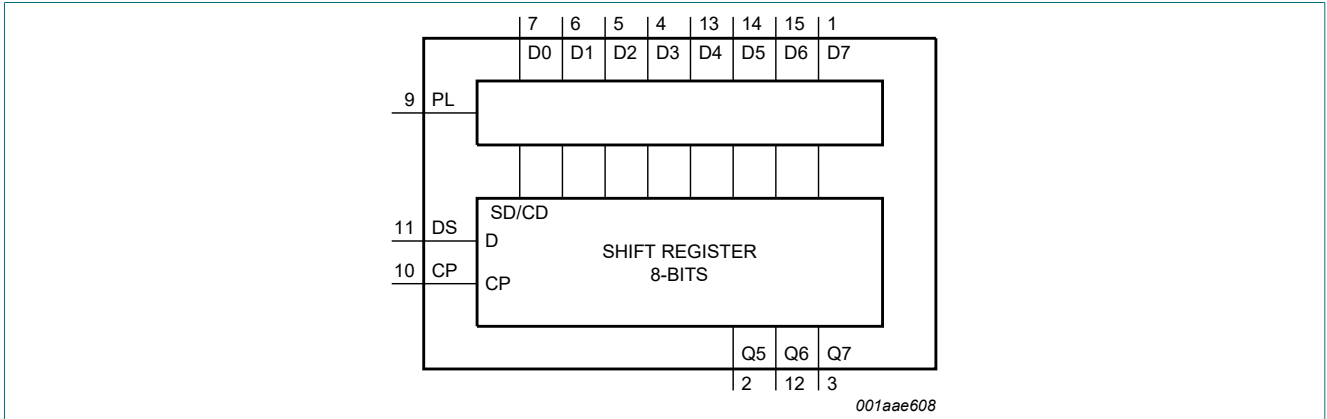


Fig. 1. Functional diagram

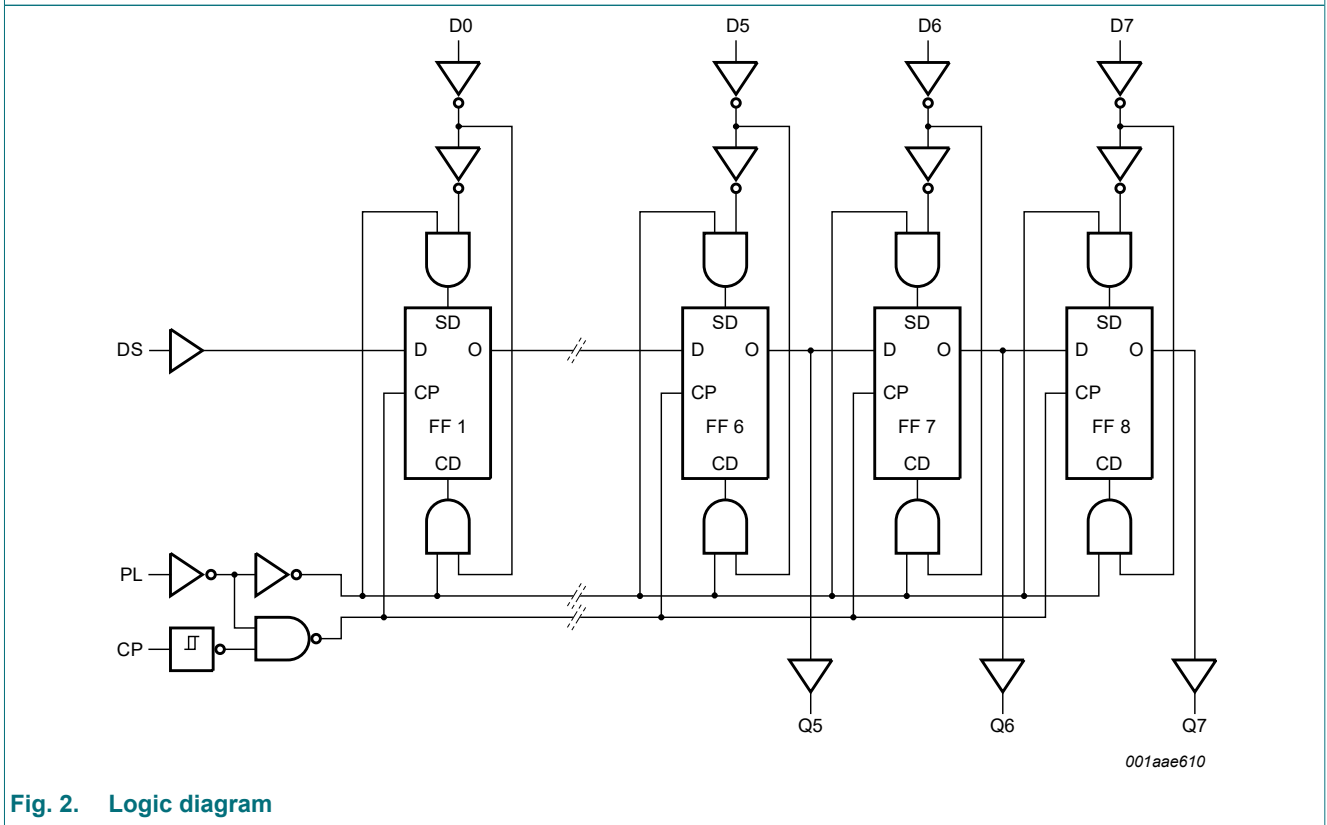


Fig. 2. Logic diagram

5. Pinning information

5.1. Pinning

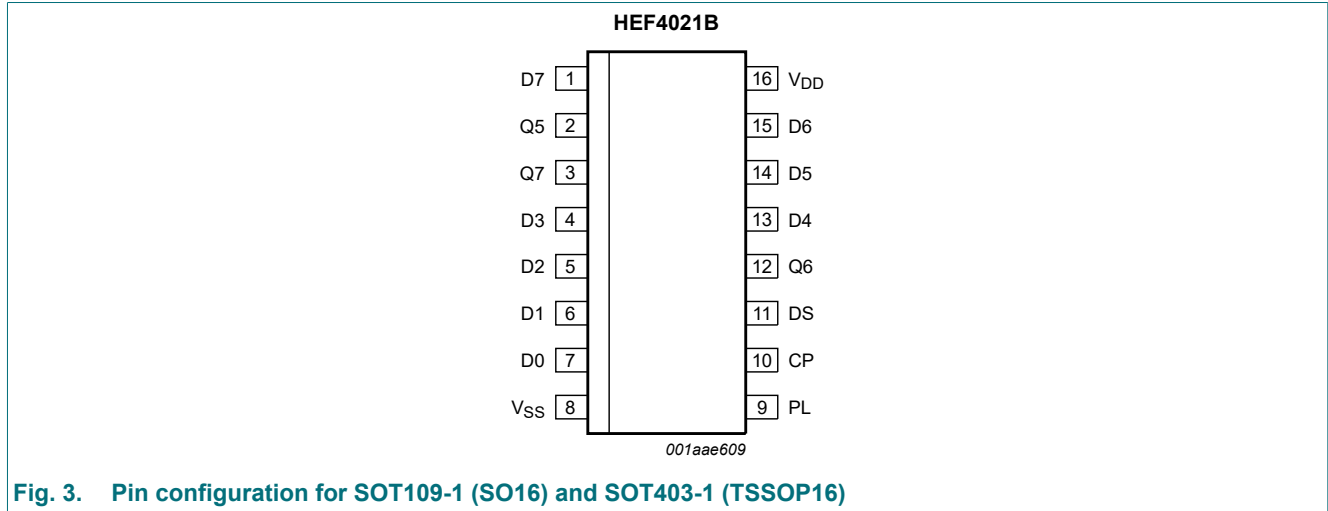


Fig. 3. Pin configuration for SOT109-1 (SO16) and SOT403-1 (TSSOP16)

5.2. Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|--------------------------------|---------------------------|---|
| Q5, Q6, Q7 | 2, 12, 3 | buffered parallel output from the last three stages |
| D0, D1, D2, D3, D4, D5, D6, D7 | 7, 6, 5, 4, 13, 14, 15, 1 | parallel data input |
| V _{SS} | 8 | ground supply voltage |
| PL | 9 | parallel load input |
| CP | 10 | clock input (LOW-to-HIGH edge-triggered) |
| DS | 11 | serial data input |
| V _{DD} | 16 | supply voltage |

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care;

↑ = LOW to HIGH clock transition; ↓ = HIGH to LOW clock transition;

data n = data (HIGH or LOW) on the DS input at the nth ↑ CP transition.

| Number of clock transitions | Inputs | | | Outputs | | |
|-----------------------------|--------|--------|----|-----------|-----------|-----------|
| | CP | DS | PL | Q5 | Q6 | Q7 |
| Serial operation | | | | | | |
| 1 | ↑ | data 1 | L | X | X | X |
| 2 | ↑ | data 2 | L | X | X | X |
| 3 | ↑ | data 3 | L | X | X | X |
| 6 | ↑ | X | L | data 1 | X | X |
| 7 | ↑ | X | L | data 2 | data 1 | X |
| 8 | ↑ | X | L | data 3 | data 2 | data 1 |
| | ↓ | X | L | no change | no change | no change |
| Parallel operation | | | | | | |
| | X | X | H | D5 | D6 | D7 |

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|-------------------------|---|------|-----------------------|------|
| V _{DD} | supply voltage | | -0.5 | +18 | V |
| I _{IK} | input clamping current | V _I < -0.5 V or V _I > V _{DD} + 0.5 V | - | ±10 | mA |
| V _I | input voltage | | -0.5 | V _{DD} + 0.5 | V |
| I _{OK} | output clamping current | V _O < -0.5 V or V _O > V _{DD} + 0.5 V | - | ±10 | mA |
| I _{I/O} | input/output current | | - | ±10 | mA |
| I _{DD} | supply current | | - | 50 | mA |
| T _{stg} | storage temperature | | -65 | +150 | °C |
| T _{amb} | ambient temperature | | -40 | +125 | °C |
| P _{tot} | total power dissipation | T _{amb} -40 °C to +125 °C [1] | - | 500 | mW |
| P | power dissipation | per output | - | 100 | mW |

- [1] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|-------------------------------------|------------------------|-----|-----|----------|-----------------|
| V_{DD} | supply voltage | | 3 | - | 15 | V |
| V_I | input voltage | | 0 | - | V_{DD} | V |
| T_{amb} | ambient temperature | in free air | -40 | - | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{DD} = 5\text{ V}$ | - | - | 3.75 | $\mu\text{s/V}$ |
| | | $V_{DD} = 10\text{ V}$ | - | - | 0.5 | $\mu\text{s/V}$ |
| | | $V_{DD} = 15\text{ V}$ | - | - | 0.08 | $\mu\text{s/V}$ |

9. Static characteristics

Table 6. Static characteristics

$V_{SS} = 0\text{ V}$; $V_I = V_{SS}$ or V_{DD} unless otherwise specified.

| Symbol | Parameter | Conditions | V_{DD} | $T_{amb} = -40\text{ °C}$ | | $T_{amb} = +25\text{ °C}$ | | $T_{amb} = +85\text{ °C}$ | | $T_{amb} = +125\text{ °C}$ | | Unit |
|----------|---------------------------|--------------------------|----------|---------------------------|-----------|---------------------------|-----------|---------------------------|-----------|----------------------------|-----------|---------------|
| | | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| V_{IH} | HIGH-level input voltage | $ I_O < 1\ \mu\text{A}$ | 5 V | 3.5 | - | 3.5 | - | 3.5 | - | 3.5 | - | V |
| | | | 10 V | 7.0 | - | 7.0 | - | 7.0 | - | 7.0 | - | V |
| | | | 15 V | 11.0 | - | 11.0 | - | 11.0 | - | 11.0 | - | V |
| V_{IL} | LOW-level input voltage | $ I_O < 1\ \mu\text{A}$ | 5 V | - | 1.5 | - | 1.5 | - | 1.5 | - | 1.5 | V |
| | | | 10 V | - | 3.0 | - | 3.0 | - | 3.0 | - | 3.0 | V |
| | | | 15 V | - | 4.0 | - | 4.0 | - | 4.0 | - | 4.0 | V |
| V_{OH} | HIGH-level output voltage | $ I_O < 1\ \mu\text{A}$ | 5 V | 4.95 | - | 4.95 | - | 4.95 | - | 4.95 | - | V |
| | | | 10 V | 9.95 | - | 9.95 | - | 9.95 | - | 9.95 | - | V |
| | | | 15 V | 14.95 | - | 14.95 | - | 14.95 | - | 14.95 | - | V |
| V_{OL} | LOW-level output voltage | $ I_O < 1\ \mu\text{A}$ | 5 V | - | 0.05 | - | 0.05 | - | 0.05 | - | 0.05 | V |
| | | | 10 V | - | 0.05 | - | 0.05 | - | 0.05 | - | 0.05 | V |
| | | | 15 V | - | 0.05 | - | 0.05 | - | 0.05 | - | 0.05 | V |
| I_{OH} | HIGH-level output current | $V_O = 2.5\text{ V}$ | 5 V | - | -1.7 | - | -1.4 | - | -1.1 | - | -1.1 | mA |
| | | $V_O = 4.6\text{ V}$ | 5 V | - | -0.64 | - | -0.5 | - | -0.36 | - | -0.36 | mA |
| | | $V_O = 9.5\text{ V}$ | 10 V | - | -1.6 | - | -1.3 | - | -0.9 | - | -0.9 | mA |
| | | $V_O = 13.5\text{ V}$ | 15 V | - | -4.2 | - | -3.4 | - | -2.4 | - | -2.4 | mA |
| I_{OL} | LOW-level output current | $V_O = 0.4\text{ V}$ | 5 V | 0.64 | - | 0.5 | - | 0.36 | - | 0.36 | - | mA |
| | | $V_O = 0.5\text{ V}$ | 10 V | 1.6 | - | 1.3 | - | 0.9 | - | 0.9 | - | mA |
| | | $V_O = 1.5\text{ V}$ | 15 V | 4.2 | - | 3.4 | - | 2.4 | - | 2.4 | - | mA |
| I_I | input leakage current | $V_{DD} = 15\text{ V}$ | 15 V | - | ± 0.1 | - | ± 0.1 | - | ± 1.0 | - | ± 1.0 | μA |
| I_{DD} | supply current | $I_O = 0\text{ A}$ | 5 V | - | 5 | - | 5 | - | 150 | - | 150 | μA |
| | | | 10 V | - | 10 | - | 10 | - | 300 | - | 300 | μA |
| | | | 15 V | - | 20 | - | 20 | - | 600 | - | 600 | μA |
| C_I | input capacitance | | - | - | - | 7.5 | - | - | - | - | pF | |

10. Dynamic characteristics

Table 7. Dynamic characteristics

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ °C}$ unless otherwise specified; for test circuit see Fig. 7.

| Symbol | Parameter | Conditions | V _{DD} | Extrapolation formula[1] | Min | Typ | Max | Unit |
|------------------|-------------------------------|--|-----------------|------------------------------------|-----|-----|-----|------|
| t _{PHL} | HIGH to LOW propagation delay | CP to Qn; see Fig. 4 | 5 V | 98 ns + (0.55 ns/pF)C _L | - | 125 | 250 | ns |
| | | | 10 V | 44 ns + (0.23 ns/pF)C _L | - | 55 | 110 | ns |
| | | | 15 V | 32 ns + (0.16 ns/pF)C _L | - | 40 | 80 | ns |
| | | PL to Qn; see Fig. 4 | 5 V | 93 ns + (0.55 ns/pF)C _L | - | 120 | 240 | ns |
| | | | 10 V | 44 ns + (0.23 ns/pF)C _L | - | 55 | 110 | ns |
| | | | 15 V | 32 ns + (0.16 ns/pF)C _L | - | 40 | 80 | ns |
| t _{PLH} | LOW to HIGH propagation delay | CP to Qn; see Fig. 4 | 5 V | 88 ns + (0.55 ns/pF)C _L | - | 115 | 230 | ns |
| | | | 10 V | 39 ns + (0.23 ns/pF)C _L | - | 50 | 100 | ns |
| | | | 15 V | 32 ns + (0.16 ns/pF)C _L | - | 40 | 80 | ns |
| | | PL to Qnl; see Fig. 4 | 5 V | 78 ns + (0.55 ns/pF)C _L | - | 105 | 210 | ns |
| | | | 10 V | 39 ns + (0.23 ns/pF)C _L | - | 50 | 100 | ns |
| | | | 15 V | 32 ns + (0.16 ns/pF)C _L | - | 40 | 80 | ns |
| t _t | transition time | Qn; see Fig. 4 | 5 V | 10 ns + (1.00 ns/pF)C _L | - | 60 | 120 | ns |
| | | | 10 V | 9 ns + (0.42 ns/pF)C _L | - | 30 | 60 | ns |
| | | | 15 V | 6 ns + (0.28 ns/pF)C _L | - | 20 | 40 | ns |
| t _{su} | set-up time | DS to CP; see Fig. 5 | 5 V | | +25 | -15 | - | ns |
| | | | 10 V | | +25 | -10 | - | ns |
| | | | 15 V | | +15 | -5 | - | ns |
| | | Dn to PL; see Fig. 6 | 5 V | | 50 | 25 | - | ns |
| | | | 10 V | | 30 | 10 | - | ns |
| | | | 15 V | | 20 | 5 | - | ns |
| t _h | hold time | DS to CP; see Fig. 5 | 5 V | | 40 | 20 | - | ns |
| | | | 10 V | | 20 | 10 | - | ns |
| | | | 15 V | | 15 | 8 | - | ns |
| | | Dn to PL; see Fig. 6 | 5 V | | +15 | -10 | - | ns |
| | | | 10 V | | 15 | 0 | - | ns |
| | | | 15 V | | 15 | 0 | - | ns |
| t _w | pulse width | CP = LOW; minimum width; see Fig. 5 | 5 V | | 70 | 35 | - | ns |
| | | | 10 V | | 30 | 15 | - | ns |
| | | | 15 V | | 24 | 12 | - | ns |
| | | PL = HIGH; minimum width; see Fig. 6 | 5 V | | 70 | 35 | - | ns |
| | | | 10 V | | 30 | 15 | - | ns |
| | | | 15 V | | 24 | 12 | - | ns |
| t _{rec} | recovery time | PL input; see Fig. 6 | 5 V | | 50 | 10 | - | ns |
| | | | 10 V | | 40 | 5 | - | ns |
| | | | 15 V | | 35 | 5 | - | ns |

| Symbol | Parameter | Conditions | V _{DD} | Extrapolation formula[1] | Min | Typ | Max | Unit |
|-----------------------|-------------------------|----------------------|-----------------|--------------------------|-----|-----|-----|------|
| f _{clk(max)} | maximum clock frequency | CP input; see Fig. 5 | 5 V | | 6 | 13 | - | MHz |
| | | | 10 V | | 15 | 30 | - | MHz |
| | | | 15 V | | 20 | 40 | - | MHz |

[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C_L in pF).

Table 8. Dynamic power dissipation P_D

P_D can be calculated from the formulas shown. V_{SS} = 0 V; t_r = t_f ≤ 20 ns; T_{amb} = 25 °C.

| Symbol | Parameter | V _{DD} | Typical formula for P _D (μW) | where: |
|----------------|---------------------------|-----------------|---|--|
| P _D | dynamic power dissipation | 5 V | $P_D = 900 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ | f _i = input frequency in MHz f _o = output frequency in MHz C _L = output load capacitance in pF V _{DD} = supply voltage in V Σ(f _o × C _L) = sum of the outputs |
| | | 10 V | $P_D = 4300 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ | |
| | | 15 V | $P_D = 12000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ | |

10.1. Waveforms and test circuit

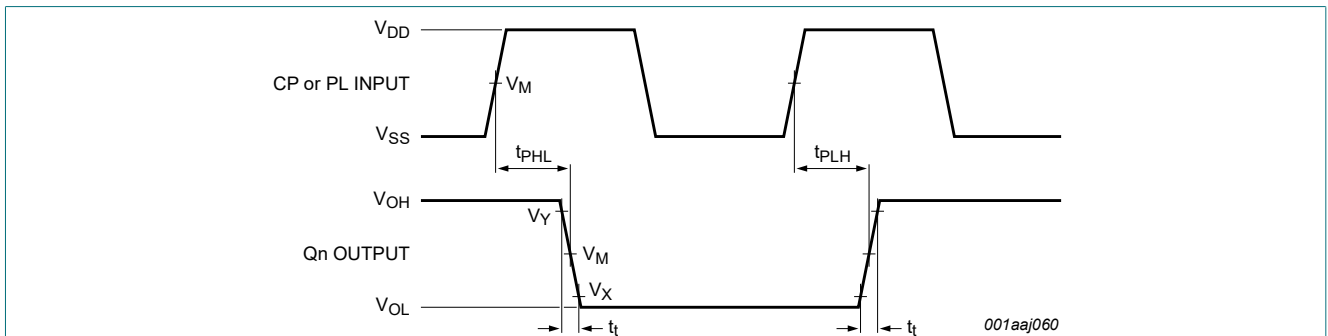


Fig. 4. Waveforms showing propagation delays for CP and PL inputs to Qn output and Qn transition times

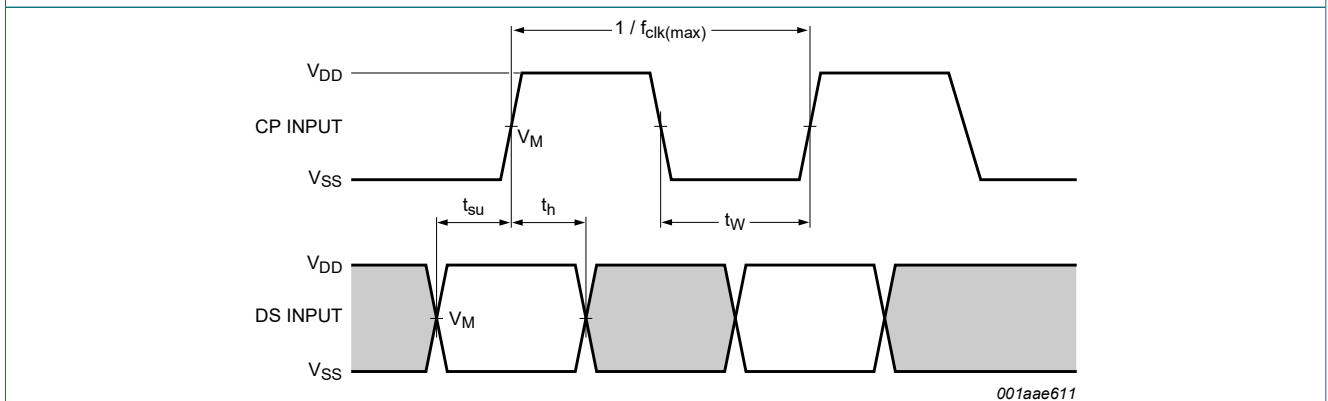
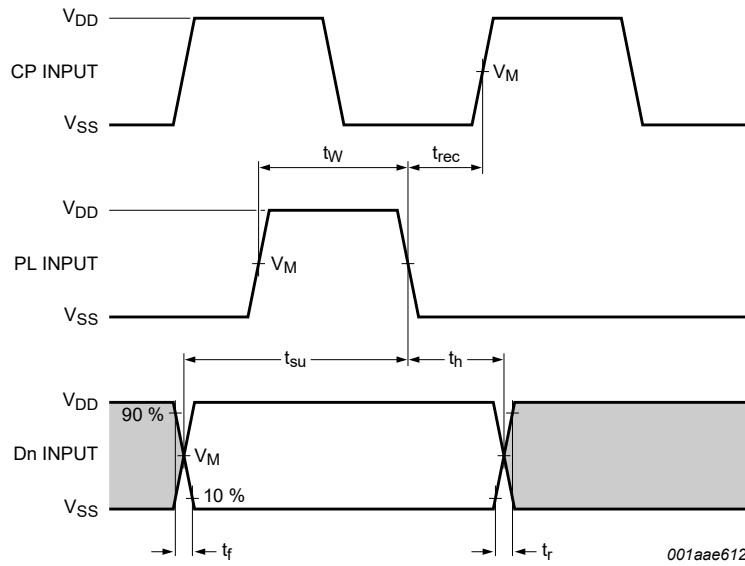


Fig. 5. Waveforms showing minimum clock pulse width, set-up time, and hold time for CP and DS

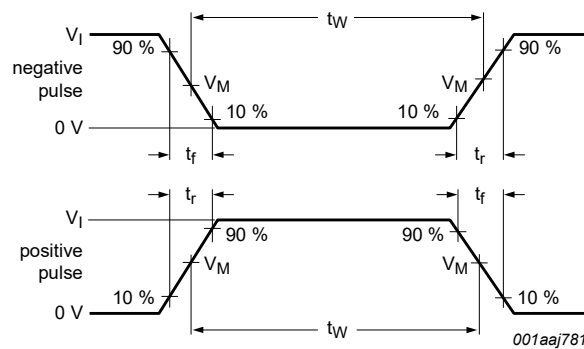


Set-up times and hold times are shown as positive values but may be specified as negative values. Measurement points are given in [Table 9](#).

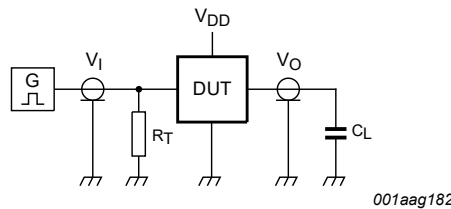
Fig. 6. Waveforms showing minimum pulse width and recovery time for PL; set-up and hold times for Dn to PL

Table 9. Measurement points

| Supply voltage | Input | Output | | |
|----------------|-------------|-------------|-------------|-------------|
| V_{DD} | V_M | V_M | V_X | V_Y |
| 5 V to 15 V | $0.5V_{DD}$ | $0.5V_{DD}$ | $0.1V_{DD}$ | $0.9V_{DD}$ |



a. Input waveform



b. Test circuit

Test data is given in [Table 10](#).

Definitions for test circuit:

C_L = load capacitance including jig and probe capacitance.

R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig. 7. Test circuit for measuring switching times

Table 10. Test data

| Supply voltage | Input | | Load |
|----------------|----------------------|--------------|-------|
| V_{DD} | V_I | t_r, t_f | C_L |
| 5 V to 15 V | V_{SS} or V_{DD} | ≤ 20 ns | 50 pF |

11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

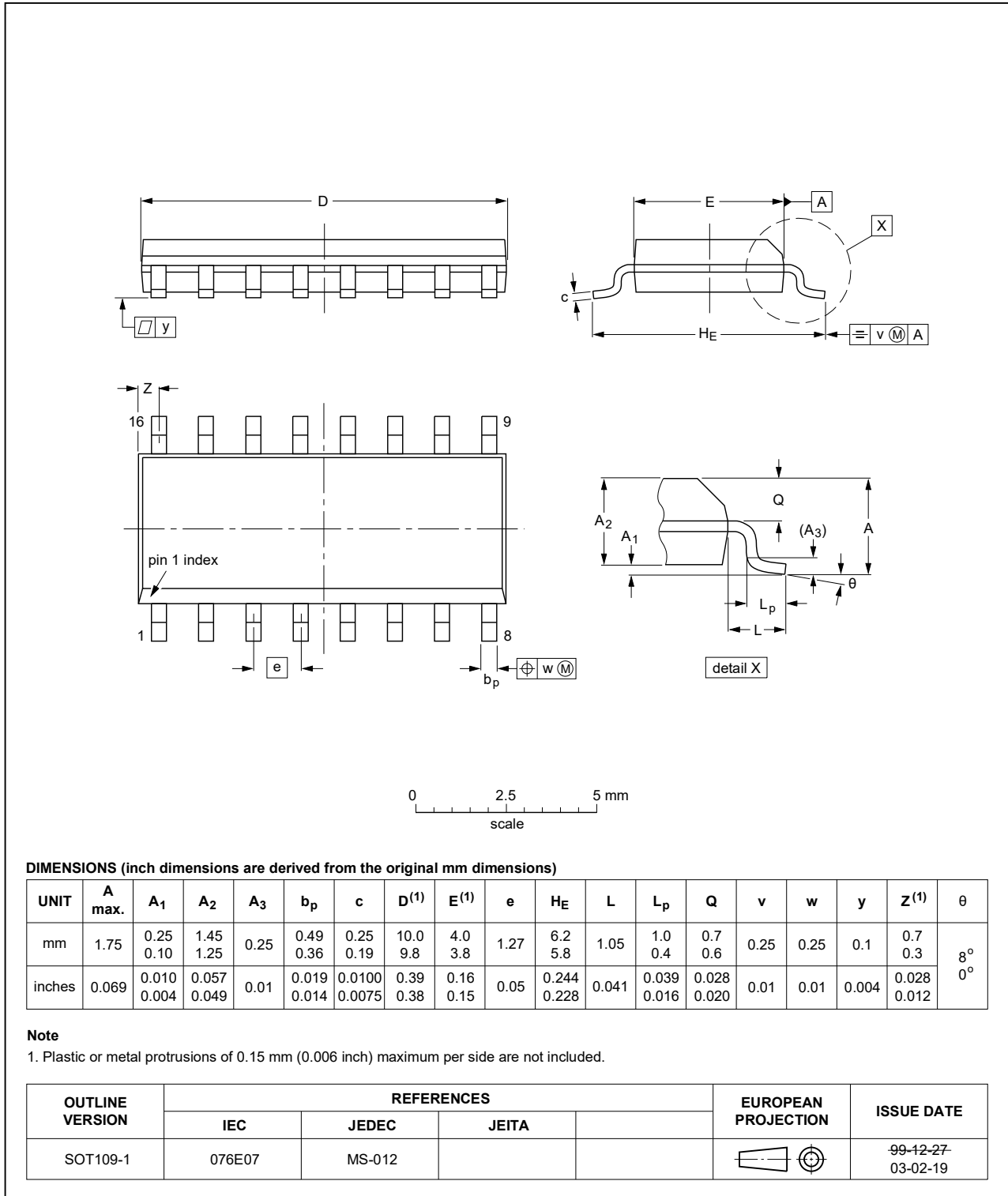


Fig. 8. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

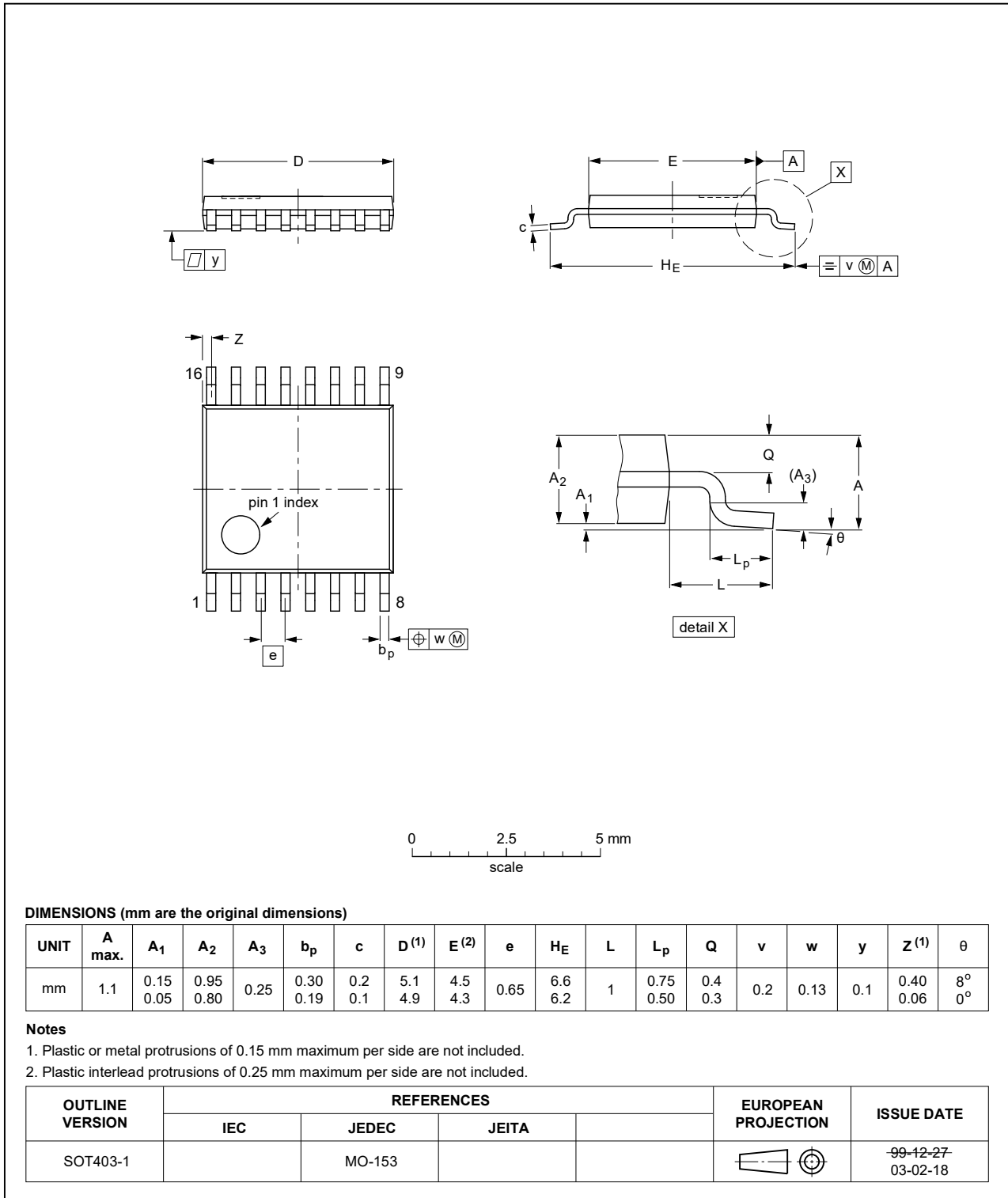


Fig. 9. Package outline SOT403-1 (TSSOP16)

12. Abbreviations

Table 11. Abbreviations

| Acronym | Description |
|---------|---|
| CMOS | Complementary Metal-Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MIL | Military |
| MM | Machine Model |

13. Revision history

Table 12. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|-------------------|---|--------------------|---------------|-------------------|
| HEF4021B_Q100 v.5 | 20211201 | Product data sheet | - | HEF4021B_Q100 v.4 |
| Modifications: | <ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Section 2 updated. Table 4: Derating values for P_{tot} total power dissipation updated. | | | |
| HEF4021B_Q100 v.4 | 20160321 | Product data sheet | - | HEF4021B_Q100 v.3 |
| Modifications: | <ul style="list-style-type: none"> Type number HEF4021BP-Q100 (SOT38-4) removed. | | | |
| HEF4021B_Q100 v.3 | 20130830 | Product data sheet | - | HEF4021B_Q100 v.2 |
| Modifications: | <ul style="list-style-type: none"> HEF4021BTT-Q100 (TSSOP16) added. | | | |
| HEF4021B_Q100 v.2 | 20130220 | Product data sheet | - | HEF4021B_Q100 v.1 |
| Modifications: | <ul style="list-style-type: none"> HEF4021BP-Q100 (DIP16) added. | | | |
| HEF4021B_Q100 v.1 | 20120807 | Product data sheet | - | - |

14. Legal information

Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

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- [2] The term 'short data sheet' is explained in section "Definitions".
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