

### General Description

The SY100EL14V is a low-skew, 1:5 clock distribution chip designed explicitly for low-skew clock distribution applications. The device can be driven by either a differential or single-ended ECL or, if positive power supplies are used, PECL input signal. The EL14V is suitable for operation in systems operating with 3.3V to 5.0V supplies. If a single-ended input is to be used, the  $V_{BB}$  output should be connected to the  $\overline{\text{CLK}}$  input and bypassed to ground via a  $0.01\mu\text{F}$  capacitor. The  $V_{BB}$  output is designed to act as the switching reference for the input of the EL14V under single-ended input conditions. As a result, this pin can only source/sink up to 0.5mA of current.

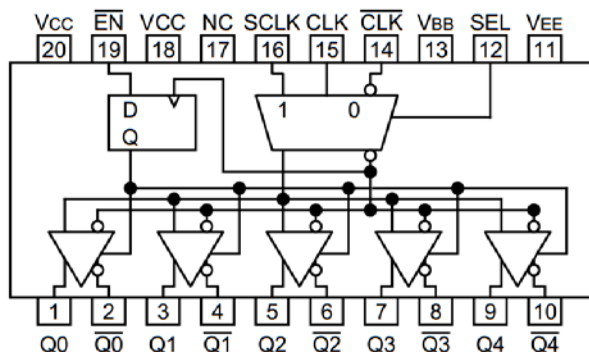
The EL14V features a multiplexed clock input to allow for the distribution of a lower speed scan or test clock along with the high speed system clock. When LOW (or left open and pulled LOW by the input pull-down resistor), the SEL pin will select the differential clock input.

The common enable ( $\overline{\text{EN}}$ ) is synchronous, so that the outputs will only be enabled/disable when they are already in the LOW state. This avoids any chance of generating a runt clock pulse when the device is enabled/disabled as can happen with an asynchronous control. The internal flip-flop is clocked on the falling edge of the input clock. Therefore, all associated specification limits are referenced to the negative edge of the clock input.

When both differential inputs are left open, CLK input will pull down to  $V_{EE}$  and  $\overline{\text{CLK}}$  input will bias around  $V_{CC}/2$ .

Datasheets and support documentation are available on Micrel's web site at: [www.micrel.com](http://www.micrel.com).

### Block Diagram



### Features

- 3.3V and 5V power supply options
- 70fs<sub>RMS</sub> typical additive phase jitter
- Typical 30ps output-to-output skew
- Max. 50ps output-to-output skew
- Synchronous enable/disable
- Multiplexed clock input
- 75k $\Omega$  internal input pull-down resistors
- Available in 20-pin SOIC package

### Applications

- Processor clock distribution
- SONET clock distribution
- Fibre Channel clock distribution
- Gigabit Ethernet clock distribution

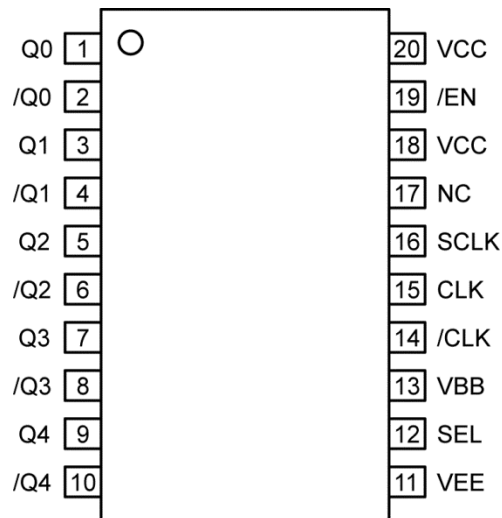
## Ordering Information<sup>(1)</sup>

| Part Number                    | Package Type | Operating Range | Package Marking                              | Lead Finish    |
|--------------------------------|--------------|-----------------|--|----------------|
| SY100EL14VZG                   | Z20-1        | Industrial      | SY100EL14VZG with Pb-Free bar-line indicator | Pb-Free NiPdAu |
| SY100EL14VZG TR <sup>(2)</sup> | Z20-1        | Industrial      | SY100EL14VZG with Pb-Free bar-line indicator | Pb-Free NiPdAu |

### Note:

- Contact factory for die availability. Dice are guaranteed at  $T_A = 25^\circ\text{C}$ , DC electricals only.
- Tape and Reel.

## Pin Configuration



20-Pin Narrow SOIC  
(Top View)

## Pin Description

| Pin     | Function                   |
|---------|----------------------------|
| CLK     | Differential clock inputs  |
| SCLK    | Scan clock input           |
| /EN     | Synchronous enable         |
| SEL     | Clock select input         |
| VBB     | Reference output           |
| Q0 – Q4 | Differential clock outputs |

## Truth Table

| CLK | SCLK | SEL | /EN | Q                |
|-----|------|-----|-----|------------------|
| L   | X    | L   | L   | L                |
| H   | X    | L   | L   | H                |
| X   | L    | H   | L   | L                |
| X   | H    | H   | L   | H                |
| X   | X    | X   | H   | L <sup>(3)</sup> |

### Note:

- On next negative transition of CLK or SCLK

**Absolute Maximum Ratings<sup>(4)</sup>**

|   |                |
|---|----------------|
| Input Voltage ( $V_{IN}$ ) <sup>(6)</sup>                       |                |
| ( $V_{CC} = 0V$ , $V_{IN}$ not more positive than $V_{CC}$ ) .. | -6V to +0V     |
| ( $V_{EE} = 0V$ , $V_{IN}$ not more positive than $V_{CC}$ )... | +0V to +6V     |
| Operating Range ( $V_{EE}$ ) <sup>(7)</sup> .....               | -5.7V to -3.0V |
| Output Current ( $I_{OUT}$ ) Continuous.....                    | 50mA           |
| Surge.....  | 100mA          |
| Lead Temperature (soldering, 20s).....                          | 260°C          |
| Storage Temperature ( $T_s$ ) .....                             | -65 to +150°C  |
| ESD Rating <sup>(8)</sup> .....                                 | >1.5kV         |

**Operating Ratings<sup>(5)</sup>**

|  |                |
|--|----------------|
| Supply Voltage ( $V_{CC}$ ) PECL Operation ..... | 3.0V to 5.5V   |
| ( $V_{EE}$ ) ECL Operation .....                 | -3.0V to -5.5V |
| Ambient Temperature ( $T_A$ ) .....              | -40°C to +85°C |
| Junction Thermal Resistance                      |                |
| SOIC ( $\theta_{JA}$ ) .....                     | 58°C/W         |

**DC Electrical Characteristics<sup>(9)</sup>**

$V_{EE} = V_{EE}(\text{min})$  to  $V_{EE}(\text{max})$ ;  $V_{CC} = \text{GND}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ , unless otherwise stated.

Outputs are terminated through a 50 $\Omega$  resistor to  $V_{CC}-2.0V$ .

| Symbol    | Parameter                           | Condition  | Min.             | Typ.             | Max.             | Units         |
|-----------|-------------------------------------|--|------------------|------------------|------------------|---------------|
| $V_{OH}$  | Output High Voltage <sup>(10)</sup> | $T_A = -40^\circ\text{C}$                        | $V_{CC} - 1.085$ | $V_{CC} - 1.005$ | $V_{CC} - 0.880$ | V             |
|           |                                     | $T_A = 0^\circ\text{C}$ to $+85^\circ\text{C}$   | $V_{CC} - 1.025$ | $V_{CC} - 0.955$ | $V_{CC} - 0.880$ | V             |
| $V_{OL}$  | Output Low Voltage <sup>(10)</sup>  | $T_A = -40^\circ\text{C}$                        | $V_{CC} - 1.830$ | $V_{CC} - 1.695$ | $V_{CC} - 1.555$ | V             |
|           |                                     | $T_A = 0^\circ\text{C}$ to $+85^\circ\text{C}$   | $V_{CC} - 1.810$ | $V_{CC} - 1.705$ | $V_{CC} - 1.620$ | V             |
| $V_{OHA}$ | Output High Voltage <sup>(10)</sup> | $T_A = -40^\circ\text{C}$                        | $V_{CC} - 1.095$ |                  |                  | V             |
|           |                                     | $T_A = 0^\circ\text{C}$ to $+85^\circ\text{C}$   | $V_{CC} - 1.035$ |                  |                  | V             |
| $V_{OLA}$ | Output Low Voltage <sup>(10)</sup>  | $T_A = -40^\circ\text{C}$                        |                  |                  | $V_{CC} - 1.555$ | V             |
|           |                                     | $T_A = 0^\circ\text{C}$ to $+85^\circ\text{C}$   |                  |                  | $V_{CC} - 1.610$ | V             |
| $V_{IH}$  | Input High Voltage                  |  | $V_{CC} - 1.165$ |                  | $V_{CC} - 0.880$ | V             |
| $V_{IL}$  | Input Low Voltage                   |  | $V_{CC} - 1.810$ |                  | $V_{CC} - 1.475$ | V             |
| $I_{IL}$  | Input Low Current <sup>(11)</sup>   | Input LOW Current<br>/CLK                        | 0.5<br>-300      |                  |                  | $\mu\text{A}$ |
| $I_{IH}$  | Input High Current                  |  |                  |                  | 150              | $\mu\text{A}$ |
| $I_{EE}$  | Power Supply Current                | $T_A = -40^\circ\text{C}$ to $+25^\circ\text{C}$ |                  | 32               | 40               | mA            |
|           |                                     | $T_A = +85^\circ\text{C}$                        |                  | 34               | 42               |               |
| $V_{BB}$  | Output Reference Voltage            |  | $V_{CC} - 1.380$ |                  | $V_{CC} - 1.260$ | V             |

**Notes:**

- Exceeding the absolute maximum ratings may damage the device.
- The device is not guaranteed to function outside its operating ratings.
- In PECL mode operation,  $V_{IN}(\text{max}) = V_{CC}$ .
- Parametric values specified at 100EL14V series: -3.0V to -5.5V.
- Devices are ESD sensitive. Handling precautions are recommended. Human body model, 1.5k $\Omega$  in series with 100pF.
- Specification for packaged product only
- $V_{IN} = V_{IH}(\text{max})$  or  $V_{IL}(\text{min})$ .
- $V_{IN} = V_{IL}(\text{max})$ .

## AC Electrical Characteristics

$V_{EE} = V_{EE}(\text{min})$  to  $V_{EE}(\text{max})$ ;  $V_{CC} = \text{GND}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ , unless otherwise stated.

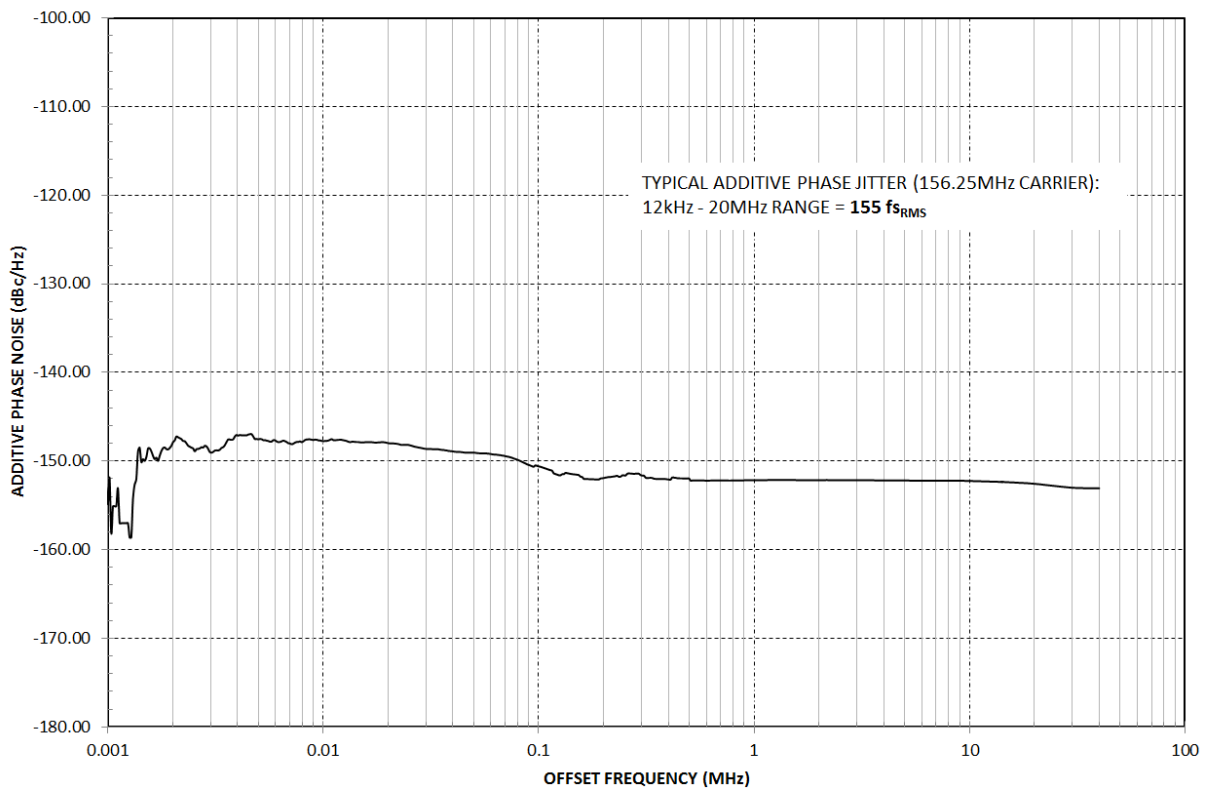
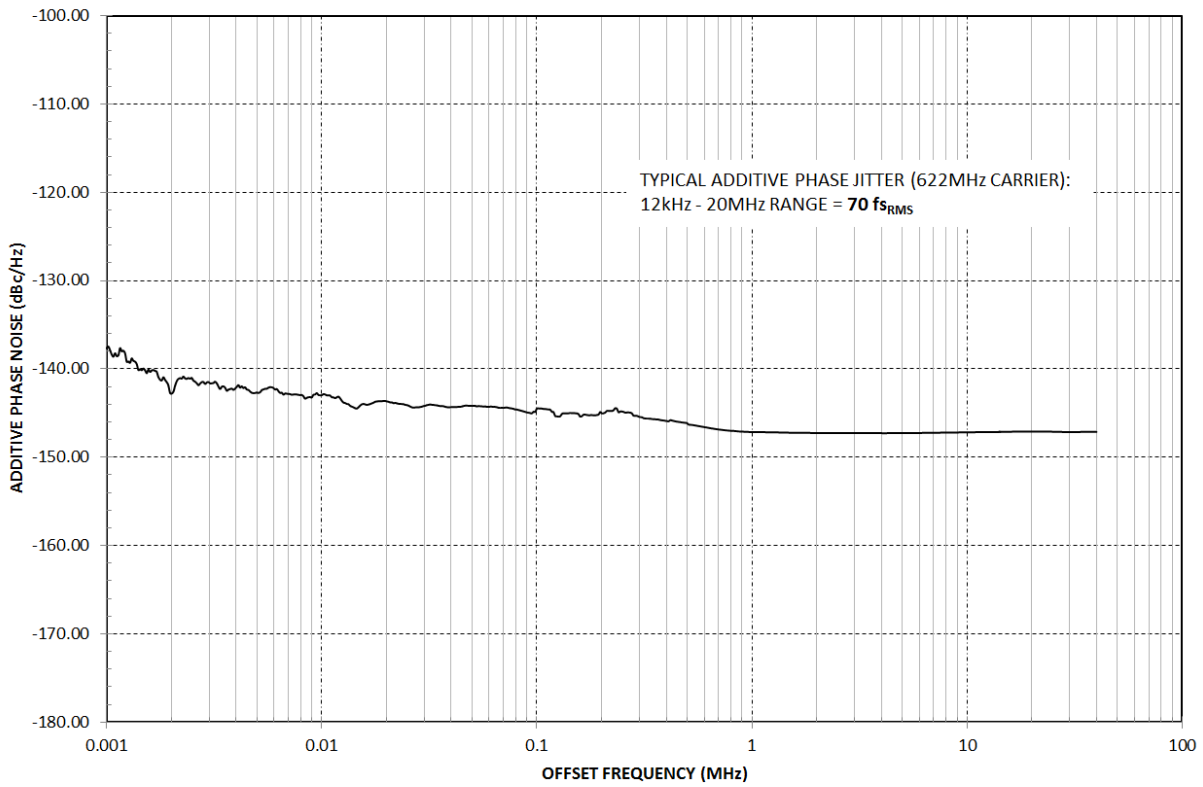
| Symbol                 | Parameter                              | Condition  | Min.   | Typ.             | Max. | Units            |   |
|------------------------|--|--|--|------------------|------|------------------|---|
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>CLK to Q (Diff)   | $T_A = -40^\circ\text{C}$  | 520  |                  | 720  | ps               |   |
|                        |  | $T_A = 0^\circ\text{C}$  | 550  |                  | 750  | ps               |   |
|                        |  | $T_A = +25^\circ\text{C}$  | 580  | 680              | 780  | ps               |   |
|                        |  | $T_A = +85^\circ\text{C}$  | 630  |                  | 830  | ps               |   |
|                        | Propagation Delay<br>CLK to Q (SE)     | $T_A = -40^\circ\text{C}$  | 470  |                  | 770  | ps               |   |
|                        |  | $T_A = 0^\circ\text{C}$  | 500  |                  | 800  | ps               |   |
|                        |  | $T_A = +25^\circ\text{C}$  | 530  | 680              | 830  | ps               |   |
|                        |  | $T_A = +85^\circ\text{C}$  | 580  |                  | 880  | ps               |   |
|                        | Propagation Delay<br>SCLK to Q         | $T_A = -40^\circ\text{C}$  | 470  |                  | 770  | ps               |   |
|                        |  | $T_A = 0^\circ\text{C}$  | 500  |                  | 800  | ps               |   |
|                        |  | $T_A = +25^\circ\text{C}$  | 530  | 680              | 830  | ps               |   |
|                        |  | $T_A = +85^\circ\text{C}$  | 580  |                  | 880  | ps               |   |
| $t_{skew}$             | Part-to-Part Skew <sup>(12)</sup>      |  |  |                  | 200  | ps               |   |
|                        | Within-Device Skew                     |  |  |                  | 50   | ps               |   |
| $t_S$                  | Setup Time /EN                         |  | 150  |                  |      | ps               |   |
| $t_H$                  | Hold Time /EN                          |  | 200  |                  |      | ps               |   |
| $V_{PP}$               | Minimum Input Swing, CLK               |  | 150  |                  |      | mV               |   |
| $V_{CMR}$              | Common Mode Range <sup>(13)</sup>      | $V_{PP} < 500\text{mV}$  | $T_A = -40^\circ\text{C}$                      | $V_{CC} - 2.000$ |      | $V_{CC} - 0.400$ | V |
|                        |  |  | $T_A = 0^\circ\text{C}$ to $+85^\circ\text{C}$ | $V_{CC} - 2.100$ |      | $V_{CC} - 0.400$ | V |
|                        |  | $V_{PP} \geq 500\text{mV}$   | $T_A = -40^\circ\text{C}$                      | $V_{CC} - 1.800$ |      | $V_{CC} - 0.400$ | V |
|                        |  |  | $T_A = 0^\circ\text{C}$ to $+85^\circ\text{C}$ | $V_{CC} - 1.900$ |      | $V_{CC} - 0.400$ | V |
| $t_r/t_f$              | Output Rise/Fall Time<br>Q (20% - 80%) | $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$<br>Typical value at $T_A = +25^\circ\text{C}$ | 230  | 360              | 500  | ps               |   |
| $t_{JITTER}$           | Additive Jitter                        | Carrier = 622MHz<br>Integration Range: 12kHz to 20MHz  |  | 70               |      | $f_{SRMS}$       |   |
|                        |  | Carrier = 156.25MHz<br>Integration Range: 12kHz to 20MHz                                       |  | 155              |      |                  |   |

### Notes:

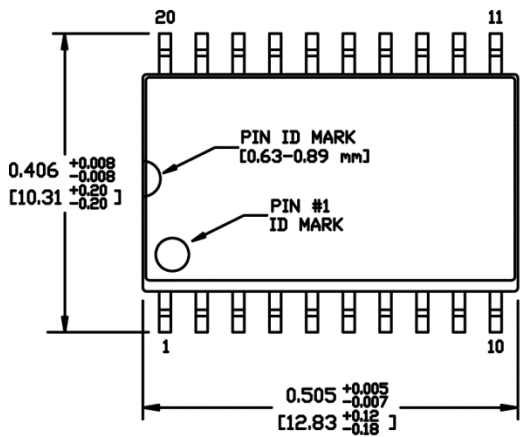
- Skews are specified for identical LOW-to-HIGH or HIGH-to-LOW transitions.
- The  $V_{CMR}$  range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{PP}(\text{min})$  and 1V. The lower end of the  $V_{CMR}$  range varies 1:1 with  $V_{EE}$ . The numbers in the specification table assume a nominal  $V_{EE}$  of 3.3V. For PECL operation, the  $V_{CMR}(\text{min})$  will be fixed at  $3.3\text{V} - |V_{CMR}(\text{min})|$ .

### Additive Phase Noise

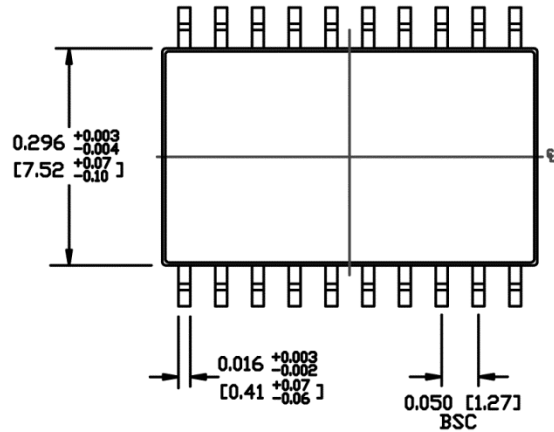
V<sub>CC</sub> = +5V, T<sub>A</sub> = 25°.



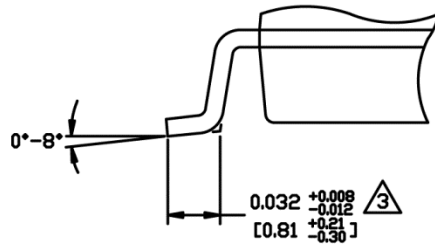
Package Information<sup>(14)</sup>



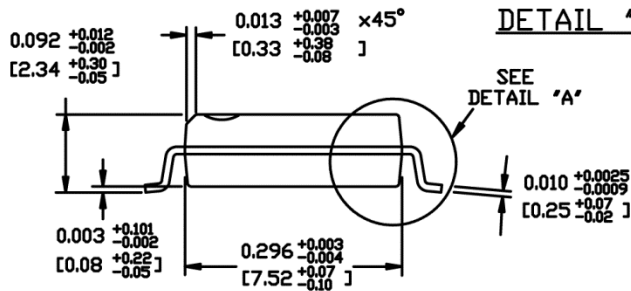
TOP VIEW  
NOTE 1, 2



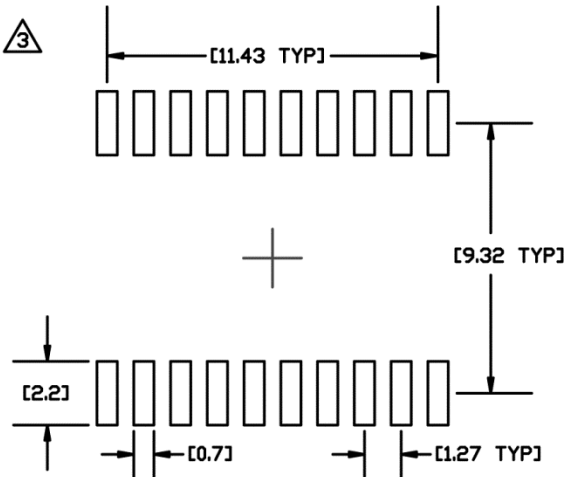
BOTTOM VIEW  
NOTE 1, 2



DETAIL "A"



END VIEW  
NOTE 1, 2, 3



RECOMMENDED LAND PATTERN

NOTES:

1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.006[0.15] PER SIDE.

20-Pin Narrow SOIC (Z20-1)

Note:

14. Package information is correct as of the publication date. For updates and most current information, go to [www.micrel.com](http://www.micrel.com).

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