SY100EL14V

5V/3.3V 1:5 Clock Distribution

General Description

The SY100EL14V is a low-skew, 1:5 clock distribution chip designed explicitly for low-skew clock distribution applications. The device can be driven by either a differential or single-ended ECL or, if positive power supplies are used, PECL input signal. The EL14V is suitable for operation in systems operating with 3.3V to 5.0V supplies. If a single-ended input is to be used, the V_{BB} output should be connected to the /CLK input and bypassed to ground via a 0.01µF capacitor. The V_{BB} output is designed to act as the switching reference for the input of the EL14V under single-ended input conditions. As a result, this pin can only source/sink up to 0.5mA of current.

The EL14V features a multiplexed clock input to allow for the distribution of a lower speed scan or test clock along with the high speed system clock. When LOW (or left open and pulled LOW by the input pull-down resistor), the SEL pin will select the differential clock input.

The common enable (/EN) is synchronous, so that the outputs will only be enabled/disable when they are already in the LOW state. This avoids any chance of generating a runt clock pulse when the device is enabled/disabled as can happen with an asynchronous control. The internal flip-flop is clocked on the falling edge of the input clock. Therefore, all associated specification limits are referenced to the negative edge of the clock input.

When both differential inputs are left open, CLK input will pull down to V_{EE} and /CLK input will bias around $V_{CC}/2$.

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.

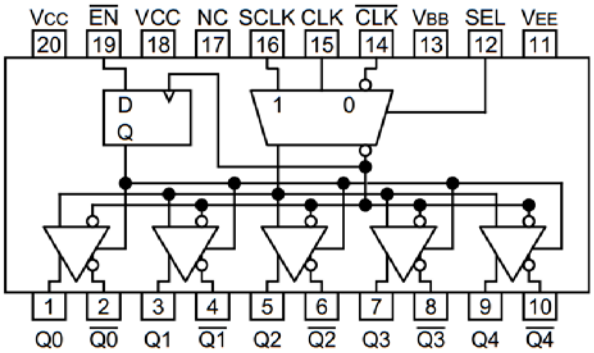
Features

- 3.3V and 5V power supply options
- 70fs$_{RMS}$ typical additive phase jitter
- Typical 30ps output-to-output skew
- Max. 50ps output-to-output skew
- Synchronous enable/disable
- Multiplexed clock input
- 75kΩ internal input pull-down resistors
- Available in 20-pin SOIC package

Applications

- Processor clock distribution
- SONET clock distribution
- Fibre Channel clock distribution
- Gigabit Ethernet clock distribution

Block Diagram



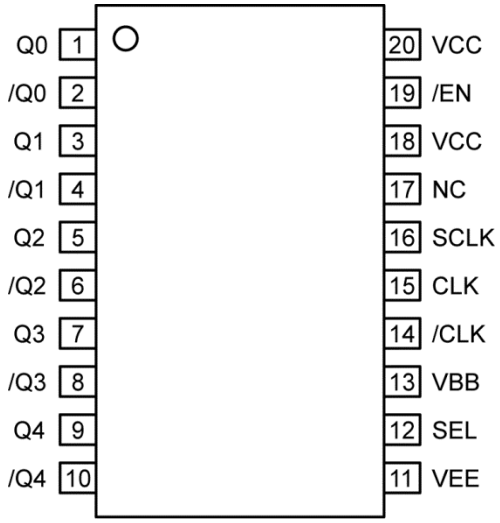
Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100EL14VZG	Z20-1	Industrial	SY100EL14VZG with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY100EL14VZG TR[2]	Z20-1	Industrial	SY100EL14VZG with Pb-Free bar-line indicator	Pb-Free NiPdAu

Note:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC electricals only.
2. Tape and Reel.

Pin Configuration



20-Pin Narrow SOIC
(Top View)

Pin Description

Pin	Function
CLK	Differential clock inputs
SCLK	Scan clock input
/EN	Synchronous enable
SEL	Clock select input
VBB	Reference output
Q0 – Q4	Differential clock outputs

Truth Table

CLK	SCLK	SEL	/EN	Q
L	X	L	L	L
H	X	L	L	H
X	L	H	L	L
X	H	H	L	H
X	X	X	H	L[3]

Note:

3. On next negative transition of CLK or SCLK

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Absolute Maximum Ratings[4]

Input Voltage (V_{IN})[6]
(V_{CC} = 0V, V_{IN} not more positive than V_{CC}) .. –6V to +0V
(V_{EE} = 0V, V_{IN} not more positive than V_{CC})... +0V to +6V
Operating Range (V_{EE})[7] ..... –5.7V to –3.0V
Output Current (I_{OUT}) Continuous.....50mA
Surge.....100mA
Lead Temperature (soldering, 20s)..... 260°C
Storage Temperature (T_s) .....–65 to +150°C
ESD Rating[8].....>1.5kV

Operating Ratings[5]

Supply Voltage (V_{CC}) PECL Operation ..... 3.0V to 5.5V
(V_{EE}) ECL Operation ..... –3.0V to –5.5V
Ambient Temperature (T_A) .....–40°C to +85°C
Junction Thermal Resistance
SOIC (θ_{JA}) .....58°C/W

DC Electrical Characteristics[9]

V_{EE} = V_{EE} (min) to V_{EE} (max); V_{CC} = GND, T_A = –40°C to +85°C, unless otherwise stated.
Outputs are terminated through a 50Ω resistor to V_{CC}–2.0V.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage[10]	T_A = –40°C	V_{CC} – 1.085	V_{CC} – 1.005	V_{CC} – 0.880	V
		T_A = 0°C to +85°C	V_{CC} – 1.025	V_{CC} – 0.955	V_{CC} – 0.880	V
V_{OL}	Output Low Voltage[10]	T_A = –40°C	V_{CC} – 1.830	V_{CC} – 1.695	V_{CC} – 1.555	V
		T_A = 0°C to +85°C	V_{CC} – 1.810	V_{CC} – 1.705	V_{CC} – 1.620	V
V_{OHA}	Output High Voltage[10]	T_A = –40°C	V_{CC} – 1.095			V
		T_A = 0°C to +85°C	V_{CC} – 1.035			V
V_{OLA}	Output Low Voltage[10]	T_A = –40°C			V_{CC} – 1.555	V
		T_A = 0°C to +85°C			V_{CC} – 1.610	V
V_{IH}	Input High Voltage		V_{CC} – 1.165		V_{CC} – 0.880	V
V_{IL}	Input Low Voltage		V_{CC} – 1.810		V_{CC} – 1.475	V
I_{IL}	Input Low Current[11]	Input LOW Current /CLK	0.5 –300			µA
I_{IH}	Input High Current				150	µA
I_{EE}	Power Supply Current	T_A = –40°C to +25°C		32	40	mA
		T_A = +85°C		34	42	
V_{BB}	Output Reference Voltage		V_{CC} – 1.380		V_{CC} – 1.260	V

Notes:

4. Exceeding the absolute maximum ratings may damage the device.
5. The device is not guaranteed to function outside its operating ratings.
6. In PECL mode operation, V_{IN}(max) = V_{CC}.
7. Parametric values specified at 100EL14V series: –3.0V to –5.5V.
8. Devices are ESD sensitive. Handling precautions are recommended. Human body model, 1.5kΩ in series with 100pF.
9. Specification for packaged product only
10. V_{IN} = V_{IH}(max) or V_{IL}(min).
11. V_{IN} = V_{IL}(max).

AC Electrical Characteristics

V_{EE} = V_{EE} (min) to V_{EE} (max); V_{CC} = GND, T_A = –40°C to +85°C, unless otherwise stated.

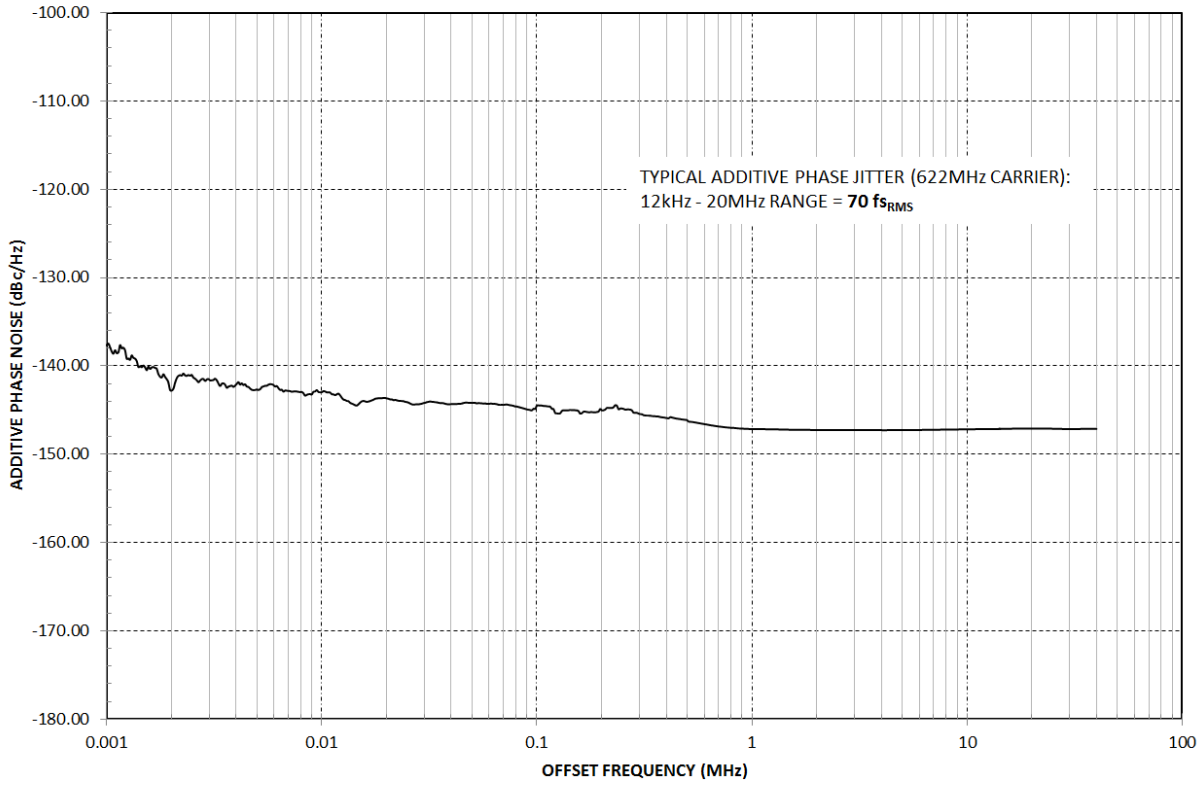
Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
t_{PLH} t_{PHL}	Propagation Delay CLK to Q (Diff)	T_A = –40°C		520		720	ps
		T_A = 0°C		550		750	ps
		T_A = +25°C		580	680	780	ps
		T_A = +85°C		630		830	ps
	Propagation Delay CLK to Q (SE)	T_A = –40°C		470		770	ps
		T_A = 0°C		500		800	ps
		T_A = +25°C		530	680	830	ps
		T_A = +85°C		580		880	ps
	Propagation Delay SCLK to Q	T_A = –40°C		470		770	ps
		T_A = 0°C		500		800	ps
		T_A = +25°C		530	680	830	ps
		T_A = +85°C		580		880	ps
t_{skew}	Part-to-Part Skew[12]					200	ps
	Within-Device Skew					50	ps
t_S	Setup Time /EN			150			ps
t_H	Hold Time /EN			200			ps
V_{PP}	Minimum Input Swing, CLK			150			mV
V_{CMR}	Common Mode Range[13]	V_{PP} < 500mV	T_A = –40°C	V_{CC} – 2.000		V_{CC} – 0.400	V
			T_A = 0°C to +85°C	V_{CC} – 2.100		V_{CC} – 0.400	
		V_{PP} ≥ 500mV	T_A = –40°C	V_{CC} – 1.800		V_{CC} – 0.400	V
			T_A = 0°C to +85°C	V_{CC} – 1.900		V_{CC} – 0.400	
t_r/t_f	Output Rise/Fall Time Q (20% - 80%)	T_A = –40°C to +85°C Typical value at T_A = +25°C		230	360	500	ps
t_{JITTER}	Additive Jitter	Carrier = 622MHz Integration Range: 12kHz to 20MHz			70		fs_{RMS}
		Carrier = 156.25MHz Integration Range: 12kHz to 20MHz			155		

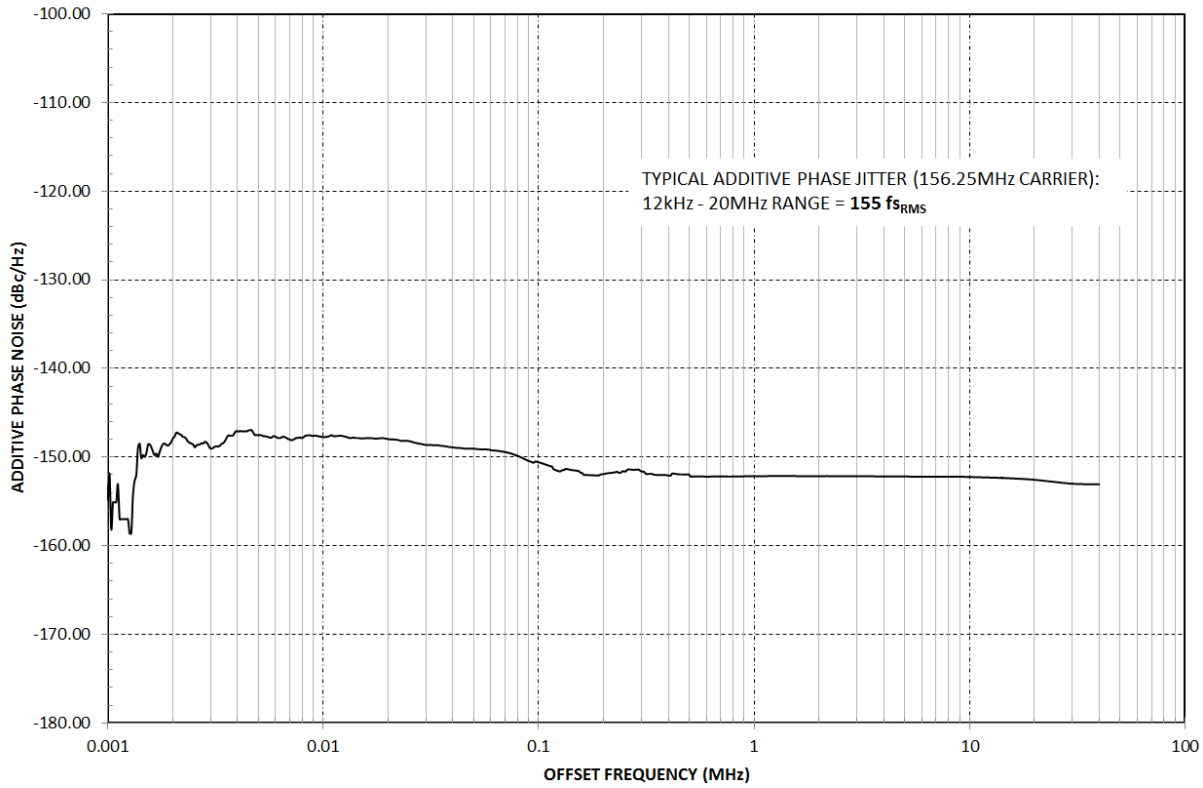
Notes:

12. Skews are specified for identical LOW-to-HIGH or HIGH-to-LOW transitions.
13. The V_{CMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}(min) and 1V. The lower end of the V_{CMR} range varies 1:1 with V_{EE}. The numbers in the specification table assume a nominal V_{EE} of 3.3V. For PECL operation, the V_{CMR}(min) will be fixed at 3.3V – |V_{CMR}(min)|.

Additive Phase Noise

V_{CC} = +5V, T_A = 25°.





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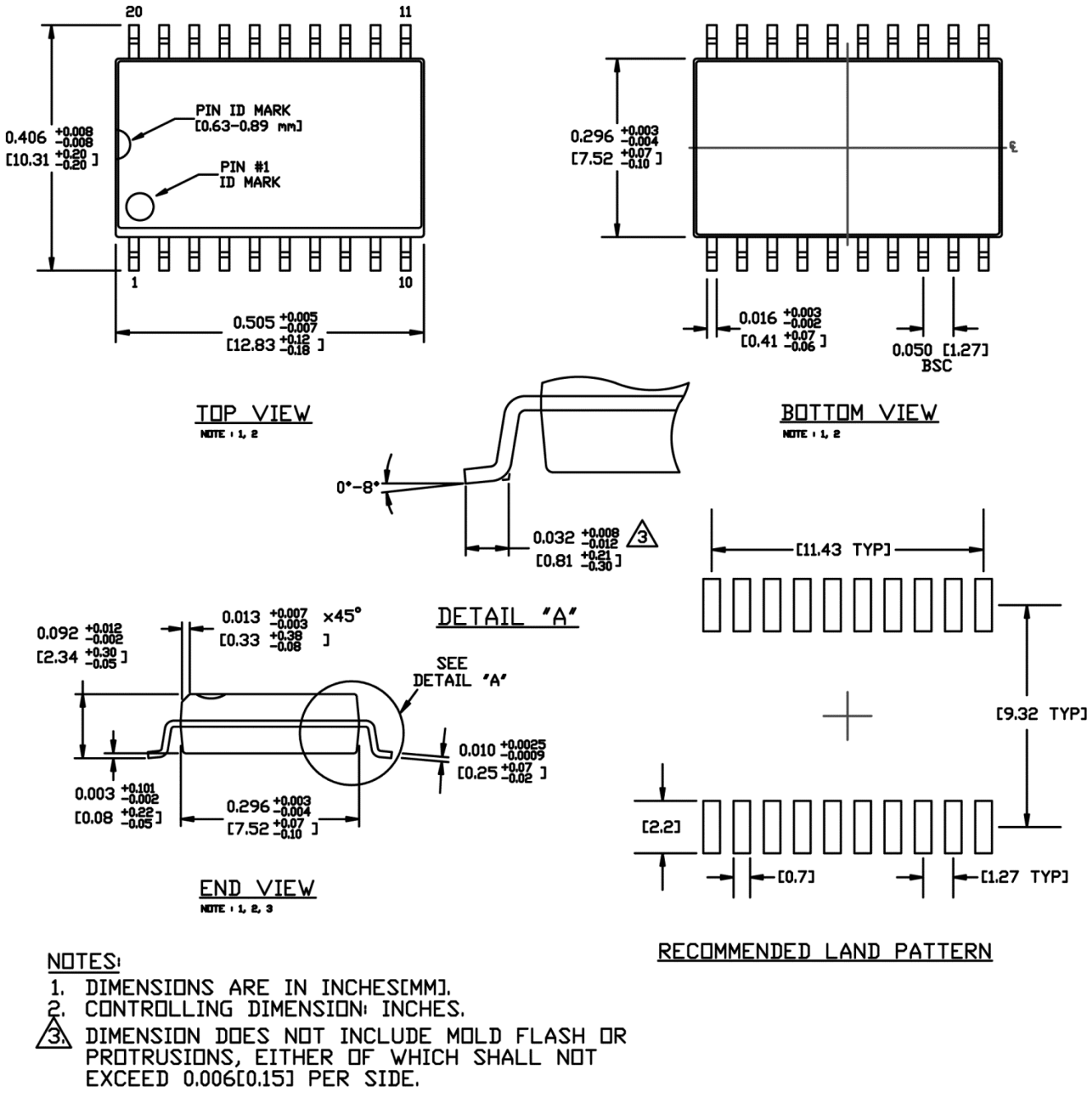
Package Information[14]



20-Pin Narrow SOIC (Z20-1)

Note:

14. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

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