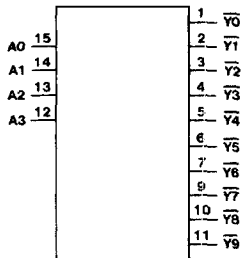


CD54/74HC42 CD54/74HCT42

High-Speed CMOS Logic



92CS-38860
FUNCTIONAL DIAGRAM

BCD to Decimal Decoder (1-of-10)

Type Features:

- Buffered inputs and outputs
- Typical propagation delay = 12 ns @ $V_{CC} = 5V, C_L = 15 pF$
 $T_A = 25^\circ C$ (HC42)

The RCA-CD54/74HC42 and CD54/74HCT42 BCD-to-Decimal Decoders utilize silicon-gate CMOS technology to achieve operating speeds similar to LSTTL decoders with the low power consumption of standard CMOS integrated circuits. These devices have the capability of driving 10 LSTTL loads and are compatible with the standard 54LS/74LS logic family. One of ten outputs (low on select) is selected in accordance with the BCD input. Non-valid BCD inputs result in none of the outputs being selected (all outputs are high).

The CD54HC42 and CD54HCT42 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC42 and CD74HCT42 are supplied in 16-lead dual-in-line plastic packages (E suffix), and in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- Fanout (Over Temperature Range):
Standard Outputs - 10 LSTTL Loads
Bus Driver Outputs - 15 LSTTL Loads
- Wide Operating Temperature Range:
CD74HC/HCT: -40 to $+85^\circ C$
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- Alternate Source is Philips/Signetics
- CD54HC/CD74HC Types:
2 to 6 V Operation
High Noise Immunity:
 $N_{IL} = 30\%, N_{IH} = 30\%$ of V_{CC} ; @ $V_{CC} = 5 V$
- CD54HCT/CD74HCT Types:
4.5 to 5.5 V Operation
Direct LSTTL Input Logic Compatibility
 $V_{IL} = 0.8 V$ Max., $V_{IH} = 2 V$ Min.
CMOS Input Compatibility
 $I_L \leq 1 \mu A$ @ V_{OL}, V_{OH}

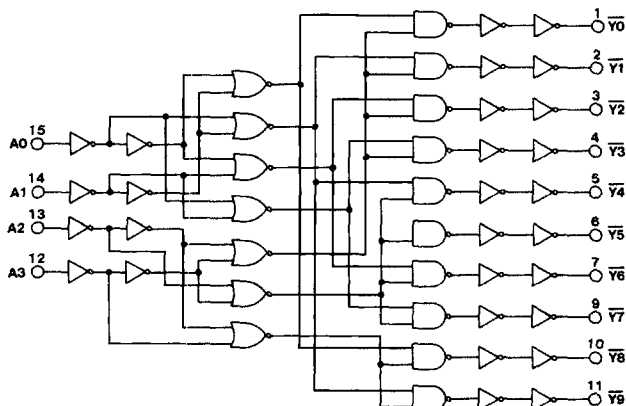
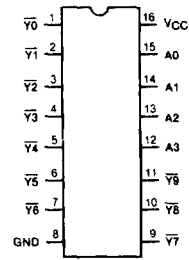


Fig. 1 — Logic diagram

92CS-38861



TERMINAL ASSIGNMENT

92CS-38869

CD54/74HC42 CD54/74HCT42

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE, (V _{CC}):	
(Voltages referenced to ground)	-0.5 to + 7 V
DC INPUT DIODE CURRENT, I _{IK} (FOR V _i < -0.5 V OR V _i > V _{CC} + 0.5V)	±20mA
DC OUTPUT DIODE CURRENT, I _{OK} (FOR V _o < -0.5 V OR V _o > V _{CC} - 0.5V)	±20mA
DC DRAIN CURRENT, PER OUTPUT (I _o) (FOR -0.5 V < V _o < V _{CC} + 0.5V)	±25mA
DC V _{CC} OR GROUND CURRENT (I _{CC})	±50mA
POWER DISSIPATION PER PACKAGE (P _o):	
For T _A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T _A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T _A = -55 to +100°C (PACKAGE TYPE F, H)	500 mW
For T _A = +100 to +125°C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/°C to 300 mW
For T _A = -40 to +70°C (PACKAGE TYPE M)	400 mW
For T _A = +70 to +125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T _A):	
PACKAGE TYPE F, H	-55 to +125°C
PACKAGE TYPE E, M	-40 to -85°C
STORAGE TEMPERATURE (T _{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)	
with solder contacting lead tips only	+300°C

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T _A = Full Package Temperature Range) V _{CC} .*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage V _i , V _o	0	V _{CC}	V
Operating Temperature T _A :			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times t _r , t _f			
at 2 V	0	1000	ns
at 4.5 V	0	500	
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

TRUTH TABLE

Inputs				Outputs									
A3	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8	Y9
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

L = Low Voltage Level
H = High Voltage Level

CD54/74HC42 CD54/74HCT42

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC42/CD54HC42										CD74HCT42/CD54HCT42								UNITS			
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES			TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES			54HCT TYPES		
	V _i V	I _o mA	V _{cc} V	+25°C			-40/ +85°C		-55/ +125°C			V _i V	V _{cc} V	+25°C			-40/ +85°C			-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max	Min			Max	Min	Max	Min	Max				
High-Level Input Voltage V _{ih}			2	1.5	—	—	1.5	—	1.5	—	—	4.5			2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—	—	to			—	—	—	—	—	—	—	
			6	4.2	—	—	4.2	—	4.2	—	—	5.5										
Low-Level Input Voltage V _{il}			2	—	—	0.5	—	0.5	—	0.5	—	4.5			—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35	—	to			—	—	—	—	—	—	—	
			6	—	—	1.8	—	1.8	—	1.8	—	5.5										
High-Level Output Voltage V _{oh} CMOS Loads	V _{ih}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V _{ih}											V
	or		4.5	4.4	—	—	4.4	—	4.4	—	or	4.5	4.4	—	—	4.4	—	4.4	—	4.4	—	
	V _{ih}		6	5.9	—	—	5.9	—	5.9	—	V _{ih}											
TTL Loads	V _{ih}										V _{ih}											V
	or	-4	4.5	3.98	—	—	3.84	—	3.7	—	or	4.5	3.98	—	—	3.84	—	3.7	—	3.7	—	
	V _{ih}	-5.2	6	5.48	—	—	5.34	—	5.2	—	V _{ih}											
Low-Level Output Voltage V _{ol} CMOS Loads	V _{ih}	0.02	2	—	—	0.1	—	0.1	—	0.1	V _{ih}											V
	or		4.5	—	—	0.1	—	0.1	—	0.1	—	or	4.5	—	—	0.1	—	0.1	—	0.1	—	
	V _{ih}		6	—	—	0.1	—	0.1	—	0.1	—	V _{ih}										
TTL Loads	V _{ih}										V _{ih}											V
	or	4	4.5	—	—	0.26	—	0.33	—	0.4	or	4.5	—	—	0.26	—	0.33	—	0.4	—	0.4	
	V _{ih}	5.2	6	—	—	0.26	—	0.33	—	0.4	V _{ih}											
Input Leakage Current I _i	V _{cc} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V _{cc} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	—	±1	μA
Quiescent Device Current I _{cc}	V _{cc} or Gnd	0	6	—	—	8	—	80	—	160	V _{cc} or Gnd	5.5	—	—	8	—	80	—	160	—	160	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI _{cc} *											V _{cc} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	—	490	μA

*For dual-supply systems theoretical worst case (V_i = 2.4 V, V_{cc} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
ALL	1

*Unit Load is ΔI_{cc} limit specified in Static Characteristic Chart.
e.g., 360 μA max. @ 25°C.

CD54/74HC42 CD54/74HCT42

SWITCHING CHARACTERISTICS ($V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, Input $t_r, t_f = 6\text{ ns}$)

CHARACTERISTIC	C_L (pF)	SYMBOL	TYPICAL		UNITS
			54/74HC	54/74HCT	
Any Input to \bar{Y}	15	t_{PHL}, t_{PLH}	12	14	ns
Power Dissipation Capacitance*	—	C_{PD}	65	70	pF

* C_{PD} is used to determine the dynamic power consumption, per package.

$$P_D = V_{CC}^2 f_i (C_{PD} + C_L) \text{ where:}$$

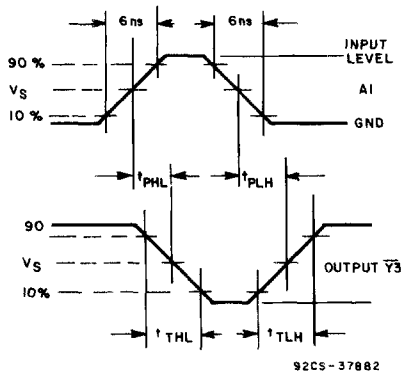
f_i = input frequency.

C_L = output load capacitance.

V_{CC} = supply voltage.

SWITCHING CHARACTERISTICS ($C_L = 50\text{ pF}$, Input $t_r, t_f = 6\text{ ns}$)

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay, Any Input to \bar{Y}	t_{PLH}	2	—	150	—	—	—	190	—	—	—	225	—	—	ns
	t_{PHL}	4.5	—	30	—	35	—	38	—	44	—	45	—	53	
		6	—	26	—	—	—	33	—	—	—	38	—	—	
Output Transition Time	t_{THL}	2	—	75	—	—	—	95	—	—	—	110	—	—	ns
	t_{TLH}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_i		—	—	—	—	—	—	—	—	—	—	—	—	pF
			—	10	—	10	—	10	—	10	—	10	—	10	
			—	—	—	—	—	—	—	—	—	—	—	—	



	54/74HC	54/74HCT
Input Level	V_{CC}	3V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Transition times and propagation delay times.