LOW SKEW CMOS PLL CLOCK DRIVER WITH INTEGRATED LOOP FILTER

QS5917T

Product Assembled from Die Bank Only

PRODUCT DISCONTINUATION NOTICE - LAST TIME BUY EXPIRES OCTOBER 28, 2014

FEATURES:

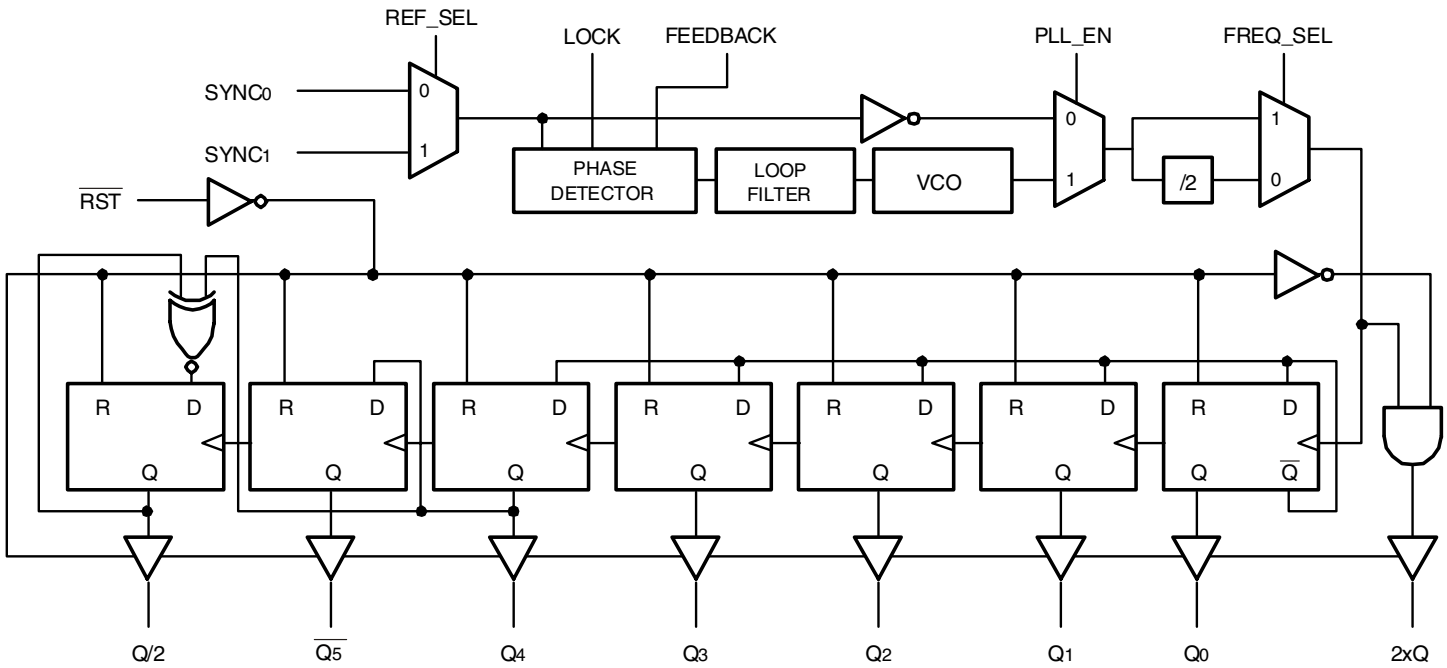
- **5V operation**
- **2xQ output, Q/2 output, Q output**
- **Outputs tri-state while $\overline{RST}$ low**
- **Internal loop filter RC network**
- **Low noise TTL level outputs**
- **< 500ps output skew, Q_0-Q_4**
- **PLL disable feature for low frequency testing**
- **Balanced Drive Outputs ± 24mA**
- **132MHz maximum frequency (2xQ output)**
- **Functional equivalent to Motorola MC88915**
- **ESD > 2000V**
- **Latch-up > –300mA**
- **Available in QSOP and PLCC packages**
- **Not Recommended for New Design**

DESCRIPTION

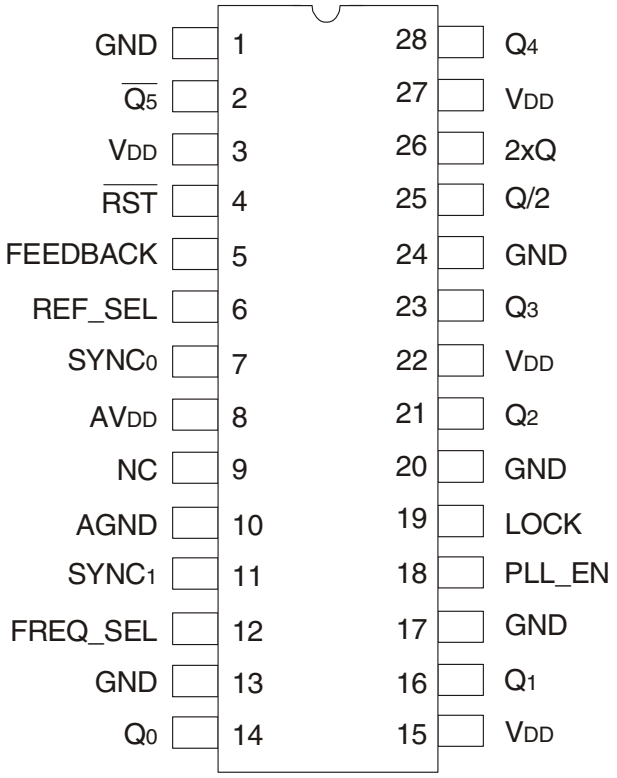
The QS5917T Clock Driver uses an internal phase locked loop (PLL) to lock low skew outputs to one of two reference clock inputs. Eight outputs are available: Q_0-Q_4, 2xQ, Q/2, $\overline{Q_5}$. Careful layout and design insures < 500ps skew between the Q_0-Q_4, and Q/2 outputs. The QS5917T includes an internal RC filter which provides excellent jitter characteristics and eliminates the need for external components. In addition, TTL level outputs reduce clock signal noise. Various combinations of feedback and a divide-by-2 in the VCO path allow applications to be customized for linear VCO operation over a wide range of input SYNC frequencies. The VCO can also be disabled by the PLL_EN signal to allow low frequency or DC testing. The LOCK output asserts to indicate when phase lock has been achieved. The QS5917T is designed for use in high-performance workstations, multi-board computers, networking hardware, and mainframe systems. Several can be used in parallel or scattered throughout a system for guaranteed low skew, system-wide clock distribution networks.

For more information on PLL clock driver products, see Application Note AN-227.

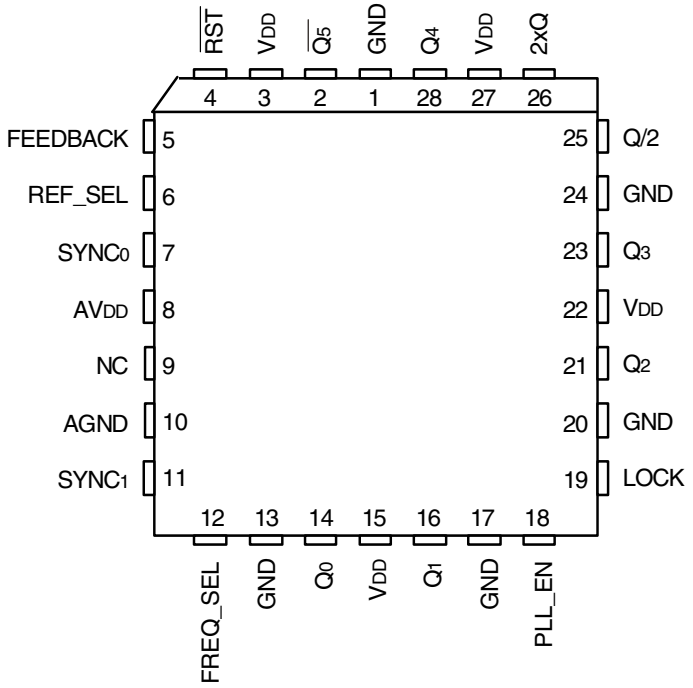
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



QSOP
TOP VIEW



PLCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Max	Unit
	Supply Voltage to Ground	–0.5 to +7	V
	DC Input Voltage V_{IN}	–0.5 to +7	V
	AC Input Voltage (pulse width ≤ 20ns)	–3	V
	Maximum Power Dissipation (T_A = 85°C)	1.2	W
T_{STG}	Storage Temperature Range	–65 to +150	°C

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz, V_{IN} = 0V)

	QSOP		PLCC		
Parameter	Typ.	Max.	Typ.	Max.	Unit
C_{IN}	3	4	4	6	pF
C_{OUT}	7	9	8	10	pF

PIN DESCRIPTION

Pin Names	I/O	Description
$SYNC_0$	I	Reference clock input
$SYNC_1$	I	Reference clock input
REF_SEL	I	Reference clock select. When 1, selects $SYNC_1$. When 0, selects $SYNC_0$.
FREQ_SEL	I	VCO frequency select. For choosing optimal VCO operating frequency depending on input frequency.
FEEDBACK	I	PLL feedback input which is connected to a user selected output pin. External feedback provides flexibility for different output frequency relationships. See the Frequency Selection Table for more information.
Q_0 - Q_4	O	Clock outputs
$\overline{Q_5}$	O	Clock output. Matched in frequency, but inverted with respect to Q.
2xQ	O	Clock output. Matched in phase, but frequency is double the Q frequency.
Q/2	O	Clock output. Matched in phase, but frequency is half the Q frequency.
LOCK	O	PLL lock indication signal. 1 indicates positive lock. 0 indicates that the PLL is not locked and outputs may not be synchronized to the inputs.
$\overline{RST}$	I	Asynchronous reset. Resets all output registers. When 0, all outputs are held in a tri-stated condition. When 1, outputs are enabled (normal operation).
PLL_EN	I	PLL enable. When 1, PLL is enabled (normal operation). When 0, PLL is disabled (for testing purposes).
NC	—	No Connection

OUTPUT FREQUENCY SPECIFICATIONS

Industrial: T_A = –40°C to +85°C, AV_{DD}/V_{DD} = 5V ± 5%

Symbol	Description	–70	–100	–132	Units
F_{2XQ}	Max Frequency, 2xQ output	70	100	132	MHz
F_Q	Max Frequency, Q_0 - Q_4, $\overline{Q_5}$ outputs	35	50	66	MHz
$F_{Q/2}$	Max Frequency, Q/2 output	17.5	25	33	MHz

FREQUENCY SELECTION TABLE

FREQ_SEL	Output Used for Feedback	SYNC (MHz) (allowable range)		Output Frequency Relationships			
		Min.	Max	Q/2	$\overline{Q_5}$	Q Outputs	2XQ
1	Q/2	14	F_{2XQ} / 4	SYNC	– SYNC X 2	SYNC X 2	SYNC X 4
1	Q_0-Q_4	28	F_{2XQ} / 2	SYNC / 2	– SYNC	SYNC	SYNC X 2
1	$\overline{Q_5}$	28	F_{2XQ} / 2	– SYNC / 2	SYNC	– SYNC	– SYNC X 2
1	2xQ	56	F_{2XQ}[1]	SYNC / 4	– SYNC / 2	SYNC / 2	SYNC
0	Q/2	7	F_{2XQ} / 8	SYNC	– SYNC X 2	SYNC X 2	SYNC X 4
0	Q_0-Q_4	14	F_{2XQ} / 4	SYNC / 2	– SYNC	SYNC	SYNC X 2
0	$\overline{Q_5}$	14	F_{2XQ} / 4	– SYNC / 2	SYNC	– SYNC	– SYNC X 2
0	2xQ	28	F_{2XQ} / 2	SYNC / 4	– SYNC / 2	SYNC / 2	SYNC

NOTE:
1. For –132 speed grade, maximum input frequency is restricted to 100MHz.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Industrial: T_A = –40°C to +85°C, A_{VDD}/V_{DD} = 5V ± 5%

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IH}	Input HIGH Voltage Level	Guaranteed Logic HIGH level	2	—	—	V
V_{IL}	Input LOW Voltage Level	Guaranteed Logic LOW level	—	—	0.9	V
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = –24mA [1]	2.4	—	—	V
		V_{DD} = Min., I_{OH} = –100µA	3	—	—	
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 24mA [1]	—	—	0.55	V
		V_{DD} = Min., I_{OL} = 100µA	—	—	0.2	
I_{OZ}	Output Leakage Current	V_{OUT} = V_{DD} or GND, V_{DD} = Max.	—	—	±5	µA
I_{IN}	Input Leakage Current	V_{IN} = AV_{DD} or GND, AV_{DD} = Max.	—	—	±5	µA

NOTE:
1. I_{OL} and I_{OH} are 12mA and –12mA, respectively, for the LOCK output.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions [1]	Typ.	Max.	Unit
ΔI_{CC}	Input Power Supply Current per TTL Input HIGH [2]	V_{DD} = Max., V_{IN} = 3.4V	0.4	1.5	mA
I_{CCD}	Dynamic Power Supply Current	V_{DD} = Max	—	0.4	mA/MHz

NOTES:
1. For conditions shown as Min. or Max., use the appropriate values specified under DC Electrical Characteristics.
2. This specification does not apply to the PLL_EN input.

INPUT TIMING REQUIREMENTS

Symbol	Description	Min.	Max.	Unit
t_R, t_F	Maximum input rise and fall times, 0.8V to 2V	—	3	ns
F_I	Input Clock Frequency, $SYNC_0$, $SYNC_1$ (1)	14	F_{2XQ}	MHz
t_{PWC}	Input clock pulse, HIGH or LOW	2	—	ns
D_H	Duty cycle, $SYNC_0$, $SYNC_1$	25	75	%

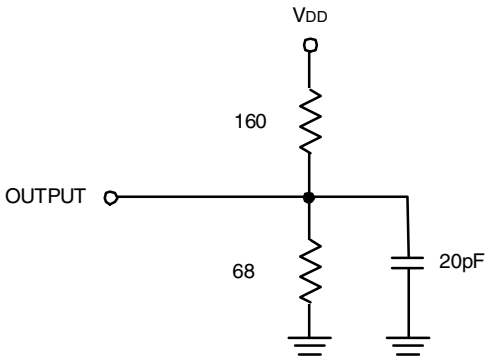
NOTE:
1. The F_I specification is based on Q output feedback. See the Frequency Selection Table for more detail on allowable SYNC input frequencies for different feedback combinations.

SWITCHING CHARACTERISTICS(1)

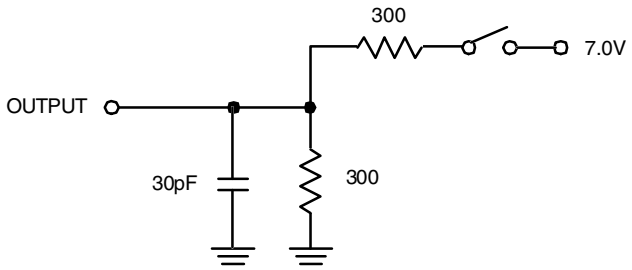
Symbol	Parameter	Min.	Max.	Unit
t_{SKR}	Output Skew Between Rising Edges, Q_0-Q_4 and Q/2 (1)	—	350	ps
t_{SKF}	Output Skew Between Falling Edges, Q_0-Q_4 (1)	—	350	ps
t_{SKALL}	Output Skew, All Outputs (1)	—	500	ps
t_{PW}	Pulse Width, $\overline{Q_5}$, 2xQ outputs	$T_{CY}/2 - 0.65$	$T_{CY}/2 + 0.65$	ns
t_{PW}	Pulse Width, Q_0-Q_4, Q/2 outputs (1)	$T_{CY}/2 - 0.5$	$T_{CY}/2 + 0.5$	ns
t_J	Cycle-to-Cycle Jitter, 33MHz (3)	—	0.25	ns
t_{PD}	SYNC Input to Feedback Delay, 28MHz	–100	400	ps
t_{PD}	SYNC Input to Feedback Delay, 33MHz, 50Ω to 1.5V	–100	400	ps
t_{LOCK}	SYNC to Phase Lock	—	10	ms
t_{PZH} t_{PZL}	Output Enable Time, $\overline{RST}$ LOW to HIGH (2)	0	7	ns
t_{PHZ} t_{PLZ}	Output Disable Time, $\overline{RST}$ HIGH to LOW (2)	0	6	ns
t_R, t_F	Output Rise/Fall Times, 0.8V to 2V	0.4	1.5	ns

NOTES:
1. Skew specifications apply under identical environments (loading, temperature, V_{DD}, device speed grade).
2. Measured in open loop mode PLL_EN = 0.
3. Jitter is characterized using an oscilloscope. Measurement is taken one cycle after jitter. Jitter is characterized but not tested. See FREQUENCY SELECTION TABLE for information on proper FREQ_SEL level for specified input frequencies.

TEST LOAD



TEST CIRCUIT 1



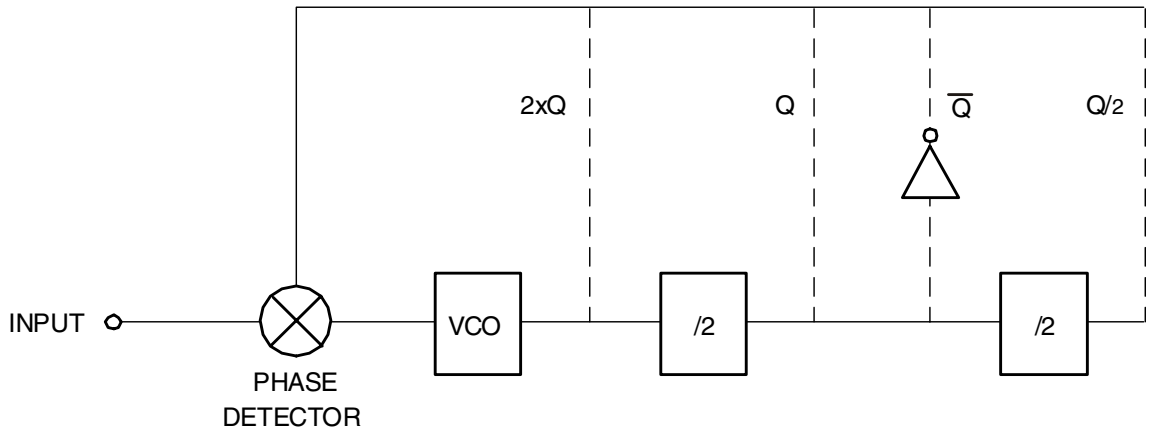
TEST CIRCUIT 2

TEST CIRCUIT 2 is used for output enable/disable parameters.
TEST CIRCUIT 1 is used for all other timing parameters.

PLL OPERATION

The Phase Locked Loop (PLL) circuit included in the QS5917T provides for replication of incoming SYNC clock signals. Any manipulation of that signal, such as frequency multiplying or inversion is performed by digital logic following the PLL (see the block diagram). The key advantage of the PLL circuit is to provide an effective zero propagation delay between the output and input signals. In fact, adding delay circuits in the feedback path, 'propagation delay' can even be negative! A simplified schematic of the QS5917T PLL circuit is shown below.

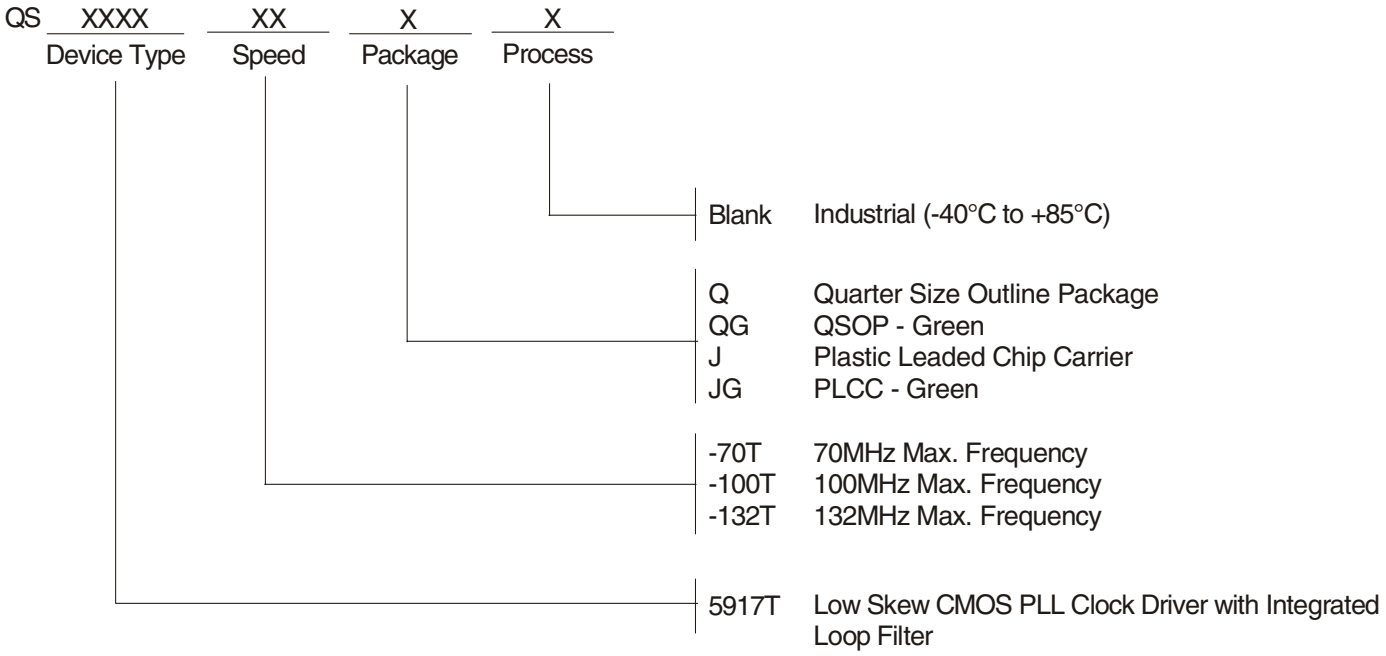
SIMPLIFIED DIAGRAM OF QS5917T FEEDBACK



The phase difference between the output and the input frequencies feeds the VCO which drives the outputs. Whichever output is fed back, it will stabilize at the same frequency as the input. Hence, this is a true negative feedback closed loop system. In most applications, the output will optimally have zero phase shift with respect to the input. In fact, the internal loop filter on the QS5917T typically provides within 150ps of phase shift between input and output.

If the user wishes to vary the phase difference (typically to compensate for backplane delays), this is most easily accomplished by adding delay circuits to the feedback path. The respective output used for feedback will be advanced by the amount of delay in the feedback path. All other outputs will retain their proper relationships to that output.

ORDERING INFORMATION



REVISION HISTORY

1/7/14 Product Discontinuation Notice - Last time buy expires October 28, 2014
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CORPORATE HEADQUARTERS
6024 Silver Creek Valley Road
San Jose, CA 95138

for SALES:
800-345-7015 or 408-284-8200
fax: 408-284-2775
www.idt.com

for Tech Support:
logichelp@idt.com