



**LOW SKEW CMOS PLL  
CLOCK DRIVER WITH  
INTEGRATED LOOP FILTER**

**QS5917T**  
*Product Assembled  
from Die Bank Only*

**PRODUCT DISCONTINUATION NOTICE - LAST TIME BUY EXPIRES OCTOBER 28, 2014**

**FEATURES:**

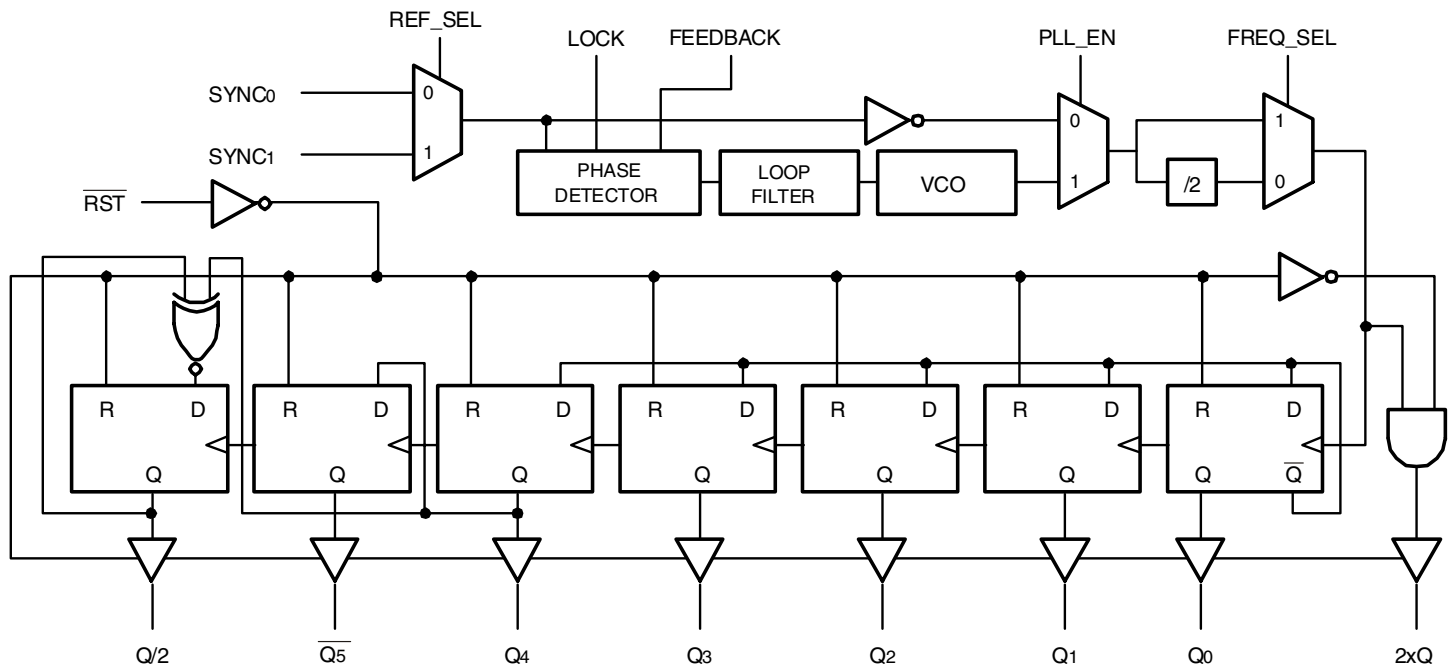
- 5V operation
- 2xQ output, Q/2 output, Q output
- Outputs tri-state while  $\overline{RST}$  low
- Internal loop filter RC network
- Low noise TTL level outputs
- < 500ps output skew, Q0-Q4
- PLL disable feature for low frequency testing
- Balanced Drive Outputs  $\pm 24mA$
- 132MHz maximum frequency (2xQ output)
- Functional equivalent to Motorola MC88915
- ESD > 2000V
- Latch-up > -300mA
- Available in QSOP and PLCC packages
- Not Recommended for New Design

**DESCRIPTION**

The QS5917T Clock Driver uses an internal phase locked loop (PLL) to lock low skew outputs to one of two reference clock inputs. Eight outputs are available: Q0-Q4, 2xQ, Q/2,  $\overline{Q5}$ . Careful layout and design insures < 500ps skew between the Q0-Q4, and Q/2 outputs. The QS5917T includes an internal RC filter which provides excellent jitter characteristics and eliminates the need for external components. In addition, TTL level outputs reduce clock signal noise. Various combinations of feedback and a divide-by-2 in the VCO path allow applications to be customized for linear VCO operation over a wide range of input SYNC frequencies. The VCO can also be disabled by the PLL\_EN signal to allow low frequency or DC testing. The LOCK output asserts to indicate when phase lock has been achieved. The QS5917T is designed for use in high-performance workstations, multi-board computers, networking hardware, and mainframe systems. Several can be used in parallel or scattered throughout a system for guaranteed low skew, system-wide clock distribution networks.

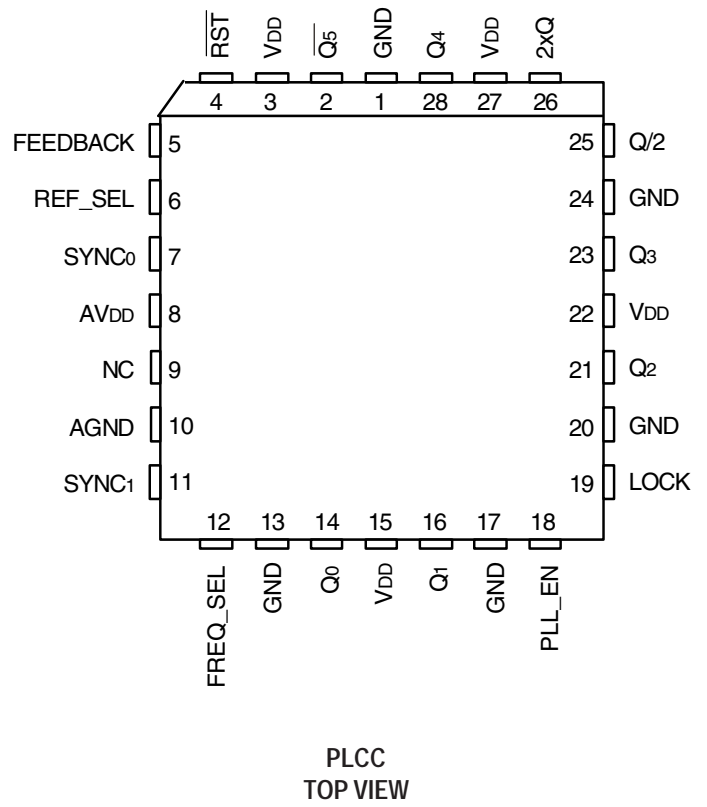
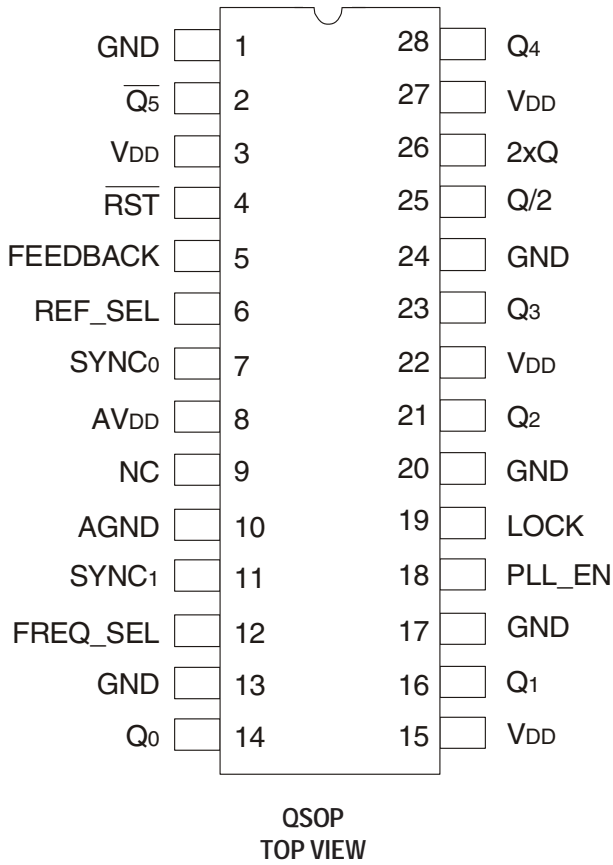
For more information on PLL clock driver products, see Application Note AN-227.

**FUNCTIONAL BLOCK DIAGRAM**



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PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Rating	Max	Unit
	Supply Voltage to Ground	-0.5 to +7	V
	DC Input Voltage $V_{IN}$	-0.5 to +7	V
	AC Input Voltage (pulse width $\leq 20$ ns)	-3	V
	Maximum Power Dissipation ( $T_A = 85^\circ\text{C}$ )	1.2	W
TSTG	Storage Temperature Range	-65 to +150	$^\circ\text{C}$

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE ( $T_A = +25^\circ\text{C}$ ,  $f = 1.0\text{MHz}$ ,  $V_{IN} = 0\text{V}$ )

Parameter	QSOP		PLCC		Unit
	Typ.	Max.	Typ.	Max.	
$C_{IN}$	3	4	4	6	pF
$C_{OUT}$	7	9	8	10	pF

### PIN DESCRIPTION

Pin Names	I/O	Description
SYNC0	I	Reference clock input
SYNC1	I	Reference clock input
REF_SEL	I	Reference clock select. When 1, selects SYNC1. When 0, selects SYNC0.
FREQ_SEL	I	VCO frequency select. For choosing optimal VCO operating frequency depending on input frequency.
FEEDBACK	I	PLL feedback input which is connected to a user selected output pin. External feedback provides flexibility for different output frequency relationships. See the Frequency Selection Table for more information.
Q0-Q4	O	Clock outputs
$\overline{Q5}$	O	Clock output. Matched in frequency, but inverted with respect to Q.
2xQ	O	Clock output. Matched in phase, but frequency is double the Q frequency.
Q/2	O	Clock output. Matched in phase, but frequency is half the Q frequency.
LOCK	O	PLL lock indication signal. 1 indicates positive lock. 0 indicates that the PLL is not locked and outputs may not be synchronized to the inputs.
$\overline{RST}$	I	Asynchronous reset. Resets all output registers. When 0, all outputs are held in a tri-stated condition. When 1, outputs are enabled (normal operation).
PLL_EN	I	PLL enable. When 1, PLL is enabled (normal operation). When 0, PLL is disabled (for testing purposes).
NC	—	No Connection

### OUTPUT FREQUENCY SPECIFICATIONS

Industrial:  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $AV_{DD}/V_{DD} = 5V \pm 5\%$

Symbol	Description	-70	-100	-132	Units
F <sub>2xQ</sub>	Max Frequency, 2xQ output	70	100	132	MHz
F <sub>Q</sub>	Max Frequency, Q0 - Q4, $\overline{Q5}$ outputs	35	50	66	MHz
F <sub>Q/2</sub>	Max Frequency, Q/2 output	17.5	25	33	MHz

## FREQUENCY SELECTION TABLE

FREQ_SEL	Output Used for Feedback	SYNC (MHz) (allowable range)		Output Frequency Relationships			
		Min.	Max	Q/2	$\overline{Q_5}$	Q Outputs	2XQ
1	Q/2	14	F2XQ / 4	SYNC	- SYNC X 2	SYNC X 2	SYNC X 4
1	Q0-Q4	28	F2XQ / 2	SYNC / 2	- SYNC	SYNC	SYNC X 2
1	$\overline{Q_5}$	28	F2XQ / 2	- SYNC / 2	SYNC	- SYNC	- SYNC X 2
1	2xQ	56	F2XQ <sup>(1)</sup>	SYNC / 4	- SYNC / 2	SYNC / 2	SYNC
0	Q/2	7	F2XQ / 8	SYNC	- SYNC X 2	SYNC X 2	SYNC X 4
0	Q0-Q4	14	F2XQ / 4	SYNC / 2	- SYNC	SYNC	SYNC X 2
0	$\overline{Q_5}$	14	F2XQ / 4	- SYNC / 2	SYNC	- SYNC	- SYNC X 2
0	2xQ	28	F2XQ / 2	SYNC / 4	- SYNC / 2	SYNC / 2	SYNC

**NOTE:**

1. For the -132 speed grade, maximum input frequency is restricted to 100MHz.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: TA = -40°C to +85°C, AVDD/VDD = 5V ± 5%

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>IH</sub>	Input HIGH Voltage Level	Guaranteed Logic HIGH level	2	—	—	V
V <sub>IL</sub>	Input LOW Voltage Level	Guaranteed Logic LOW level	—	—	0.9	V
V <sub>OH</sub>	Output HIGH Voltage	V <sub>DD</sub> = Min., I <sub>OH</sub> = -24mA <sup>(1)</sup>	2.4	—	—	V
		V <sub>DD</sub> = Min., I <sub>OH</sub> = -100μA	3	—	—	
V <sub>OL</sub>	Output LOW Voltage	V <sub>DD</sub> = Min., I <sub>OL</sub> = 24mA <sup>(1)</sup>	—	—	0.55	V
		V <sub>DD</sub> = Min., I <sub>OL</sub> = 100μA	—	—	0.2	
I <sub>oz</sub>	Output Leakage Current	V <sub>OUT</sub> = V <sub>DD</sub> or GND, V <sub>DD</sub> = Max.	—	—	±5	μA
I <sub>IN</sub>	Input Leakage Current	V <sub>IN</sub> = AV <sub>DD</sub> or GND, AV <sub>DD</sub> = Max.	—	—	±5	μA

**NOTE:**

1. I<sub>OL</sub> and I<sub>OH</sub> are 12mA and -12mA, respectively, for the LOCK output.

## POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Typ.	Max.	Unit
ΔI <sub>CC</sub>	Input Power Supply Current per TTL Input HIGH <sup>(2)</sup>	V <sub>DD</sub> = Max., V <sub>IN</sub> = 3.4V	0.4	1.5	mA
I <sub>CCD</sub>	Dynamic Power Supply Current	V <sub>DD</sub> = Max	—	0.4	mA/MHz

**NOTES:**

- For conditions shown as Min. or Max., use the appropriate values specified under DC Electrical Characteristics.
- This specification does not apply to the PLL\_EN input.

## INPUT TIMING REQUIREMENTS

Symbol	Description	Min.	Max.	Unit
t <sub>R</sub> , t <sub>F</sub>	Maximum input rise and fall times, 0.8V to 2V	—	3	ns
F <sub>I</sub>	Input Clock Frequency, SYNC <sub>0</sub> , SYNC <sub>1</sub> <sup>(1)</sup>	14	F <sub>2XQ</sub>	MHz
t <sub>PWC</sub>	Input clock pulse, HIGH or LOW	2	—	ns
DH	Duty cycle, SYNC <sub>0</sub> , SYNC <sub>1</sub>	25	75	%

**NOTE:**  
1. The F<sub>I</sub> specification is based on Q output feedback. See the Frequency Selection Table for more detail on allowable SYNC input frequencies for different feedback combinations.

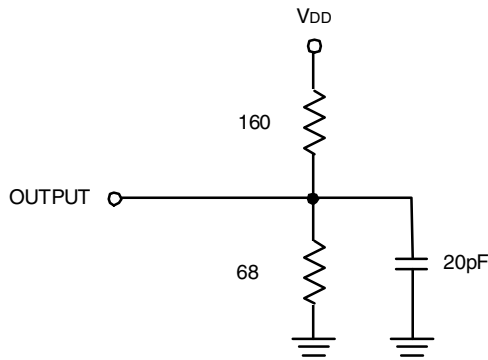
## SWITCHING CHARACTERISTICS<sup>(1)</sup>

Symbol	Parameter	Min.	Max.	Unit
t <sub>SKR</sub>	Output Skew Between Rising Edges, Q <sub>0</sub> -Q <sub>4</sub> and Q/2 <sup>(1)</sup>	—	350	ps
t <sub>SKF</sub>	Output Skew Between Falling Edges, Q <sub>0</sub> -Q <sub>4</sub> <sup>(1)</sup>	—	350	ps
t <sub>SKALL</sub>	Output Skew, All Outputs <sup>(1)</sup>	—	500	ps
t <sub>PW</sub>	Pulse Width, $\overline{Q_5}$ , 2xQ outputs	T <sub>cy</sub> /2 – 0.65	T <sub>cy</sub> /2 + 0.65	ns
t <sub>PW</sub>	Pulse Width, Q <sub>0</sub> -Q <sub>4</sub> , Q/2 outputs <sup>(1)</sup>	T <sub>cy</sub> /2 – 0.5	T <sub>cy</sub> /2 + 0.5	ns
t <sub>J</sub>	Cycle-to-Cycle Jitter, 33MHz <sup>(3)</sup>	—	0.25	ns
t <sub>PD</sub>	SYNC Input to Feedback Delay, 28MHz	– 100	400	ps
t <sub>PD</sub>	SYNC Input to Feedback Delay, 33MHz, 50Ω to 1.5V	– 100	400	ps
t <sub>LOCK</sub>	SYNC to Phase Lock	—	10	ms
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time, $\overline{RST}$ LOW to HIGH <sup>(2)</sup>	0	7	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time, $\overline{RST}$ HIGH to LOW <sup>(2)</sup>	0	6	ns
t <sub>R</sub> , t <sub>F</sub>	Output Rise/Fall Times, 0.8V to 2V	0.4	1.5	ns

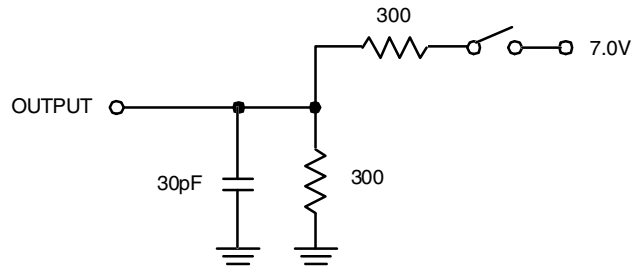
**NOTES:**

1. Skew specifications apply under identical environments (loading, temperature, V<sub>DD</sub>, device speed grade).
2. Measured in open loop mode PLL\_EN = 0.
3. Jitter is characterized using an oscilloscope. Measurement is taken one cycle after jitter. Jitter is characterized but not tested. See FREQUENCY SELECTION TABLE for information on proper FREQ\_SEL level for specified input frequencies.

## TEST LOAD



TEST CIRCUIT 1



TEST CIRCUIT 2

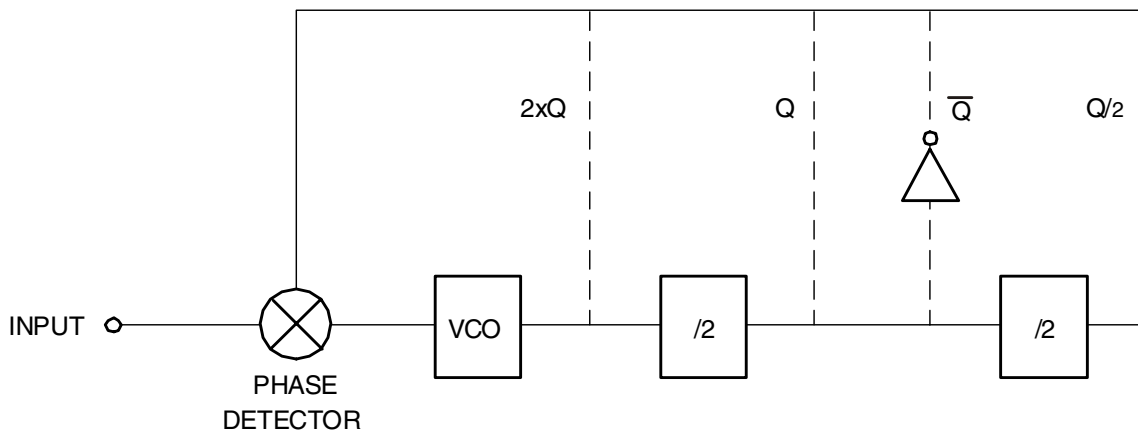
TEST CIRCUIT 2 is used for output enable/disable parameters.  
 TEST CIRCUIT 1 is used for all other timing parameters.

## PLL OPERATION

The Phase Locked Loop (PLL) circuit included in the QS5917T provides for replication of incoming SYNC clock signals. Any manipulation of that signal, such as frequency multiplying or inversion is performed by digital logic following the PLL (see the block diagram). The key advantage of the

PLL circuit is to provide an effective zero propagation delay between the output and input signals. In fact, adding delay circuits in the feedback path, 'propagation delay' can even be negative! A simplified schematic of the QS5917T PLL circuit is shown below.

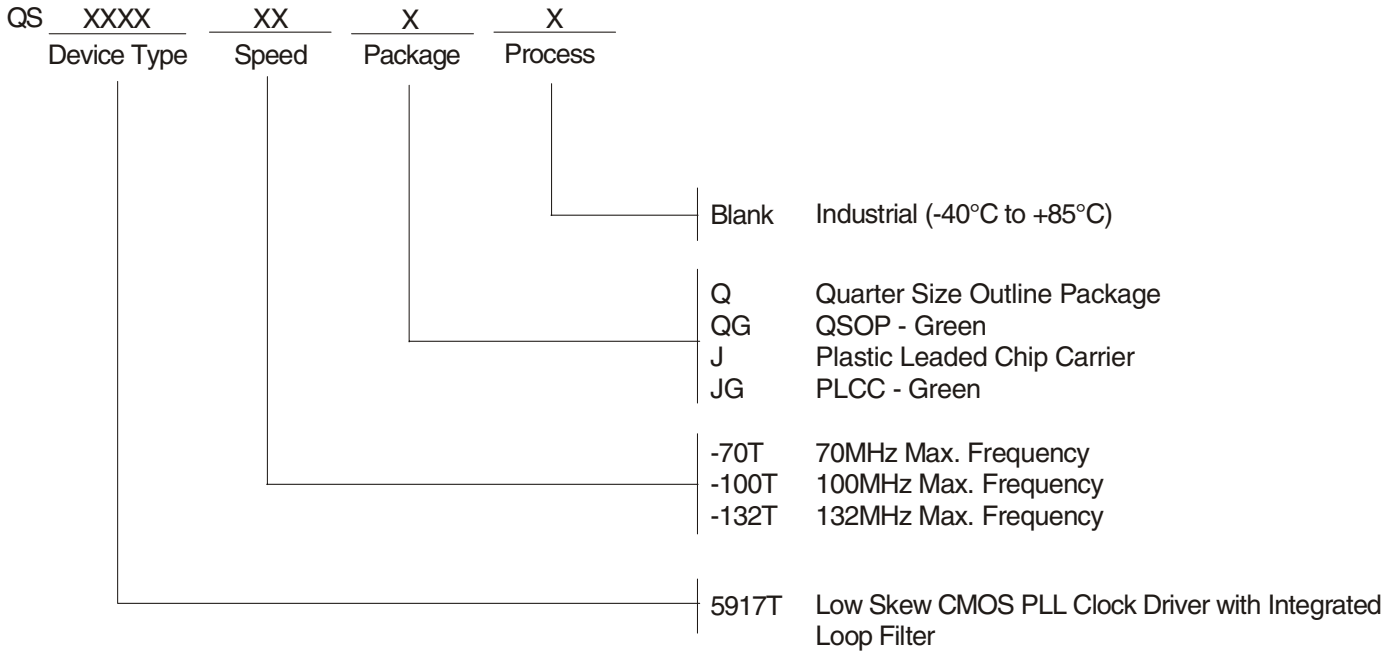
## SIMPLIFIED DIAGRAM OF QS5917T FEEDBACK



The phase difference between the output and the input frequencies feeds the VCO which drives the outputs. Whichever output is fed back, it will stabilize at the same frequency as the input. Hence, this is a true negative feedback closed loop system. In most applications, the output will optimally have zero phase shift with respect to the input. In fact, the internal loop filter on the QS5917T typically provides within 150ps of phase shift between input and output.

If the user wishes to vary the phase difference (typically to compensate for backplane delays), this is most easily accomplished by adding delay circuits to the feedback path. The respective output used for feedback will be advanced by the amount of delay in the feedback path. All other outputs will retain their proper relationships to that output.

*ORDERING INFORMATION*



*REVISION HISTORY*

1/7/14 Product Discontinuation Notice - Last time buy expires October 28, 2014  
 PDN# CQ-13-02



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