ANALOG DEVICES

LC²MOS Precision 5 V/3 V Quad SPST Switches

ADG511/ADG512/ADG513

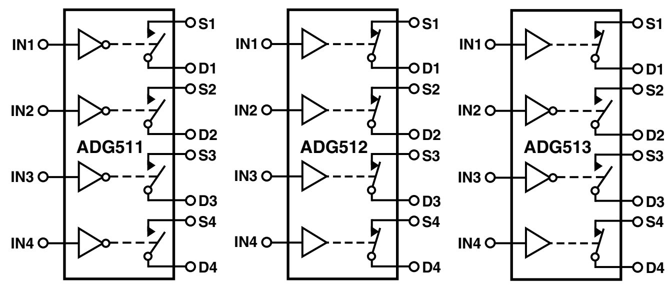
FEATURES

+3 V, +5 V or ±5 V Power Supplies
Ultralow Power Dissipation (<0.5 μW)
Low Leakage (<100 pA)
Low On Resistance (<50 Ω)
Fast Switching Times
Low Charge Injection
TTL/CMOS Compatible
16-Lead DIP or SOIC Package

APPLICATIONS

Battery-Powered Instruments
Single Supply Systems
Remote Powered Equipment
5 V Supply Systems
Computer Peripherals such as Disk Drives
Precision Instrumentation
Audio and Video Switching
Automatic Test Equipment
Precision Data Acquisition
Sample Hold Systems
Communication Systems
Compatible with ±5 V Supply DACs and ADCs such as AD7840/AD7848, AD7870/AD7871/AD7872/AD7874/ AD7875/AD7876/AD7878

FUNCTIONAL BLOCK DIAGRAMS



SWITCHES SHOWN FOR A LOGIC "1" INPUT

GENERAL DESCRIPTION

The ADG511, ADG512 and ADG513 are monolithic CMOS ICs containing four independently selectable analog switches. These switches feature low, well-controlled on resistance and wide analog signal range, making them ideal for precision analog signal switching.

These switch arrays are fabricated using Analog Devices' advanced linear compatible CMOS (LC²MOS) process which offers the additional benefits of low leakage currents, ultralow power dissipation and low capacitance for fast switching speeds with minimum charge injection. These features make the ADG511, ADG512 and ADG513 the optimum choice for a wide variety of signal switching tasks in precision analog signal processing and data acquisition systems.

The ability to operate from single +3 V, +5 V or ±5 V bipolar supplies make the ADG511, ADG512 and ADG513 perfect for use in battery-operated instruments, 4–20 mA loop systems and with the new generation of DACs and ADCs from Analog Devices. The use of 5 V supplies and reduced operating currents give much lower power dissipation than devices operating from ±15 V supplies.

The ADG511, ADG512 and ADG513 contain four independent SPST switches. The ADG511 and ADG512 differ only in that the digital control logic is inverted. The ADG511 switch is turned on with a logic low on the appropriate control input, while a logic high is required for the ADG512. The ADG513 contains two switches whose digital control logic is similar to that of the ADG511 while the logic is inverted in the remaining two switches.

PRODUCT HIGHLIGHTS

1. 5 Volt Single Supply Operation
   The ADG511/ADG512/ADG513 offers high performance, including low on resistance and wide signal range, fully specified and guaranteed with +3 V, ±5 V as well as +5 V supply rails.
2. Ultralow Power Dissipation
   CMOS construction ensures ultralow power dissipation.
3. Low R_{ON}
4. Break-Before-Make Switching
   Switches are guaranteed to have break-before-make operation. This allows multiple outputs to be tied together for multiplexer applications without the possibility of momentary shorting between channels.

REV. C

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ADG511/ADG512/ADG513–SPECIFICATIONS[1]

Dual Supply (V_{DD} = +5 V ± 10%, V_{SS} = –5 V ± 10%, GND = 0 V, unless otherwise noted)

Parameter	B Versions 25°C	B Versions –40°C to +85°C	T Version 25°C	T Version –55°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH						
Analog Signal Range		V_{DD} to V_{SS}		V_{DD} to V_{SS}	V	
R_{ON}	30		30		Ω typ	V_D = ±3.5 V, I_S = –10 mA;
		50		50	Ω max	V_{DD} = +4.5 V, V_{SS} = –4.5 V
LEAKAGE CURRENTS						V_{DD} = +5.5 V, V_{SS} = –5.5 V
Source OFF Leakage I_S (OFF)	±0.025		±0.025		nA typ	V_D = ±4.5 V, V_S = ∓4.5 V;
	±0.1	±2.5	±0.1	±2.5	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.025		±0.025		nA typ	V_D = ±4.5 V, V_S = ∓4.5 V;
	±0.1	±2.5	±0.1	±2.5	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.05		±0.05		nA typ	V_D = V_S = ±4.5 V;
	±0.2	±5	±0.2	±5	nA max	Test Circuit 3
DIGITAL INPUTS						
Input High Voltage, V_{INH}		2.4		2.4	V min	
Input Low Voltage, V_{INL}		0.8		0.8	V max	
Input Current						
I_{INL} or I_{INH}	0.005		0.005		µA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1		±0.1	µA max	
DYNAMIC CHARACTERISTICS[2]						
t_{ON}	200		200		ns typ	R_L = 300 Ω. C_L = 35 pF;
		375		375	ns max	V_S = ±3 V; Test Circuit 4
t_{OFF}	120		120		ns typ	R_L = 300 Ω. C_L = 35 pF;
		150		150	ns max	V_S = ±3 V; Test Circuit 4
Break-Before-Make Time Delay, t_D (ADG513 Only)	100		100		ns typ	R_L = 300 Ω, C_L = 35 pF; V_{S1} = V_{S2} = 3 V; Test Circuit 5
Charge Injection	11		11		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 10 nF; Test Circuit 6
OFF Isolation	68		68		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 7
Channel-to-Channel Crosstalk	85		85		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 8
C_S (OFF)	9		9		pF typ	f = 1 MHz
C_D (OFF)	9		9		pF typ	f = 1 MHz
C_D, C_S (ON)	35		35		pF typ	f = 1 MHz
POWER REQUIREMENTS						
V_{DD}		+4.5/5.5		+4.5/5.5	V min/max	
V_{SS}		–4.5/–5.5		–4.5/–5.5	V min/max	
I_{DD}	0.0001		0.0001		µA typ	V_{DD} = +5.5 V, V_{SS} = –5.5 V
		1		1	µA max	Digital Inputs = 0 V or 5 V
I_{SS}	0.0001		0.0001		µA typ	
		1		1	µA max	

NOTES

[1]Temperature ranges are as follows: B Versions –40°C to +85°C; T Version –55°C to +125°C.

[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

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Single Supply (V_{DD} = 5 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted)

Parameter	B Versions 25°C	B Versions –40°C to +85°C	T Version 25°C	T Version –55°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH						
Analog Signal Range		0 V to V_{DD}		0 V to V_{DD}	V	
R_{ON}	45		45		Ω typ	V_D = 3.5 V, I_S = –10 mA;
		75		75	Ω max	V_{DD} = 4.5 V
LEAKAGE CURRENTS						V_{DD} = 5.5 V
Source OFF Leakage I_S (OFF)	±0.025		±0.025		nA typ	V_D = 4.5/1 V, V_S = 1/4.5 V;
	±0.1	±2.5	±0.1	±2.5	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.025		±0.025		nA typ	V_D = 4.5/1 V, V_S = 1/4.5 V;
	±0.1	±2.5	±0.1	±2.5	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.05		±0.05		nA typ	V_D = V_S = 4.5 V/1 V;
	±0.2	±5	±0.2	±5	nA max	Test Circuit 3
DIGITAL INPUTS						
Input High Voltage, V_{INH}		2.4		2.4	V min	
Input Low Voltage, V_{INL}		0.8		0.8	V max	
Input Current						
I_{INL} or I_{INH}	0.005		0.005		µA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1		±0.1	µA max	
DYNAMIC CHARACTERISTICS[2]						
t_{ON}	250		250		ns typ	R_L = 300 Ω, C_L = 35 pF;
		500		500	ns max	V_S = 2 V; Test Circuit 4
t_{OFF}	50		50		ns typ	R_L = 300 Ω, C_L = 35 pF;
		100		100	ns max	V_S = 2 V; Test Circuit 4
Break-Before-Make Time	200		200		ns typ	R_L = 300 Ω, C_L = 35 pF;
Delay, t_D (ADG513 Only)						V_{S1} = V_{S2} = 2 V; Test Circuit 5
Charge Injection	16		16		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 10 nF;
						Test Circuit 6
OFF Isolation	68		68		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz;
						Test Circuit 7
Channel-to-Channel Crosstalk	85		85		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz;
						Test Circuit 8
C_S (OFF)	9		9		pF typ	f = 1 MHz
C_D (OFF)	9		9		pF typ	f = 1 MHz
C_D, C_S (ON)	35		35		pF typ	f = 1 MHz
POWER REQUIREMENTS						
V_{DD}		4.5/5.5		4.5/5.5	V min/max	
I_{DD}	0.0001		0.0001		µA typ	V_{DD} = 5.5 V
		1		1	µA max	Digital Inputs = 0 V or 5 V

NOTES
[1]Temperature ranges are as follows: B Versions –40°C to +85°C; T Version –55°C to +125°C.
[2]Guaranteed by design, not subject to production test.
Specifications subject to change without notice.

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ADG511/ADG512/ADG513–SPECIFICATIONS[1]

Single Supply (V_{DD} = 3.3 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted)

Parameter	B Version 25°C	B Version 0°C to 70°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	
R_{ON}	200		Ω typ	V_D = 1.5 V, I_S = –1 mA;
		500	Ω max	V_{DD} = 3 V
LEAKAGE CURRENTS				V_{DD} = 3.6 V
Source OFF Leakage I_S (OFF)	±0.025		nA typ	V_D = 2.6/1 V, V_S = 1/2.6 V;
	±0.1	±2.5	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.025		nA typ	V_D = 2.6/1 V, V_S = 1/2.6 V;
	±0.1	±2.5	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.05		nA typ	V_D = V_S = 2.6 V/1 V;
	±0.2	±5	nA max	Test Circuit 3
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}	0.005		µA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	µA max	
DYNAMIC CHARACTERISTICS[2]				
t_{ON}	600		ns typ	R_L = 300 Ω, C_L = 35 pF;
		1200	ns max	V_S = 1 V; Test Circuit 4
t_{OFF}	100		ns typ	R_L = 300 Ω, C_L = 35 pF;
		160	ns max	V_S = 1 V; Test Circuit 4
Break-Before-Make Time	500		ns typ	R_L = 300 Ω, C_L = 35 pF;
Delay, t_D (ADG513 Only)				V_{S1} = V_{S2} = 1 V; Test Circuit 5
Charge Injection	11		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 10 nF; Test Circuit 6
OFF Isolation	68		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 7
Channel-to-Channel Crosstalk	85		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 8
C_S (OFF)	9		pF typ	f = 1 MHz
C_D (OFF)	9		pF typ	f = 1 MHz
C_D, C_S (ON)	35		pF typ	f = 1 MHz
POWER REQUIREMENTS				
V_{DD}		3/3.6	V min/max	
I_{DD}	0.0001		µA typ	V_{DD} = 3.6 V
		1	µA max	Digital Inputs = 0 V or 3 V

NOTES

[1]Temperature range is as follows: B Version –40°C to +85°C.

[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

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ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{DD} to V_{SS} . . . . 44 V
V_{DD} to GND . . . . –0.3 V to +25 V
V_{SS} to GND . . . . +0.3 V to –25 V
Analog, Digital Inputs[2] . . . . V_{SS} – 2 V to V_{DD} + 2 V or 30 mA, Whichever Occurs First
Continuous Current, S or D . . . . 30 mA
Peak Current, S or D . . . . 100 mA
(Pulsed at 1 ms, 10% Duty Cycle max)
Operating Temperature Range
  Industrial (B Version) . . . . –40°C to +85°C
  Extended (T Version) . . . . –55°C to +125°C
Storage Temperature Range . . . . –65°C to +150°C
Junction Temperature . . . . 150°C
Cerdip Package, Power Dissipation . . . . 900 mW
  θ_{JA} Thermal Impedance . . . . 76°C/W
  Lead Temperature, Soldering (10 sec) . . . . 300°C
Plastic Package, Power Dissipation . . . . 470 mW
  θ_{JA} Thermal Impedance . . . . 117°C/W
  Lead Temperature, Soldering (10 sec) . . . . 260°C
SOIC Package, Power Dissipation . . . . 600 mW
  θ_{JA} Thermal Impedance . . . . 77°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec) . . . . 215°C
    Infrared (15 sec) . . . . 220°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.
[2]Overvoltages at IN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG511/ADG512/ADG513 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ORDERING GUIDE

Model[1]	Temperature Range[2]	Package Option[3]
ADG511BN	–40°C to +85°C	N-16
ADG511BR	–40°C to +85°C	R-16A
ADG511ABR[4]	–40°C to +85°C	R-16A
ADG511TQ[4]	–55°C to +125°C	Q-16
ADG512BN	–40°C to +85°C	N-16
ADG512BR	–40°C to +85°C	R-16A
ADG512ABR[4]	–40°C to +85°C	R-16A
ADG513BN	–40°C to +85°C	N-16
ADG513BR	–40°C to +85°C	R-16A
ADG513ABR[4]	–40°C to +85°C	R-16A

NOTES
[1]For availability of MIL-STD-883, Class B processed parts, contact factory.
[2]3.3 V specifications apply over 0°C to 70°C temperature range.
[3]N = Plastic DIP; R = 0.15" Small Outline IC (SOIC); Q = Cerdip.
[4]Trench isolated latch-up proof parts. See Trench Isolation section.

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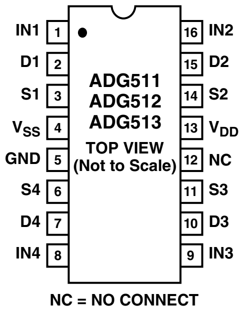
PIN CONFIGURATION (DIP/SOIC)



Truth Table (ADG511/ADG512)

ADG511 In	ADG512 In	Switch Condition
0	1	ON
1	0	OFF

Truth Table (ADG513)

Logic	Switch 1, 4	Switch 2, 3
0	OFF	ON
1	ON	OFF

TERMINOLOGY

V_{DD}	Most Positive Power Supply Potential.
V_{SS}	Most Negative Power Supply Potential in dual supplies. In single supply applications, it may be connected to GND.
GND	Ground (0 V) Reference.
S	Source Terminal. May be an input or output.
D	Drain Terminal. May be an input or output.
IN	Logic Control Input.
R_{ON}	Ohmic Resistance between D and S.
I_S (OFF)	Source Leakage Current with the switch “OFF.”
I_D (OFF)	Drain Leakage Current with the switch “OFF.”
I_D, I_S (ON)	Channel Leakage Current with the switch “ON.”
V_D (V_S)	Analog Voltage on terminals D, S.
C_S (OFF)	“OFF” Switch Source Capacitance.
C_D (OFF)	“OFF” Switch Drain Capacitance.
C_D, C_S (ON)	“ON” Switch Capacitance.
t_{ON}	Delay between applying the digital control input and the output switching on.
t_{OFF}	Delay between applying the digital control input and the output switching off.
t_D	“OFF” or “ON” time measured between the 90% points of both switches when switching from one address state to another.
Crosstalk	A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance.
Off Isolation	A measure of unwanted signal coupling through an “OFF” switch.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.

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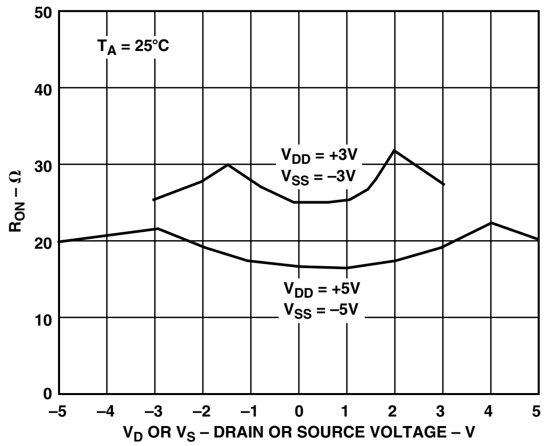
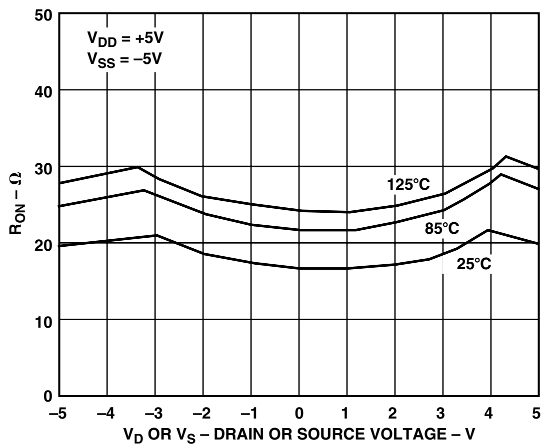
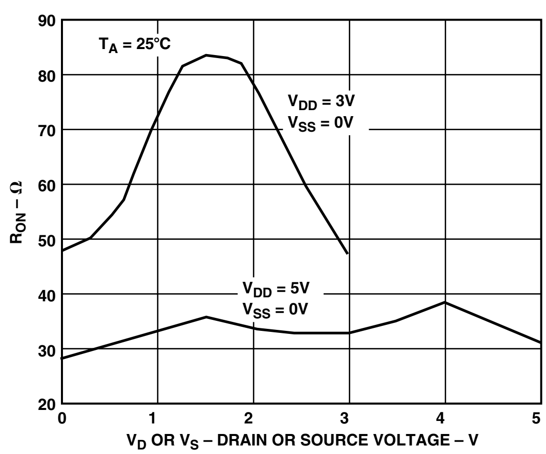


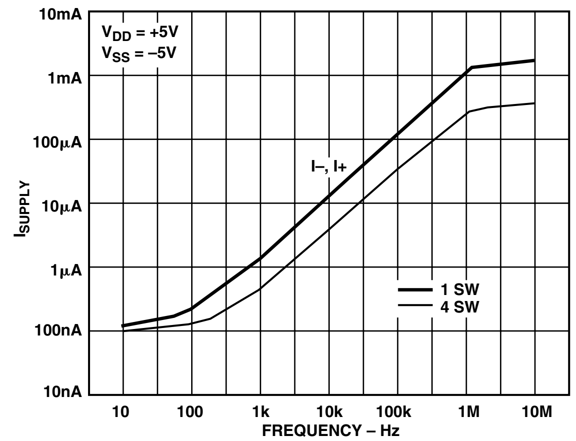
TPC 1. *On Resistance as a Function of V_D (V_S) Dual Supplies*



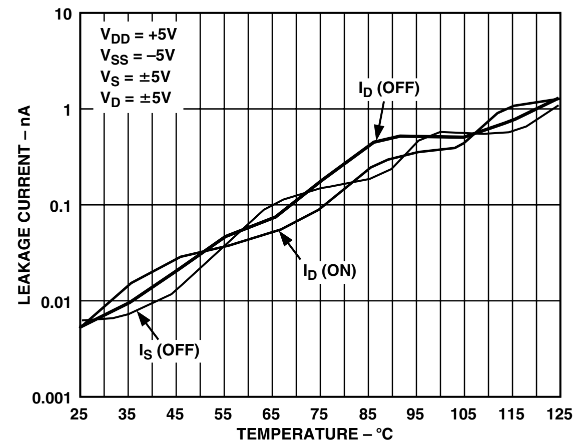
TPC 2. *On Resistance as a Function of V_D (V_S) for Different Temperatures*



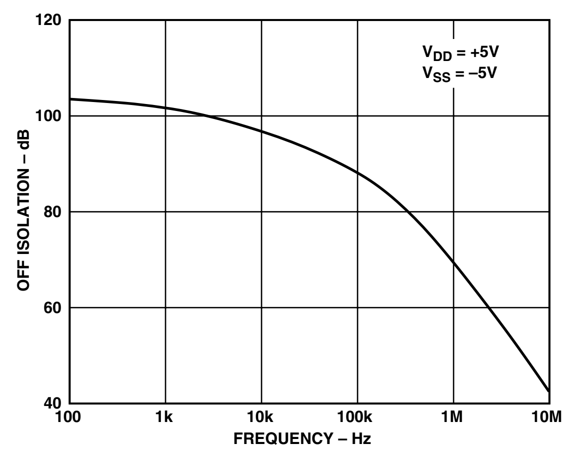
TPC 3. *On Resistance as a Function of V_D (V_S) Single Supply*



TPC 4. *Supply Current vs. Input Switching Frequency*



TPC 5. *Leakage Currents as a Function of Temperature*



TPC 6. *Off Isolation vs. Frequency*

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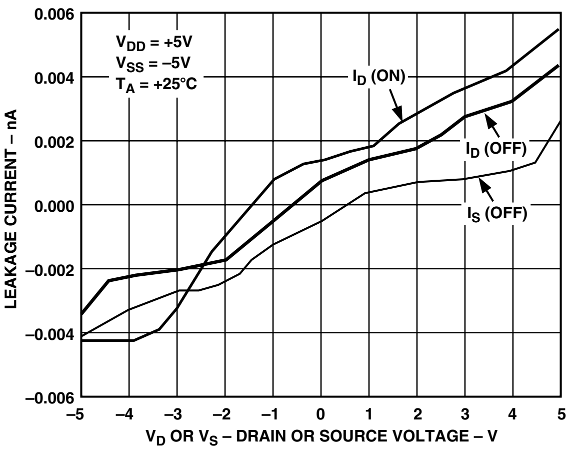
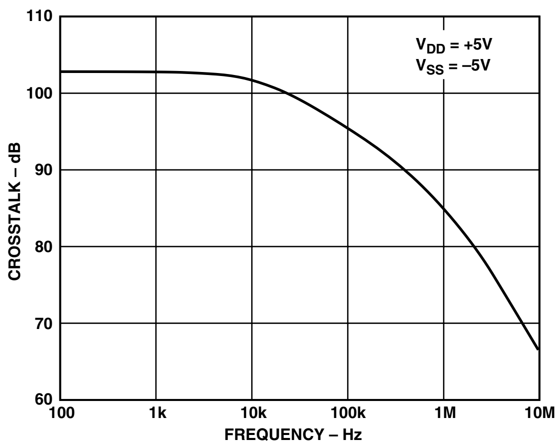


TPC 7. Leakage Currents as a Function of V_D (V_S)



TPC 8. Crosstalk vs. Frequency

APPLICATION

Figure 1 illustrates a precise sample-and-hold circuit. An AD845 is used as the input buffer while the output operational amplifier is an OP07. During the track mode, SW1 is closed and the output V_{OUT} follows the input signal V_{IN}. In the hold mode, SW1 is opened and the signal is held by the hold capacitor C_H.

Due to switch and capacitor leakage, the voltage on the hold capacitor will decrease with time. The ADG511/ADG512/ADG513 minimizes this droop due to its low leakage specifications. The droop rate is further minimized by the use of a polystyrene hold capacitor. The droop rate for the circuit shown is typically 15 µV/µs.

A second switch, SW2, which operates in parallel with SW1, is included in this circuit to reduce pedestal error. Since both switches will be at the same potential, they will have a differential effect on the op amp OP07, which will minimize charge injection effects. Pedestal error is also reduced by the compensation network R_C and C_C. This compensation network also reduces the hold time glitch while optimizing the acquisition time. Using the illustrated op amps and component values, the pedestal error has a maximum value of 5 mV over the ±3 V input range. The acquisition time is 2.5 µs while the settling time is 1.85 µs.

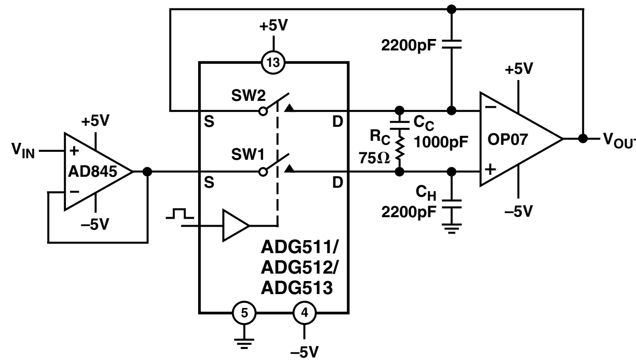


Figure 1. Accurate Sample-and-Hold

TRENCH ISOLATION

The MOS devices that make up the ADG511A/ADG512A/ADG513A are isolated from each other by an oxide layer (trench) (see Figure 2). When the NMOS and PMOS devices are not electrically isolated from each other, there exists the possibility of "latch-up" caused by parasitic junctions between CMOS transistors. Latch-up is caused when P-N junctions that are normally reverse biased, become forward biased, causing large currents to flow. This can be destructive.

CMOS devices are normally isolated from each other by *Junction Isolation*. In Junction Isolation the N and P wells of the CMOS transistors form a diode that is reverse biased under normal operation. However, during overvoltage conditions, this diode becomes forward biased. A Silicon-Controlled Rectifier (SCR)-type circuit is formed by the two transistors, causing a significant amplification of the current that, in turn, leads to latch-up. With Trench Isolation, this diode is removed; the result is a latch-up-proof circuit.

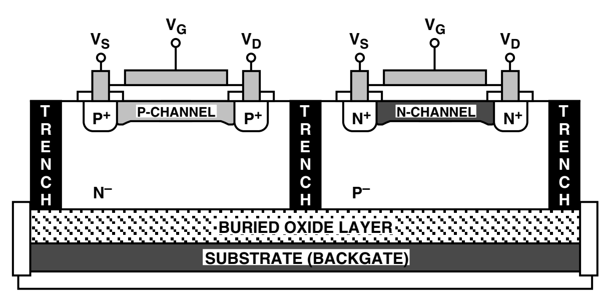


Figure 2. Trench Isolation

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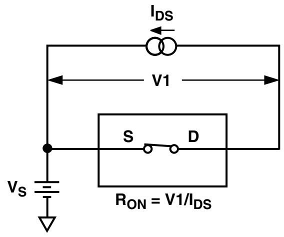
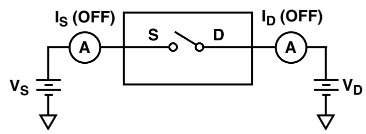
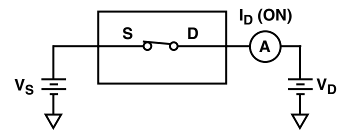
Test Circuits



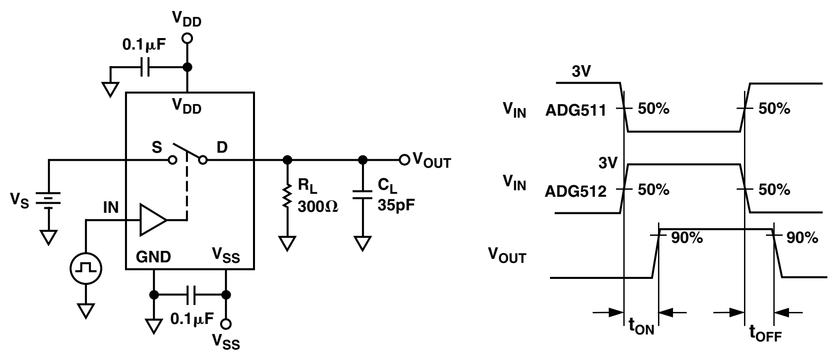
Test Circuit 1. On Resistance



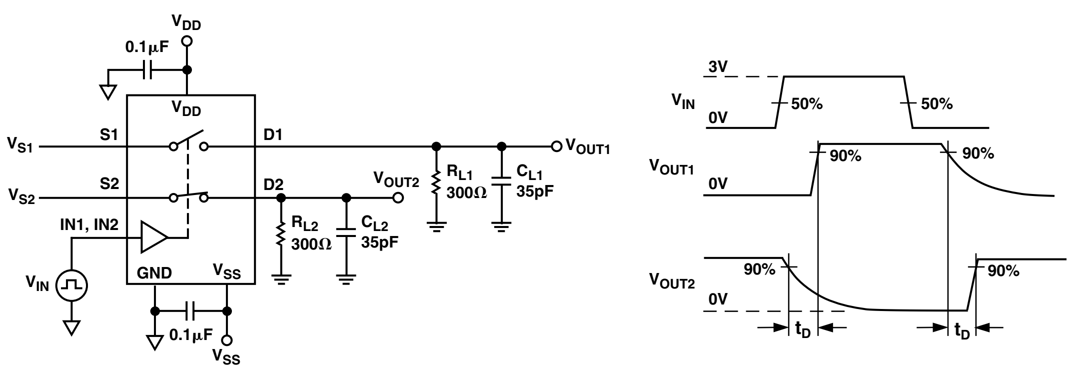
Test Circuit 2. Off Leakage



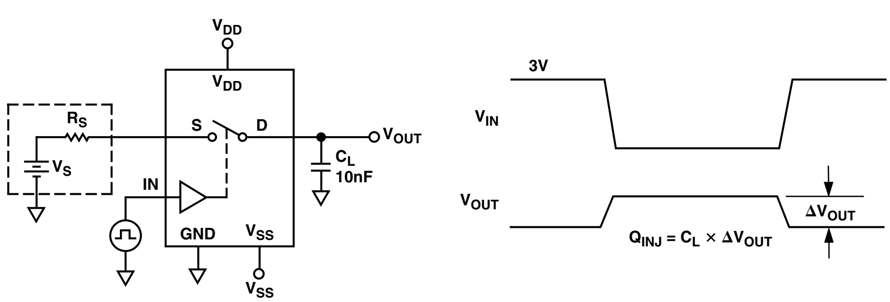
Test Circuit 3. On Leakage



Test Circuit 4. Switching Times



Test Circuit 5. Break-Before-Make Time Delay



Test Circuit 6. Charge Injection

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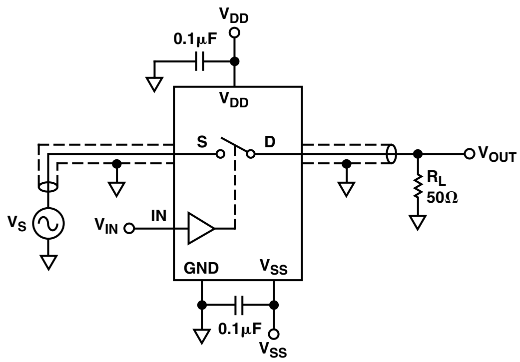
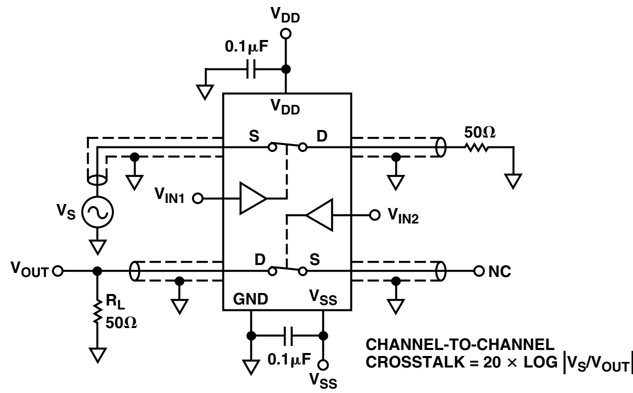


Test Circuit 7. Off Isolation



Test Circuit 8. Channel-to-Channel Crosstalk

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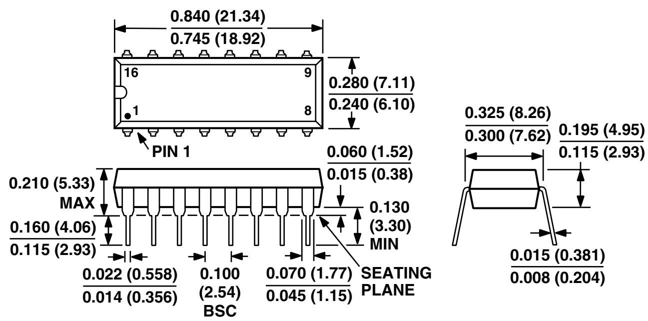
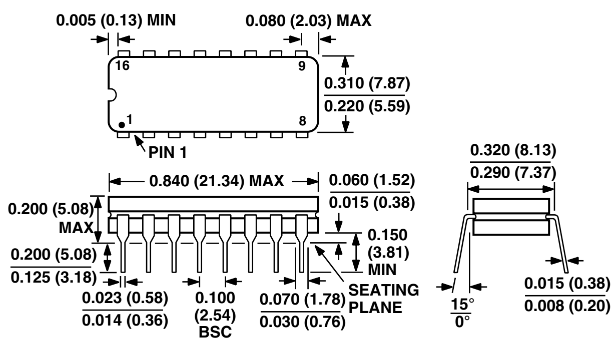
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

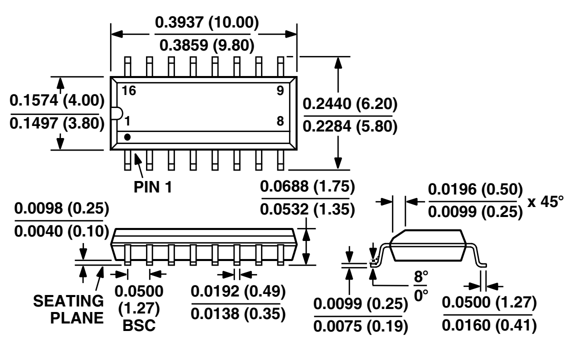
16-Lead Plastic DIP (N-16)



16-Lead Cerdip (Q-16)



16-Lead SOIC (R-16A)



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ADG511/ADG512/ADG513–Revision History

Location **Page**

Data Sheet changed from REV. B to REV. C.

C00036b–0–5/01(C)

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