

# DATA SHEET

**74LVC162245A; 74LVCH162245A**  
16-bit transceiver with direction pin;  
30  $\Omega$  series termination resistors;  
5 V tolerant input/output; 3-state

Product specification  
Supersedes data of 1998 Feb 17

2003 Dec 08

# 16-bit transceiver with direction pin; 30 $\Omega$ series termination resistors; 5 V tolerant input/output; 3-state

## 74LVC162245A; 74LVCH162245A

### FEATURES

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 to 3.6 V
- CMOS low power consumption
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- Inputs accept voltages up to 5.5 V
- Integrated 30  $\Omega$  termination resistors
- High-impedance when  $V_{CC} = 0$  V
- All data inputs have bushold (74LVCH162245A only)
- Complies with JEDEC standard no. 8-1A
- ESD protection:  
HBM EIA/JESD22-A114-A exceeds 2000 V  
MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from  $-40$  to  $+85$  °C and  $-40$  to  $+125$  °C.

### DESCRIPTION

The 74LVC(H)162245A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 or 5 V devices. In 3-state operation, outputs can handle 5 V. These features allow the use of these devices as translators in a mixed 3.3 and 5 V environment.

The 74LVC(H)162245A is a 16-bit transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions.

The 74LVC(H)162245A features two output enable ( $\overline{nOE}$ ) inputs for easy cascading and two send/receive ( $nDIR$ ) inputs for direction control.  $\overline{nOE}$  controls the outputs so that the buses are effectively isolated. This device can be used as two 8-bit transceivers or one 16-bit transceiver.

The 74LVCH162245A bushold data inputs eliminates the need for external pull-up resistors to hold unused inputs.

The 74LVC(H)162245A is designed with 30  $\Omega$  series termination resistors in both HIGH and LOW output stages to reduce line noise.

### QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25$  °C;  $t_r = t_f \leq 2.5$  ns.

| SYMBOL            | PARAMETER                                | CONDITIONS                      | TYPICAL | UNIT |
|-------------------|--|---------------------------------|---------|------|
| $t_{PHL}/t_{PLH}$ | propagation delay nAn to nBn; nBn to nAn | $C_L = 50$ pF; $V_{CC} = 3.3$ V | 3.3     | ns   |
| $C_I$             | input capacitance                        |                                 | 5.0     | pF   |
| $C_{I/O}$         | input/output capacitance                 |                                 | 10      | pF   |
| $C_{PD}$          | power dissipation capacitance            | $V_{CC} = 3.3$ V; notes 1 and 2 | 28      | pF   |

### Note

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu$ W).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in Volts;

$N$  = total load switching outputs;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

2. The condition is  $V_I = \text{GND to } V_{CC}$ .

16-bit transceiver with direction pin; 30  $\Omega$  series  
 termination resistors; 5 V tolerant input/output; 3-state

74LVC162245A;  
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### FUNCTION TABLE

See note 1.

| INPUT                   |      | OUTPUT |        |
|-------------------------|------|--------|--------|
| $\overline{\text{nOE}}$ | nDIR | nAn    | nBn    |
| L                       | L    | A = B  | inputs |
| L                       | H    | inputs | B = A  |
| H                       | X    | Z      | Z      |

### Note

1. H = HIGH voltage level;  
 L = LOW voltage level;  
 X = don't care;  
 Z = high-impedance OFF-state.

### ORDERING INFORMATION

| TYPE NUMBER      | PACKAGE           |      |         |          |          |
|------------------|-------------------|------|---------|----------|----------|
|                  | TEMPERATURE RANGE | PINS | PACKAGE | MATERIAL | CODE     |
| 74LVC162245ADL   | -40 to +125 °C    | 48   | SSOP48  | plastic  | SOT370-1 |
| 74LVCH162245ADL  | -40 to +125 °C    | 48   | SSOP48  | plastic  | SOT370-1 |
| 74LVC162245ADGG  | -40 to +125 °C    | 48   | TSSOP48 | plastic  | SOT362-1 |
| 74LVCH162245ADGG | -40 to +125 °C    | 48   | TSSOP48 | plastic  | SOT362-1 |

16-bit transceiver with direction pin; 30 Ω series termination resistors; 5 V tolerant input/output; 3-state

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**PINNING**

| SYMBOL          | PIN                           | DESCRIPTION                      |
|-----------------|-------------------------------|----------------------------------|
| 1DIR            | 1                             | direction control input          |
| n.c.            | –                             | not connected                    |
| 1B0             | 2                             | data input/output                |
| 1B1             | 3                             | data input/output                |
| GND             | 4, 10, 15, 21, 28, 34, 39, 45 | ground (0 V)                     |
| 1B2             | 5                             | data input/output                |
| 1B3             | 6                             | data input/output                |
| V <sub>CC</sub> | 7, 18, 31, 42                 | supply voltage                   |
| 1B4             | 8                             | data input/output                |
| 1B5             | 9                             | data input/output                |
| 1B6             | 11                            | data input/output                |
| 1B7             | 12                            | data input/output                |
| 2B0             | 13                            | data input/output                |
| 2B1             | 14                            | data input/output                |
| 2B2             | 16                            | data input/output                |
| 2B3             | 17                            | data input/output                |
| 2B4             | 19                            | data input/output                |
| 2B5             | 20                            | data input/output                |
| 2B6             | 22                            | data input/output                |
| 2B7             | 23                            | data input/output                |
| 2DIR            | 24                            | direction control input          |
| 2OE             | 25                            | output enable input (active LOW) |
| 2A7             | 26                            | data input/output                |
| 2A6             | 27                            | data input/output                |
| 2A5             | 29                            | data input/output                |
| 2A4             | 30                            | data input/output                |
| 2A3             | 32                            | data input/output                |
| 2A2             | 33                            | data input/output                |
| 2A1             | 35                            | data input/output                |
| 2A0             | 36                            | data input/output                |
| 1A7             | 37                            | data input/output                |
| 1A6             | 38                            | data input/output                |

| SYMBOL | PIN | DESCRIPTION                      |
|--------|-----|----------------------------------|
| 1A5    | 40  | data input/output                |
| 1A4    | 41  | data input/output                |
| 1A3    | 43  | data input/output                |
| 1A2    | 44  | data input/output                |
| 1A1    | 46  | data input/output                |
| 1A0    | 47  | data input/output                |
| 1OE    | 48  | output enable input (active LOW) |

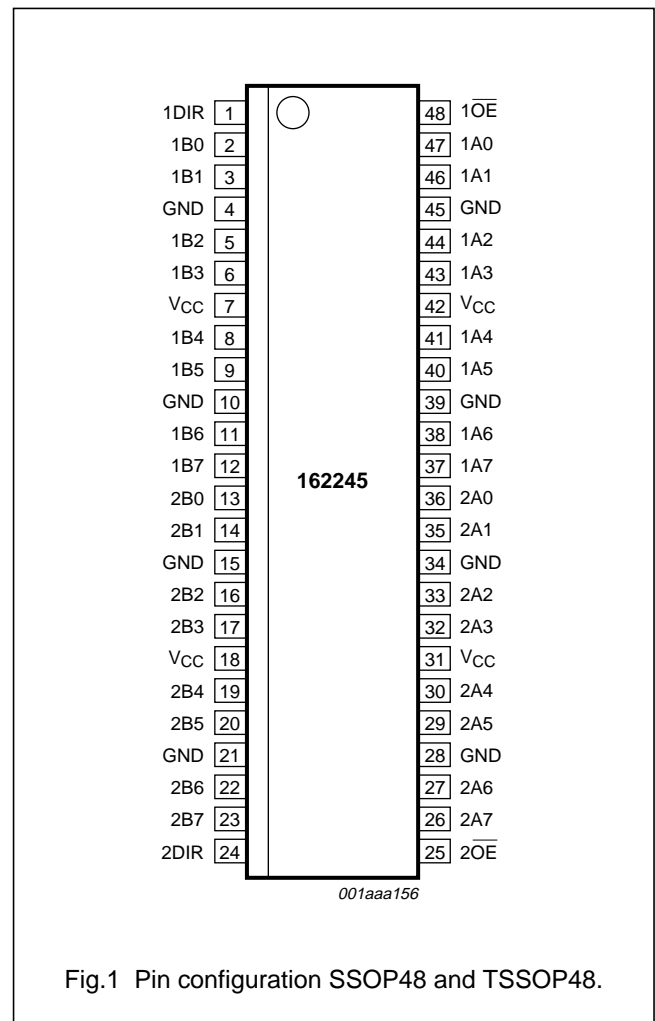


Fig.1 Pin configuration SSOP48 and TSSOP48.

16-bit transceiver with direction pin; 30 Ω series termination resistors; 5 V tolerant input/output; 3-state

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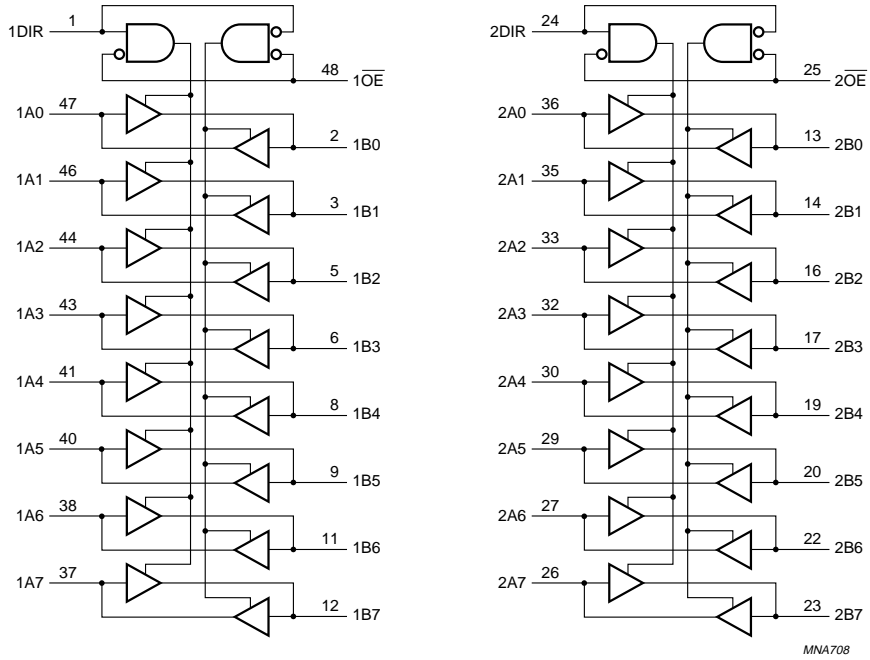
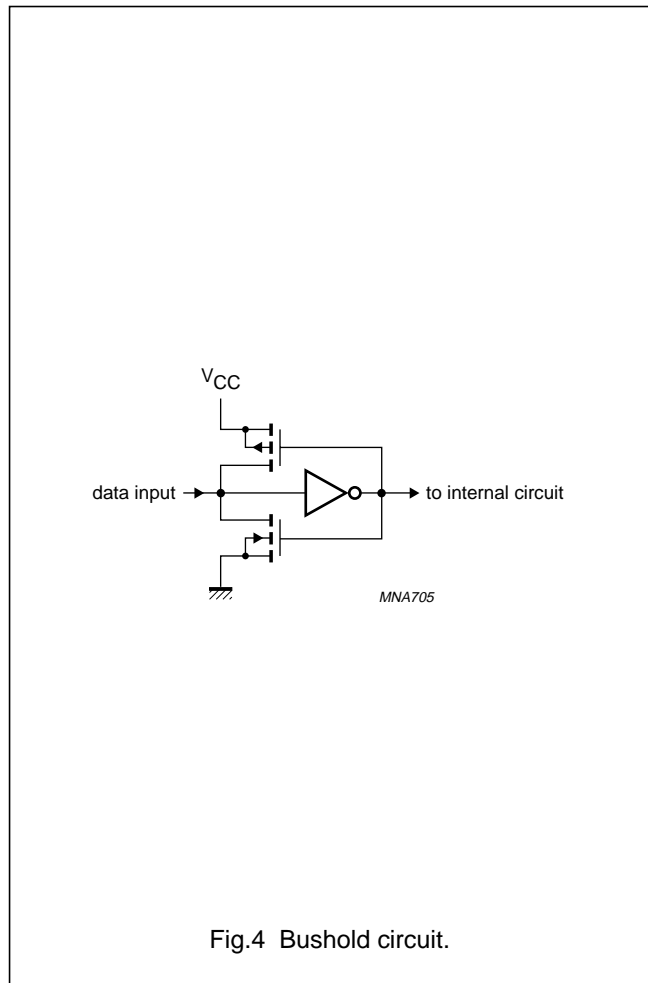
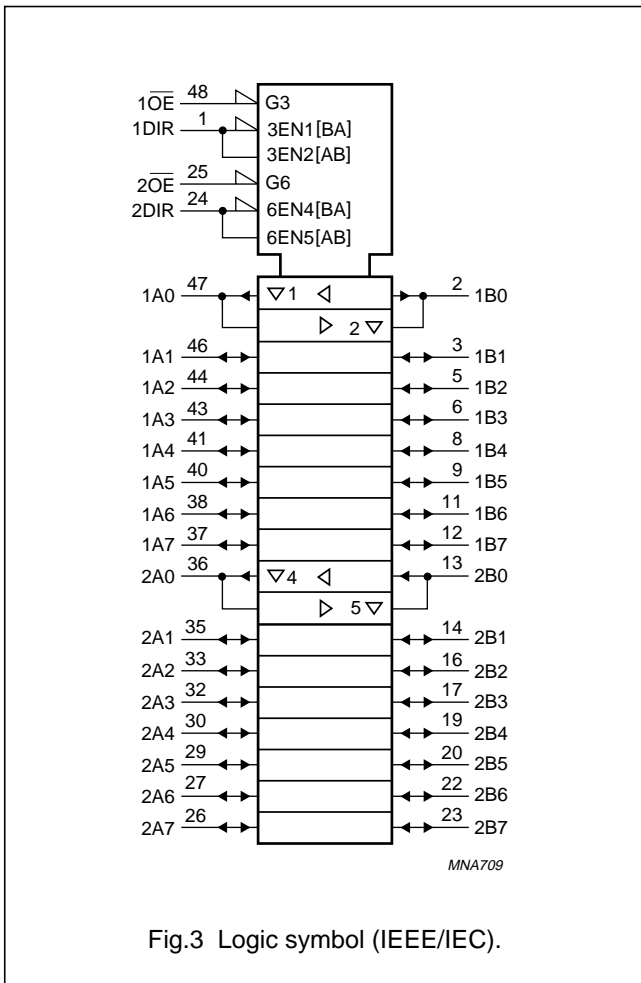


Fig.2 Logic symbol.

16-bit transceiver with direction pin; 30 Ω series termination resistors; 5 V tolerant input/output; 3-state

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#### RECOMMENDED OPERATING CONDITIONS

| SYMBOL     | PARAMETER                 | CONDITIONS                    | MIN. | MAX.     | UNIT               |
|------------|---------------------------|-------------------------------|------|----------|--------------------|
| $V_{CC}$   | supply voltage            | for maximum speed performance | 2.7  | 3.6      | V                  |
|            |                           | for low voltage applications  | 1.2  | 3.6      | V                  |
| $V_I$      | input voltage             |                               | 0    | 5.5      | V                  |
| $V_O$      | output voltage            | output HIGH or LOW state      | 0    | $V_{CC}$ | V                  |
|            |                           | output 3-state                | 0    | 5.5      | V                  |
| $T_{amb}$  | ambient temperature       | in free air                   | -40  | +125     | $^{\circ}\text{C}$ |
| $t_r, t_f$ | input rise and fall times | $V_{CC} = 1.2$ to $2.7$ V     | 0    | 20       | ns/V               |
|            |                           | $V_{CC} = 2.7$ to $3.6$ V     | 0    | 10       | ns/V               |

#### LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

| SYMBOL            | PARAMETER                     | CONDITIONS  | MIN. | MAX.           | UNIT               |
|-------------------|-------------------------------|---|------|----------------|--------------------|
| $V_{CC}$          | supply voltage                |   | -0.5 | +6.5           | V                  |
| $I_{IK}$          | input diode current           | $V_I < 0$   | -    | -50            | mA                 |
| $V_I$             | input voltage                 | note 1  | -0.5 | +6.5           | V                  |
| $I_{OK}$          | output diode current          | $V_O > V_{CC}$ or $V_O < 0$                           | -    | $\pm 50$       | mA                 |
| $V_O$             | output voltage                | output HIGH or LOW state; note 1                      | -0.5 | $V_{CC} + 0.5$ | V                  |
|                   |                               | output 3-state; note 1                                | -0.5 | +6.5           | V                  |
| $I_O$             | output source or sink current | $V_O = 0$ to $V_{CC}$                                 | -    | $\pm 50$       | mA                 |
| $I_{CC}, I_{GND}$ | $V_{CC}$ or GND current       |   | -    | $\pm 100$      | mA                 |
| $T_{stg}$         | storage temperature           |   | -65  | +150           | $^{\circ}\text{C}$ |
| $P_{tot}$         | power dissipation             | $T_{amb} = -40$ to $+125$ $^{\circ}\text{C}$ ; note 2 | -    | 500            | mW                 |

#### Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. Above 60  $^{\circ}\text{C}$  the value of  $P_{tot}$  derates linearly with 5.5 mW/K.

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### DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| SYMBOL                                 | PARAMETER   | TEST CONDITIONS  |                     | MIN.                  | TYP. <sup>(1)</sup> | MAX.     | UNIT    |
|--|---|--|---------------------|-----------------------|---------------------|----------|---------|
|  |   | OTHER  | V <sub>CC</sub> (V) |                       |                     |          |         |
| <b>T<sub>amb</sub> = -40 to +85 °C</b> |   |  |                     |                       |                     |          |         |
| V <sub>IH</sub>                        | HIGH-level input voltage                          |  | 1.2                 | V <sub>CC</sub>       | –                   | –        | V       |
|  |   |  | 2.7 to 3.6          | 2.0                   | –                   | –        | V       |
| V <sub>IL</sub>                        | LOW-level input voltage                           |  | 1.2                 | –                     | –                   | GND      | V       |
|  |   |  | 2.7 to 3.6          | –                     | –                   | 0.8      | V       |
| V <sub>OH</sub>                        | HIGH-level output voltage                         | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub><br>I <sub>O</sub> = -100 $\mu$ A                     | 2.7 to 3.6          | V <sub>CC</sub> - 0.2 | V <sub>CC</sub>     | –        | V       |
|  |   | I <sub>O</sub> = -6 mA   | 2.7                 | V <sub>CC</sub> - 0.5 | –                   | –        | V       |
|  |   | I <sub>O</sub> = -12 mA  | 3.0                 | V <sub>CC</sub> - 0.8 | –                   | –        | V       |
| V <sub>OL</sub>                        | LOW-level output voltage                          | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub><br>I <sub>O</sub> = 100 $\mu$ A                      | 2.7 to 3.6          | –                     | 0                   | 0.20     | V       |
|  |   | I <sub>O</sub> = 6 mA  | 2.7                 | –                     | –                   | 0.40     | V       |
|  |   | I <sub>O</sub> = 12 mA   | 3.0                 | –                     | –                   | 0.55     | V       |
| I <sub>LI</sub>                        | input leakage current                             | V <sub>I</sub> = 5.5 V or GND;<br>note 2   | 3.6                 | –                     | $\pm$ 0.1           | $\pm$ 5  | $\mu$ A |
| I <sub>OZ</sub>                        | 3-state output OFF-state current                  | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ;<br>V <sub>O</sub> = 5.5 V or GND;<br>notes 2 and 3 | 3.6                 | –                     | $\pm$ 0.1           | $\pm$ 5  | $\mu$ A |
| I <sub>off</sub>                       | power-off leakage supply current                  | V <sub>I</sub> or V <sub>O</sub> = 5.5 V   | 0.0                 | –                     | $\pm$ 0.1           | $\pm$ 10 | $\mu$ A |
| I <sub>CC</sub>                        | quiescent supply current                          | V <sub>I</sub> = V <sub>CC</sub> or GND;<br>I <sub>O</sub> = 0   | 3.6                 | –                     | 0.1                 | 20       | $\mu$ A |
| $\Delta$ I <sub>CC</sub>               | additional quiescent supply current per input pin | V <sub>I</sub> = V <sub>CC</sub> - 0.6 V;<br>I <sub>O</sub> = 0  | 2.7 to 3.6          | –                     | 5                   | 500      | $\mu$ A |
| I <sub>BHL</sub>                       | bushold LOW sustaining current                    | V <sub>I</sub> = 0.8 V;<br>notes 4 and 5   | 3.0                 | 75                    | –                   | –        | $\mu$ A |
| I <sub>BHH</sub>                       | bushold HIGH sustaining current                   | V <sub>I</sub> = 2.0 V;<br>notes 4 and 5   | 3.0                 | -75                   | –                   | –        | $\mu$ A |
| I <sub>BHLO</sub>                      | bushold LOW overdrive current                     | notes 4 and 6  | 3.6                 | 500                   | –                   | –        | $\mu$ A |
| I <sub>BHNO</sub>                      | bushold HIGH overdrive current                    | notes 4 and 6  | 3.6                 | -500                  | –                   | –        | $\mu$ A |



16-bit transceiver with direction pin; 30  $\Omega$  series  
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| SYMBOL                                  | PARAMETER   | TEST CONDITIONS   |                     | MIN.                   | TYP. <sup>(1)</sup> | MAX.     | UNIT    |
|---|---|---|---------------------|------------------------|---------------------|----------|---------|
|   |   | OTHER   | V <sub>CC</sub> (V) |                        |                     |          |         |
| <b>T<sub>amb</sub> = -40 to +125 °C</b> |   |   |                     |                        |                     |          |         |
| V <sub>IH</sub>                         | HIGH-level input voltage                          |   | 1.2                 | V <sub>CC</sub>        | –                   | –        | V       |
|   |   |   | 2.7 to 3.6          | 2.0                    | –                   | –        | V       |
| V <sub>IL</sub>                         | LOW-level input voltage                           |   | 1.2                 | –                      | –                   | GND      | V       |
|   |   |   | 2.7 to 3.6          | –                      | –                   | 0.8      | V       |
| V <sub>OH</sub>                         | HIGH-level output voltage                         | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub><br>I <sub>O</sub> = -100 $\mu$ A<br>I <sub>O</sub> = -6 mA<br>I <sub>O</sub> = -12 mA | 2.7 to 3.6          | V <sub>CC</sub> - 0.3  | –                   | –        | V       |
|   |   |   | 2.7                 | V <sub>CC</sub> - 0.65 | –                   | –        | V       |
|   |   |   | 3.0                 | V <sub>CC</sub> - 1    | –                   | –        | V       |
| V <sub>OL</sub>                         | LOW-level output voltage                          | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub><br>I <sub>O</sub> = 100 $\mu$ A<br>I <sub>O</sub> = 6 mA<br>I <sub>O</sub> = 12 mA    | 2.7 to 3.6          | –                      | –                   | 0.3      | V       |
|   |   |   | 2.7                 | –                      | –                   | 0.6      | V       |
|   |   |   | 3.0                 | –                      | –                   | 0.8      | V       |
| I <sub>LI</sub>                         | input leakage current                             | V <sub>I</sub> = 5.5 V or GND;<br>note 2  | 3.6                 | –                      | –                   | $\pm$ 20 | $\mu$ A |
| I <sub>OZ</sub>                         | 3-state output OFF-state current                  | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ;<br>V <sub>O</sub> = 5.5 V or GND;<br>notes 2 and 3                                  | 3.6                 | –                      | –                   | $\pm$ 20 | $\mu$ A |
| I <sub>off</sub>                        | power-off leakage supply current                  | V <sub>I</sub> or V <sub>O</sub> = 5.5 V  | 0.0                 | –                      | –                   | $\pm$ 20 | $\mu$ A |
| I <sub>CC</sub>                         | quiescent supply current                          | V <sub>I</sub> = V <sub>CC</sub> or GND;<br>I <sub>O</sub> = 0  | 3.6                 | –                      | –                   | 80       | $\mu$ A |
| $\Delta$ I <sub>CC</sub>                | additional quiescent supply current per input pin | V <sub>I</sub> = V <sub>CC</sub> - 0.6 V;<br>I <sub>O</sub> = 0   | 2.7 to 3.6          | –                      | –                   | 5000     | $\mu$ A |
| I <sub>BHL</sub>                        | bushold LOW sustaining current                    | V <sub>I</sub> = 0.8 V;<br>notes 4 and 5  | 3.0                 | 60                     | –                   | –        | $\mu$ A |
| I <sub>BHH</sub>                        | bushold HIGH sustaining current                   | V <sub>I</sub> = 2.0 V;<br>notes 4 and 5  | 3.0                 | -60                    | –                   | –        | $\mu$ A |
| I <sub>BHLO</sub>                       | bushold LOW overdrive current                     | notes 4 and 6   | 3.6                 | 500                    | –                   | –        | $\mu$ A |
| I <sub>BHHO</sub>                       | bushold HIGH overdrive current                    | notes 4 and 6   | 3.6                 | -500                   | –                   | –        | $\mu$ A |

#### Notes

1. All typical values are measured at V<sub>CC</sub> = 3.3 V and T<sub>amb</sub> = 25 °C.
2. For bushold parts, the bushold circuit is switched off when V<sub>I</sub> > V<sub>CC</sub> allowing 5.5 V on the input terminal.
3. For I/O ports the parameter I<sub>OZ</sub> includes the input leakage current.
4. Valid for data inputs of bushold parts (LVCH162245A) only. For data inputs only, control inputs do not have a bushold circuit.
5. The specified sustaining current at the data input holds the input below the specified V<sub>I</sub> level.
6. The specified overdrive current at the data input forces the data input to the opposite logic input state.

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### AC CHARACTERISTICS

GND = 0 V;  $t_r = t_f \leq 2.5$  ns.

| SYMBOL                                  | PARAMETER   | TEST CONDITIONS  |                     | MIN. | TYP. <sup>(1)</sup> | MAX. | UNIT |
|---|---|------------------|---------------------|------|---------------------|------|------|
|   |   | WAVEFORMS        | V <sub>CC</sub> (V) |      |                     |      |      |
| <b>T<sub>amb</sub> = -40 to +85 °C</b>  |   |                  |                     |      |                     |      |      |
| t <sub>PHL</sub> /t <sub>PLH</sub>      | propagation delay nAn to nBn;<br>nBn to nAn                                       | see Figs 5 and 7 | 1.2                 | –    | 12                  | –    | ns   |
|   |   |                  | 2.7                 | 1.0  | 4.2                 | 6.7  | ns   |
|   |   |                  | 3.0 to 3.6          | 1.0  | 3.3 <sup>(2)</sup>  | 5.7  | ns   |
| t <sub>PZH</sub> /t <sub>PZL</sub>      | 3-state output enable time n $\overline{OE}$<br>to nAn; n $\overline{OE}$ to nBn  | see Figs 6 and 7 | 1.2                 | –    | 18                  | –    | ns   |
|   |   |                  | 2.7                 | 1.5  | 5.1                 | 8.5  | ns   |
|   |   |                  | 3.0 to 3.6          | 1.0  | 3.4 <sup>(2)</sup>  | 7.5  | ns   |
| t <sub>PHZ</sub> /t <sub>PLZ</sub>      | 3-state output disable time n $\overline{OE}$<br>to nAn; n $\overline{OE}$ to nBn | see Figs 6 and 7 | 1.2                 | –    | 10                  | –    | ns   |
|   |   |                  | 2.7                 | 1.5  | 3.5                 | 7.5  | ns   |
|   |   |                  | 3.0 to 3.6          | 1.5  | 3.3 <sup>(2)</sup>  | 6.5  | ns   |
| <b>T<sub>amb</sub> = -40 to +125 °C</b> |   |                  |                     |      |                     |      |      |
| t <sub>PHL</sub> /t <sub>PLH</sub>      | propagation delay nAn to nBn;<br>nBn to nAn                                       | see Figs 5 and 7 | 1.2                 | –    | –                   | –    | ns   |
|   |   |                  | 2.7                 | 1.0  | –                   | 8.5  | ns   |
|   |   |                  | 3.0 to 3.6          | 1.0  | –                   | 9.5  | ns   |
| t <sub>PZH</sub> /t <sub>PZL</sub>      | 3-state output enable time n $\overline{OE}$<br>to nAn; n $\overline{OE}$ to nBn  | see Figs 6 and 7 | 1.2                 | –    | –                   | –    | ns   |
|   |   |                  | 2.7                 | 1.5  | –                   | 7.5  | ns   |
|   |   |                  | 3.0 to 3.6          | 1.0  | –                   | 9.5  | ns   |
| t <sub>PHZ</sub> /t <sub>PLZ</sub>      | 3-state output disable time n $\overline{OE}$<br>to nAn; n $\overline{OE}$ to nBn | see Figs 6 and 7 | 1.2                 | –    | –                   | –    | ns   |
|   |   |                  | 2.7                 | 1.5  | –                   | 11.0 | ns   |
|   |   |                  | 3.0 to 3.6          | 1.5  | –                   | 8.5  | ns   |

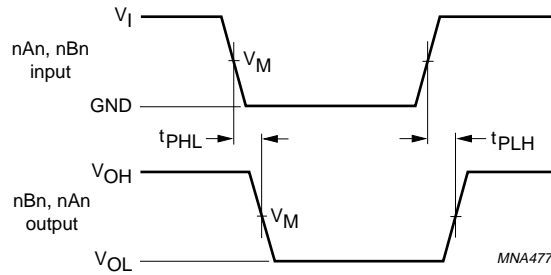
### Notes

1. All typical values are measured at T<sub>amb</sub> = 25 °C.
2. These typical values are measured at V<sub>CC</sub> = 3.3 V and T<sub>amb</sub> = 25 °C.

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AC WAVEFORMS



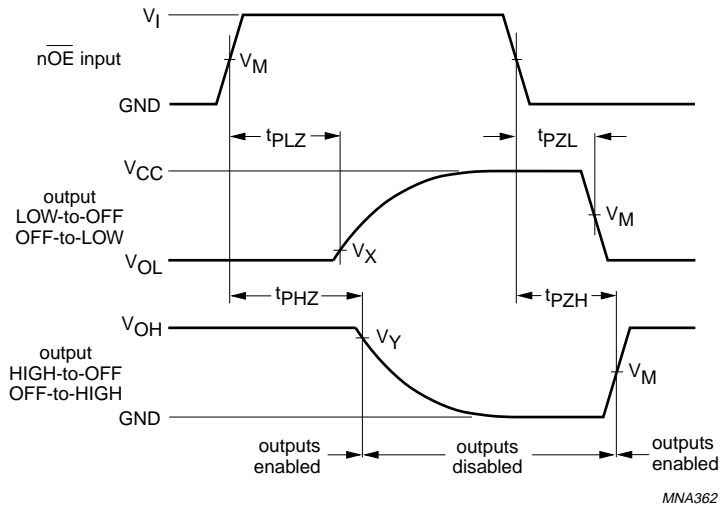
| V <sub>CC</sub> | V <sub>M</sub>        | INPUT           |                                 |
|-----------------|-----------------------|-----------------|---------------------------------|
|                 |                       | V <sub>I</sub>  | t <sub>r</sub> = t <sub>f</sub> |
| 1.2 V           | 0.5 × V <sub>CC</sub> | V <sub>CC</sub> | ≤ 2.5 ns                        |
| 2.7 V           | 1.5 V                 | 2.7 V           | ≤ 2.5 ns                        |
| 3.0 to 3.6 V    | 1.5 V                 | 2.7 V           | ≤ 2.5 ns                        |

V<sub>OL</sub> and V<sub>OH</sub> are typical output voltage drop that occur with the output load.

Fig.5 The input (nAn, nBn) to outputs (nBn, nAn) propagation delays.

16-bit transceiver with direction pin; 30 Ω series termination resistors; 5 V tolerant input/output; 3-state

74LVC162245A;  
74LVCH162245A



| V <sub>CC</sub> | V <sub>M</sub>        | INPUT           |                                 |
|-----------------|-----------------------|-----------------|---------------------------------|
|                 |                       | V <sub>I</sub>  | t <sub>r</sub> = t <sub>f</sub> |
| 1.2 V           | 0.5 × V <sub>CC</sub> | V <sub>CC</sub> | ≤ 2.5 ns                        |
| 2.7 V           | 1.5 V                 | 2.7 V           | ≤ 2.5 ns                        |
| 3.0 to 3.6 V    | 1.5 V                 | 2.7 V           | ≤ 2.5 ns                        |

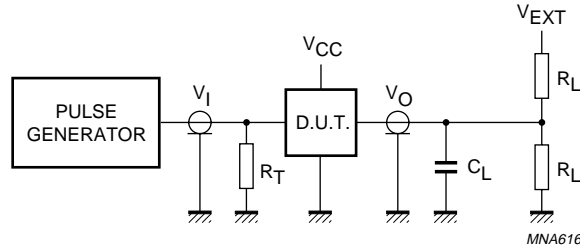
V<sub>X</sub> = V<sub>OL</sub> + 0.3 V at V<sub>CC</sub> ≥ 2.7 V;  
 V<sub>X</sub> = V<sub>OL</sub> + 0.1 V at V<sub>CC</sub> < 2.7 V;  
 V<sub>Y</sub> = V<sub>OH</sub> - 0.3 V at V<sub>CC</sub> ≥ 2.7 V;  
 V<sub>Y</sub> = V<sub>OH</sub> - 0.1 V at V<sub>CC</sub> < 2.7 V.

V<sub>OL</sub> and V<sub>OH</sub> are typical output voltage drop that occur with the output load.

Fig.6 3-state enable and disable times.

16-bit transceiver with direction pin; 30 Ω series termination resistors; 5 V tolerant input/output; 3-state

74LVC162245A;  
74LVCH162245A



| V <sub>CC</sub> | V <sub>I</sub>  | C <sub>L</sub> | R <sub>L</sub>       | V <sub>EXT</sub>                   |                                    |                                    |
|-----------------|-----------------|----------------|----------------------|------------------------------------|------------------------------------|------------------------------------|
|                 |                 |                |                      | t <sub>PLH</sub> /t <sub>PHL</sub> | t <sub>PZH</sub> /t <sub>PHZ</sub> | t <sub>PZL</sub> /t <sub>PLZ</sub> |
| 1.2 V           | V <sub>CC</sub> | 50 pF          | 500 Ω <sup>(1)</sup> | open                               | GND                                | 2 × V <sub>CC</sub>                |
| 2.7 V           | 2.7 V           | 50 pF          | 500 Ω                | open                               | GND                                | 2 × V <sub>CC</sub>                |
| 3.0 to 3.6 V    | 2.7 V           | 50 pF          | 500 Ω                | open                               | GND                                | 2 × V <sub>CC</sub>                |

**Note**

1. The circuit performs better when R<sub>L</sub> = 1000 Ω.

Definitions for test circuits:

R<sub>L</sub> = Load resistor.

C<sub>L</sub> = Load capacitance including jig and probe capacitance.

R<sub>T</sub> = Termination resistance should be equal to the output impedance Z<sub>o</sub> of the pulse generator.

Fig.7 Load circuitry for switching times.

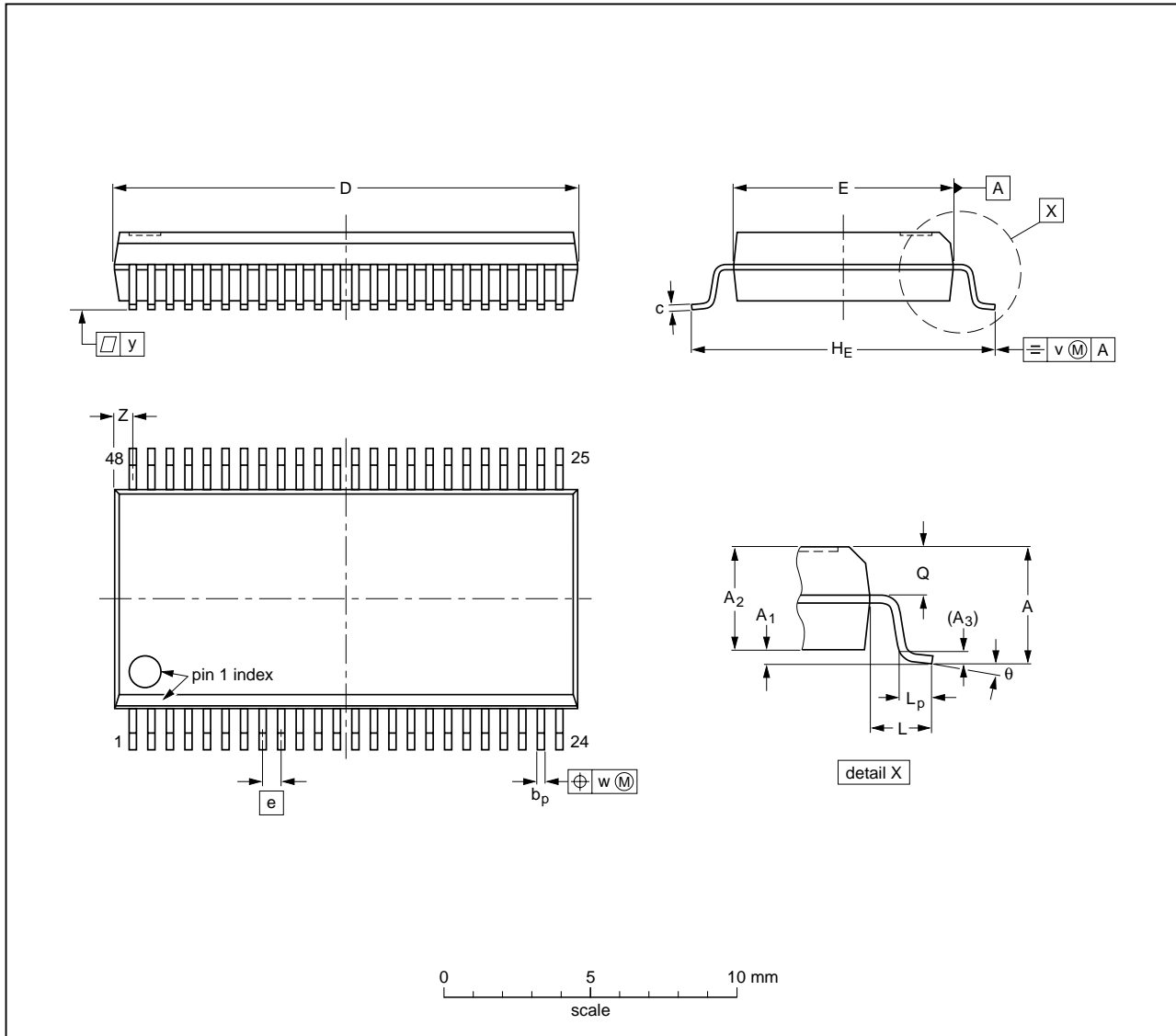
16-bit transceiver with direction pin; 30 Ω series termination resistors; 5 V tolerant input/output; 3-state

74LVC162245A;  
74LVCH162245A

PACKAGE OUTLINES

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm

SOT370-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A max. | A <sub>1</sub> | A <sub>2</sub> | A <sub>3</sub> | b <sub>p</sub> | c            | D <sup>(1)</sup> | E <sup>(1)</sup> | e     | H <sub>E</sub> | L   | L <sub>p</sub> | Q          | v    | w    | y   | z <sup>(1)</sup> | θ        |
|------|--------|----------------|----------------|----------------|----------------|--------------|------------------|------------------|-------|----------------|-----|----------------|------------|------|------|-----|------------------|----------|
| mm   | 2.8    | 0.4<br>0.2     | 2.35<br>2.20   | 0.25           | 0.3<br>0.2     | 0.22<br>0.13 | 16.00<br>15.75   | 7.6<br>7.4       | 0.635 | 10.4<br>10.1   | 1.4 | 1.0<br>0.6     | 1.2<br>1.0 | 0.25 | 0.18 | 0.1 | 0.85<br>0.40     | 8°<br>0° |

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

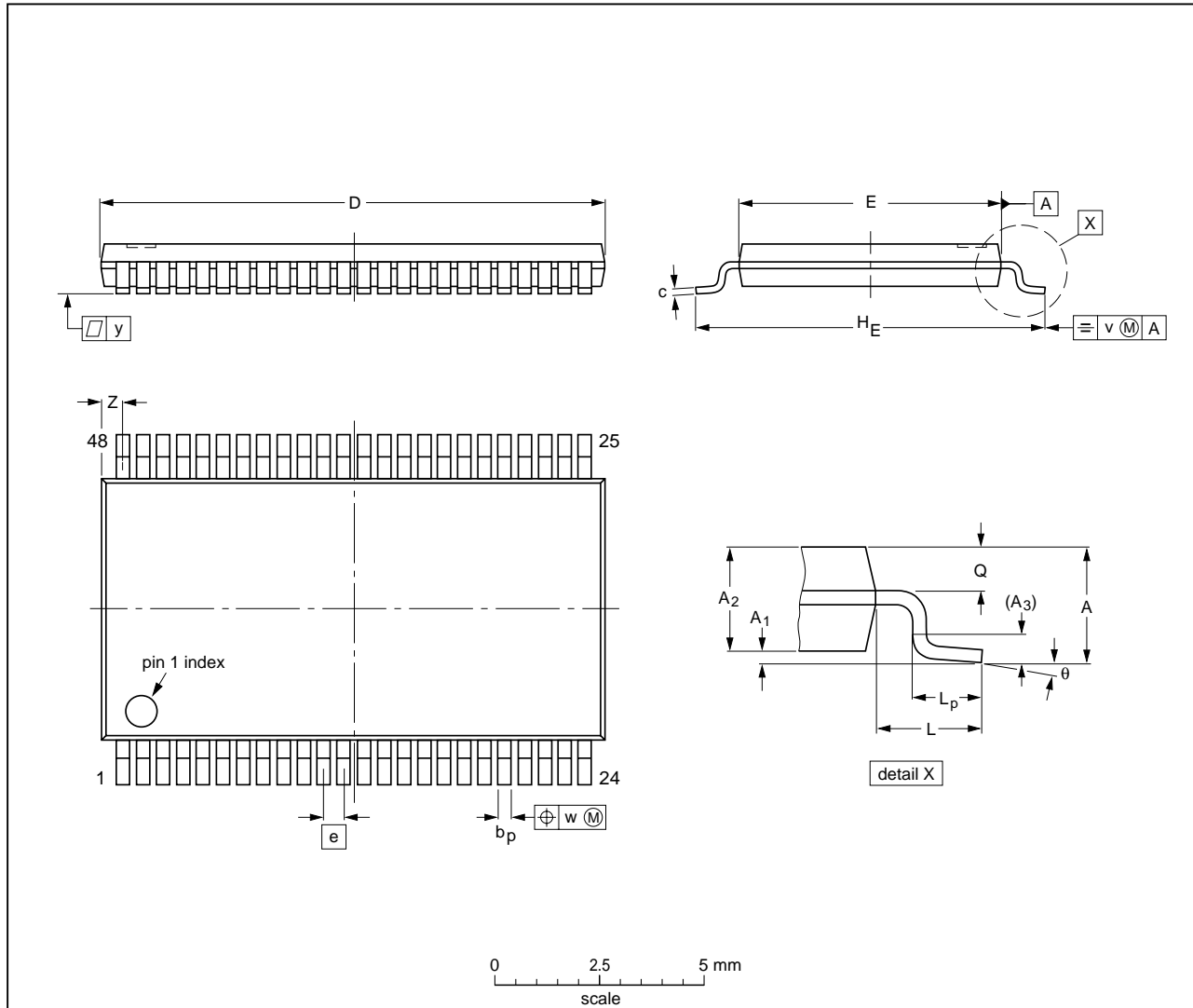
| OUTLINE VERSION | REFERENCES |        |       | EUROPEAN PROJECTION | ISSUE DATE           |
|-----------------|------------|--------|-------|---------------------|----------------------|
|                 | IEC        | JEDEC  | JEITA |                     |                      |
| SOT370-1        |            | MO-118 |       |                     | 99-12-27<br>03-02-19 |

16-bit transceiver with direction pin; 30 Ω series termination resistors; 5 V tolerant input/output; 3-state

74LVC162245A;  
74LVCH162245A

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1



**DIMENSIONS** (mm are the original dimensions).

| UNIT | A max. | A <sub>1</sub> | A <sub>2</sub> | A <sub>3</sub> | b <sub>p</sub> | c          | D <sup>(1)</sup> | E <sup>(2)</sup> | e   | H <sub>E</sub> | L | L <sub>p</sub> | Q            | v    | w    | y   | Z          | θ        |
|------|--------|----------------|----------------|----------------|----------------|------------|------------------|------------------|-----|----------------|---|----------------|--------------|------|------|-----|------------|----------|
| mm   | 1.2    | 0.15<br>0.05   | 1.05<br>0.85   | 0.25           | 0.28<br>0.17   | 0.2<br>0.1 | 12.6<br>12.4     | 6.2<br>6.0       | 0.5 | 8.3<br>7.9     | 1 | 0.8<br>0.4     | 0.50<br>0.35 | 0.25 | 0.08 | 0.1 | 0.8<br>0.4 | 8°<br>0° |

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES |        |       | EUROPEAN PROJECTION | ISSUE DATE           |
|-----------------|------------|--------|-------|---------------------|----------------------|
|                 | IEC        | JEDEC  | JEITA |                     |                      |
| SOT362-1        |            | MO-153 |       |                     | 99-12-27<br>03-02-19 |

16-bit transceiver with direction pin; 30  $\Omega$  series  
termination resistors; 5 V tolerant input/output; 3-state

74LVC162245A;  
74LVCH162245A

#### DATA SHEET STATUS

| LEVEL | DATA SHEET STATUS <sup>(1)</sup> | PRODUCT STATUS <sup>(2)(3)</sup> | DEFINITION   |
|-------|----------------------------------|----------------------------------|--|
| I     | Objective data                   | Development                      | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.  |
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