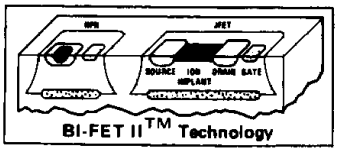
National Semiconductor



LF13741
Monolithic JFET Input Operational Amplifier

General Description

The LF13741 is a 741 with BI-FET™ input followers on the same die. Familiar operating characteristics—those of a 741—with the added advantage of low input bias current make the LF13741 easy to use. Monolithic fabrication makes this "drop-in-replacement" operational amplifier very economical.

Applications in which the LF13741 excels are those which require low bias current, moderate speed and low cost. A few examples include high impedance transducer amplifiers, photocell amplifiers, buffers for high impedance, slow to moderate speed sources and buffers in sample-and-hold type systems where leakage from the hold capacitor node must be kept to a minimum.

Systems designers can take full advantage of their knowledge of the 741 when designing with the LF13741 to achieve extremely rapid "design times." The LF13741 can also be used in existing sockets to make the "error budget" for input bias and/or offset currents negligible and in many cases eliminate trimming. For higher speed and lower noise use the LF155, LF156, LF157 series of BI-FET operational amplifiers.

Features

- Low input bias current 50 pA
- Input common-mode range to positive supply voltage
- Low input noise current 0.01 pA/$\sqrt{Hz}$
- High input impedance $5 \times 10^{11}\Omega$
- Familiar operating characteristics

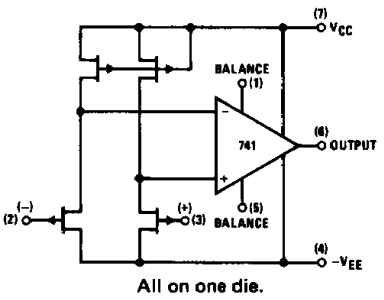
Advantages

- FET inputs—741 operating characteristics
- Low cost
- Ease of use
- Standard supplies
- Standard pin outs
- Non-rectifying input for RF environment
- Rapid "design time"

Applications

- Smoke detectors
- I to V converters
- High impedance buffers
- Low drift sample and hold circuits
- High input impedance, slow comparators
- Long time timers
- Low drift peak detectors
- Supply current monitors
- Low error budget systems

Simplified Schematic

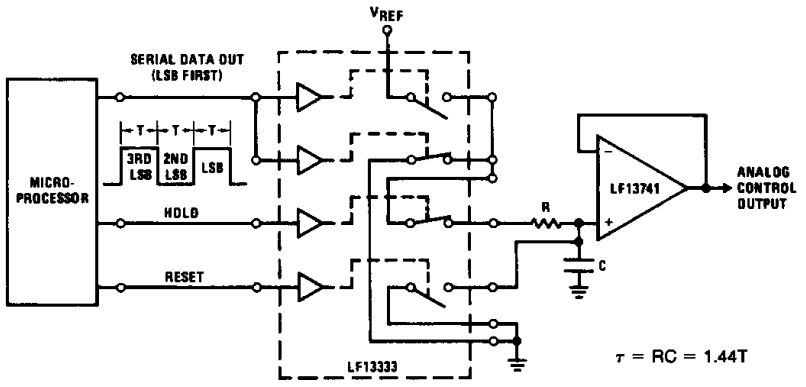


All on one die.

TL/H/9296–1

Typical Applications

Inexpensive Microprocessor D/A



TL/H/9296–2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±18V
Operating Temperature Range	0°C to +70°C
$T_{j(MAX)}$	100°C
Differential Input Voltage	±30V
Input Voltage Range (Note 3)	±16V
Output Short Circuit Duration	Continuous
Storage Temperature Range	−65°C to +150°C

	H Package	N Package
θ_{jA} (Typical)		
(Note 1)	70°C/W	163°C/W
(Note 2)	175°C/W	218°C/W
θ_{jC} (Typical)	25°C/W	

Metal Package Lead Temperature (Soldering, 10 sec.) 300°C

Plastic Package (Soldering, 4 sec.) 260°C

ESD rating to be determined.

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OS}	Input Offset Voltage	R_S = 10 kΩ, T_A = 25°C		5	15	mV
		Over Temperature			20	
	Voltage Offset Adjustment Range		10			mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S = 10 kΩ		10		μV/°C
I_{OS}	Input Offset Current	T_j = 25°C (Notes 4, 5)		10	50	pA
		$T_j \leq$ 70°C			2	nA
I_B	Input Bias Current	T_j = 25°C (Notes 4, 5)		50	200	pA
		$T_j \leq$ 70°C		1.6	8	nA
R_{IN}	Input Resistance	T_j = 25°C		5×10^{11}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S = ±15V, T_A = 25°C V_O = ±10V, R_L = 2 kΩ	25	100		V/mV
		Over Temperature	15			V/mV
V_O	Output Voltage Swing	V_S = ±15V, R_L = 10 kΩ	±12	±13		V
V_{CM}	Input Common-Mode Voltage Range	V_S = ±15V	±11	+15.1 −12		V
CMRR	Common-Mode Rejection Ratio	$R_S \leq$ 10 kΩ	70	90		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	77	96		dB
I_S	Supply Current			2	4	mA

3

AC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SR	Slew Rate	$V_S = \pm 15V$, $T_A = 25°C$		0.5		V/μs
GBW	Gain-Bandwidth Product	$V_S = \pm 15V$, $T_A = 25°C$		1.0		MHz
e_n	Equivalent Input Noise Voltage	$T_A = 25°C$, $R_S = 100\Omega$ f = 100 Hz f = 1000 Hz		 50 37		 $nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	$T_j = 25°C$ f = 100 Hz f = 1000 Hz		 0.01 0.01		 $pA/\sqrt{Hz}$ $pA/\sqrt{Hz}$

Note 1: The value given is in 400 Linear Feet/Min air flow.

Note 2: The value given is in static air.

Note 3: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

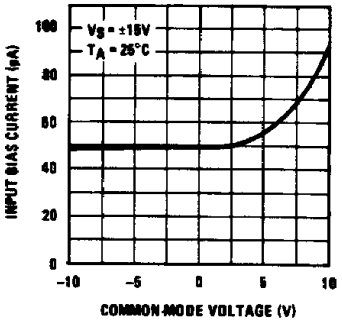
Note 4: These specifications apply for $V_S = \pm 15V$ and $0°C \leq T_A \leq +70°C$. V_{OS}, I_B, and I_{OS} are measured at $V_{CM} = 0$.

Note 5: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

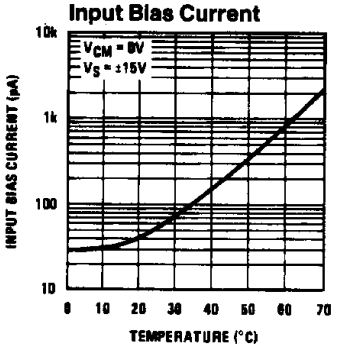
Note 6: Supply Voltage Rejection Ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice from $V_S = \pm 10V$ to $\pm 15V$.

Typical Performance Characteristics

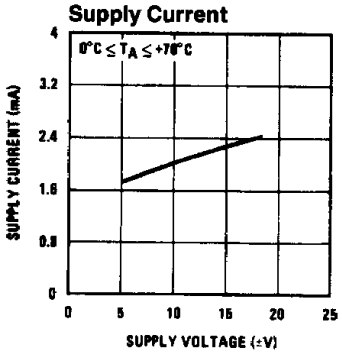
Input Bias Current



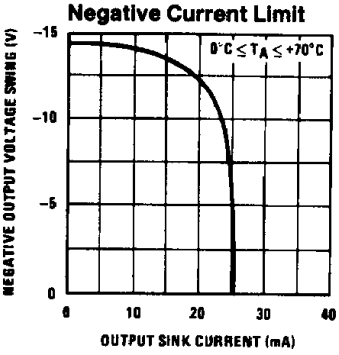
Input Bias Current



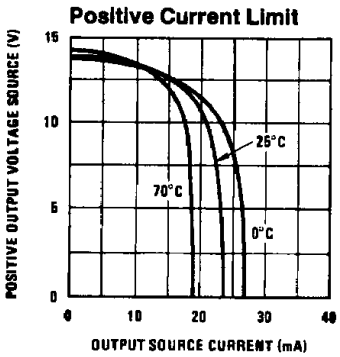
Supply Current



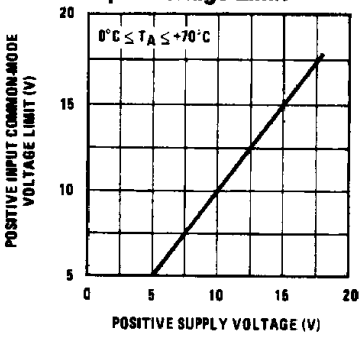
Negative Current Limit



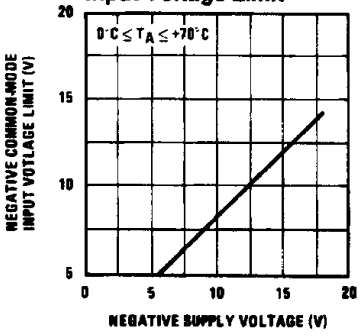
Positive Current Limit



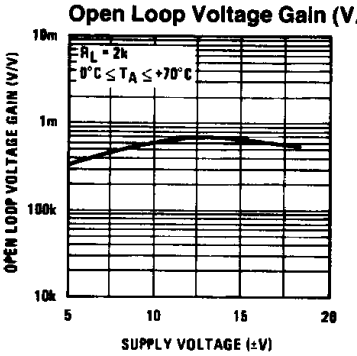
Positive Common-Mode Input Voltage Limit



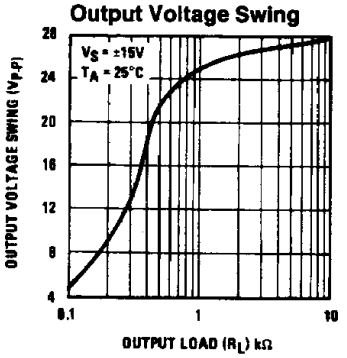
Negative Common-Mode Input Voltage Limit



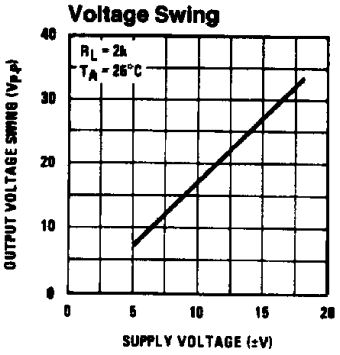
Open Loop Voltage Gain (V/V)



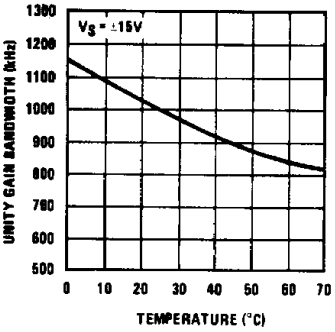
Output Voltage Swing



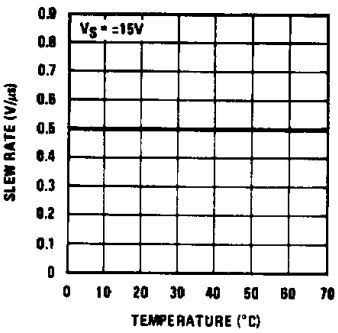
Voltage Swing



Gain Bandwidth



Slew Rate



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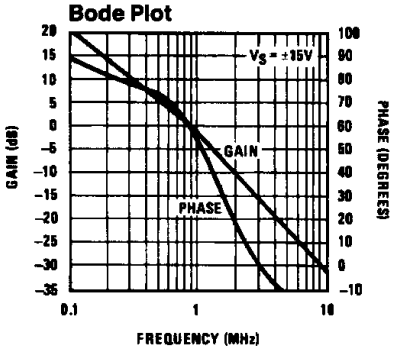
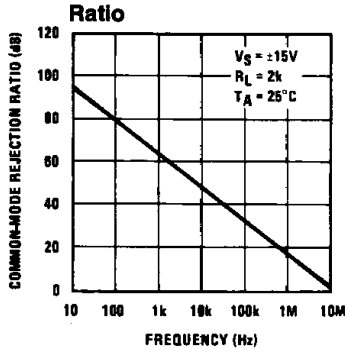
Typical Performance Characteristics (Continued)

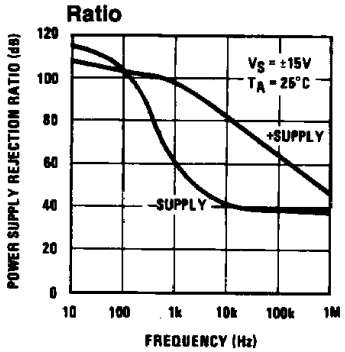
Bode Plot



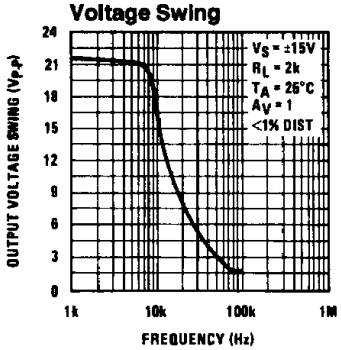
Common-Mode Rejection Ratio



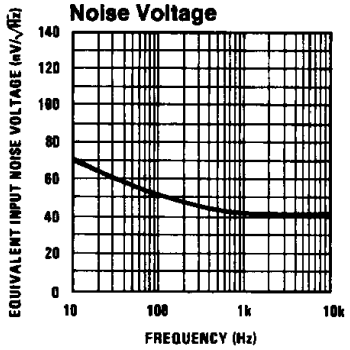
Power Supply Rejection Ratio



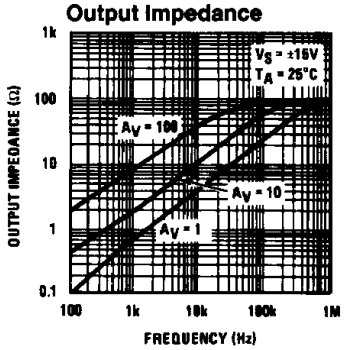
Undistorted Output Voltage Swing



Equivalent Input Noise Voltage



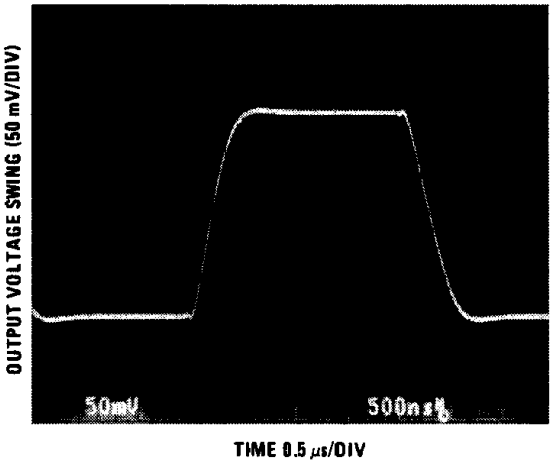
Output Impedance



TL/H/9296–4

LF13741 Pulse Responses

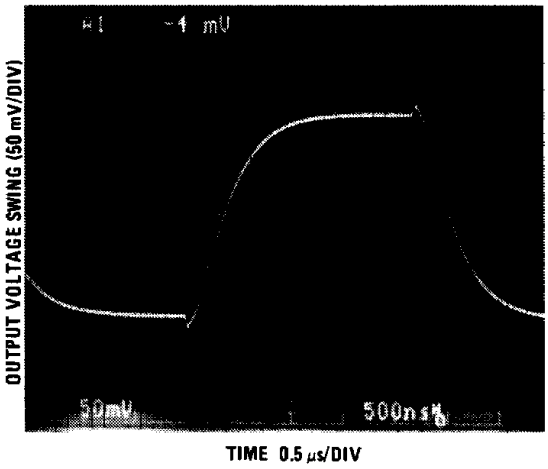
Small Signal Non-Inverting Pulse Response



TL/H/9296–5

$A_V = +1$ (Follower)

Small Signal Inverting Pulse Response



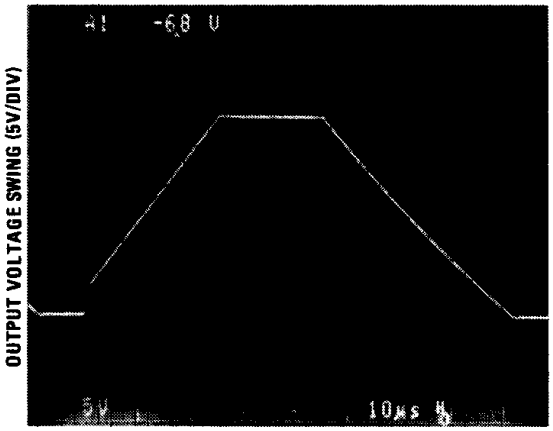
TL/H/9296–6

$A_V = -1$ (Inverter)

Typical Performance Characteristics (Continued)

LF13741 Pulse Responses (Continued)

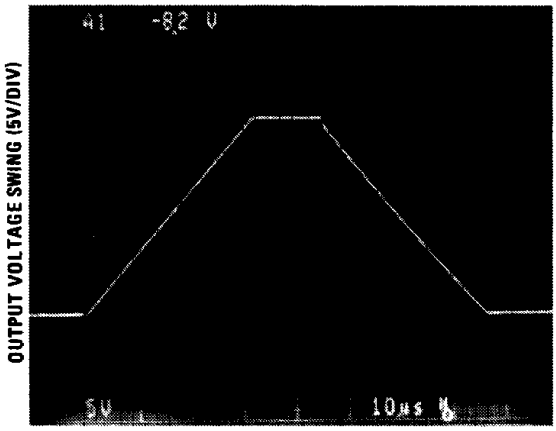
Large Signal Non-Inverting Pulse Response



TIME 10 μs/DIV

TL/H/9296–7

Large Signal Inverting Pulse Response



TIME 10 μs/DIV

TL/H/9296–8

Application Hints

GENERAL CHARACTERISTICS

The LF13741 makes the job of converting from a bipolar to an FET input op amp easy. As a systems designer you are probably very familiar with the operating characteristics of a 741 op amp. In fact, many of you have used 741s with FET input followers—that's just what the LF13741 is, but it's all on a single die.

When you need a low cost, reliable, well known op amp with low input currents and moderate speed, use an LF13741.

DIFFERENTIAL INPUTS

You don't have to use clamps across the inputs for differential input voltages of less than 40V. The input JFETs of the LF13741, in addition to being well matched, have large reverse breakdown voltages from gate to source and drain.

POSITIVE INPUT COMMON-MODE VOLTAGE LIMIT

With the LF13741 (unlike the normal 741) you can take both inputs above the positive supply voltage by more than 0.1V before the amplifier ceases to function. This feature enables you to use the LF13741 to monitor and/or limit the current from the same supply used to power it (see typical applications).

If you exceed the positive common-mode voltage limit on only one input, the output phase will remain correct. When you exceed the limit on both inputs, the output phase is unpredictable.

NEGATIVE INPUT COMMON-MODE VOLTAGE LIMIT

There are two negative input voltage ranges of interest:

1. The range between the negative common-mode voltage limit and the negative supply voltage.
2. Voltages which are more negative than the negative supply voltage.

If you take only one of the inputs of the LF13741 into the first range, the output phase will remain correct. When you take both inputs into this range the output will go toward the positive supply voltage.

If you force either or both of the inputs into the second range, an internal diode will be turned "ON." Unless you externally limit the diode current to about 1 mA, the device will be destroyed. In either case, limited or unlimited input current, you cannot predict the output.

HANDLING

You do not have to take any special precautions in handling the LF13741. It has JFET, as opposed to fragile MOSFET, inputs.

APPLYING POWER

You should never: reverse the power supplies to the LF13741; plug a part in backwards in a powered socket or board; make the negative supply voltage more positive than an input voltage.

Any one of these supply conditions will forward bias an internal diode. If you have not externally limited the resulting current, the device will be destroyed.

LAYOUT

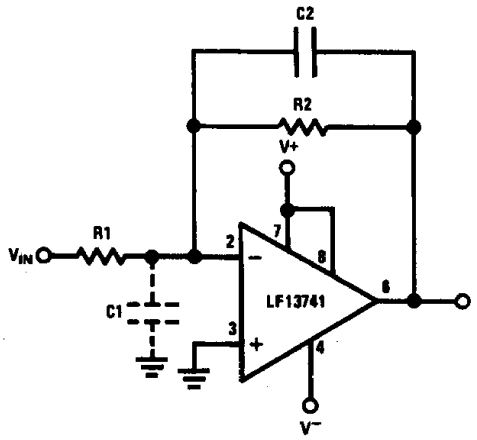
To ensure stability of response you should take care with lead dress, component placement and power supply decoupling. For example, the body of feedback resistors (from output to input pins) should be placed close to the inverting input pin. Noise "pickup" and capacitance to ground from the input pin will be minimized—effects which are usually desirable.

Because of the very low input bias currents of the LF13741, special care should be taken in printed circuit board layouts to prevent unnecessary leakage from the input nodes, (see Typical Applications).

Application Hints (Continued)

FEEDBACK POLE

You create a feedback pole when you place resistive feedback around an amplifier. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency (a distinct possibility when using FET op amps), you should place a lead capacitor from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant *(Figure 1)*.



TL/H/9296–9

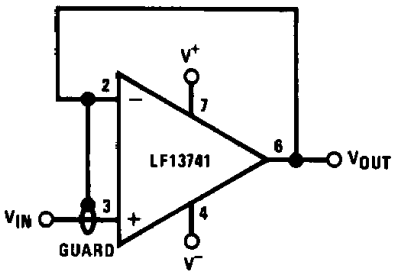
Parasitic input capacitance C1 ≅ (3 pF for LF13741 plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate, add C2 such that: R2C2 ≅ R1C1.

FIGURE 1

Typical Applications (Continued)

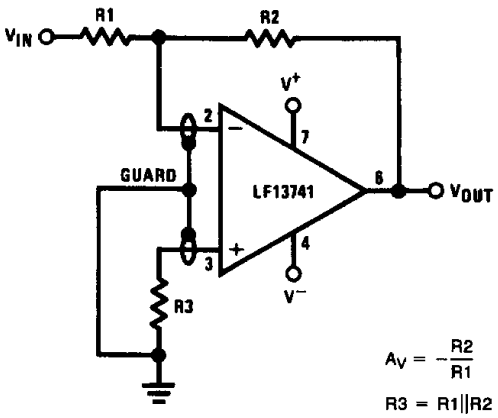
Circuits Using Guard Rings to Prevent Leakage Currents Between Inputs and V⁻

Guarded Voltage Follower



TL/H/9296–10

Guarded Inverting Amplifier

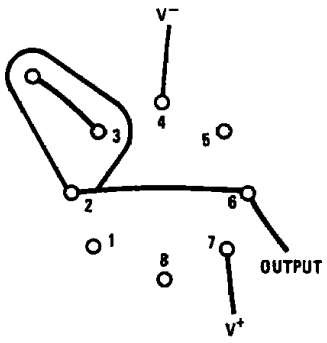


$$A_V = -\frac{R2}{R1}$$

$$R3 = R1 \| R2$$

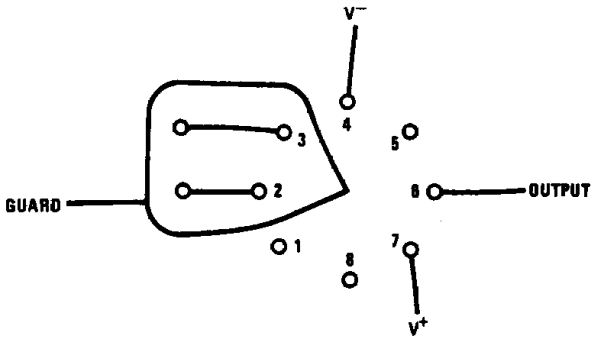
TL/H/9296–11

PC Layout



TL/H/9296–12

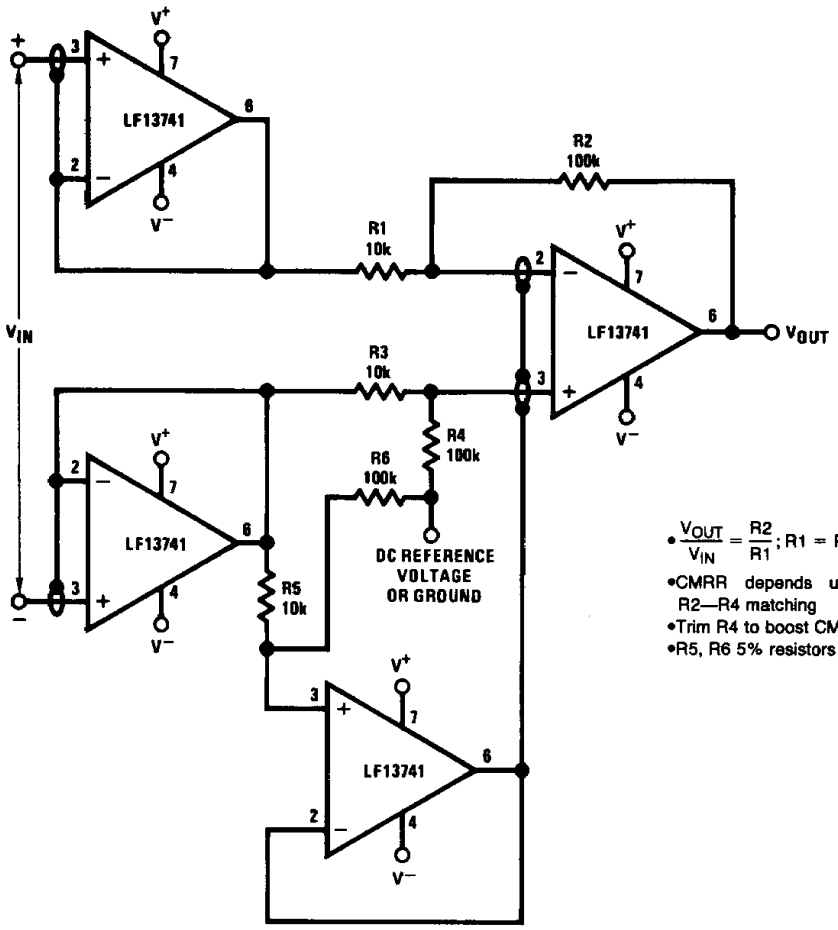
PC Layout



TL/H/9296–13

Typical Applications (Continued)

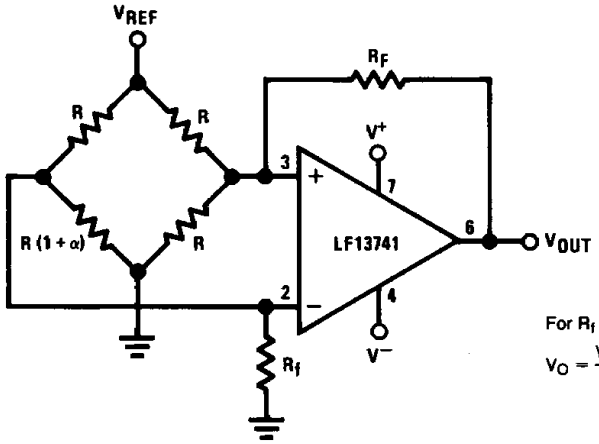
Guarded Instrumentation Amplifier



- $\frac{V_{OUT}}{V_{IN}} = \frac{R2}{R1}$; R1 = R3, R2 = R4
- CMRR depends upon R1—R3, R2—R4 matching
- Trim R4 to boost CMRR
- R5, R6 5% resistors

TL/H/9296–14

Bridge Amplifier



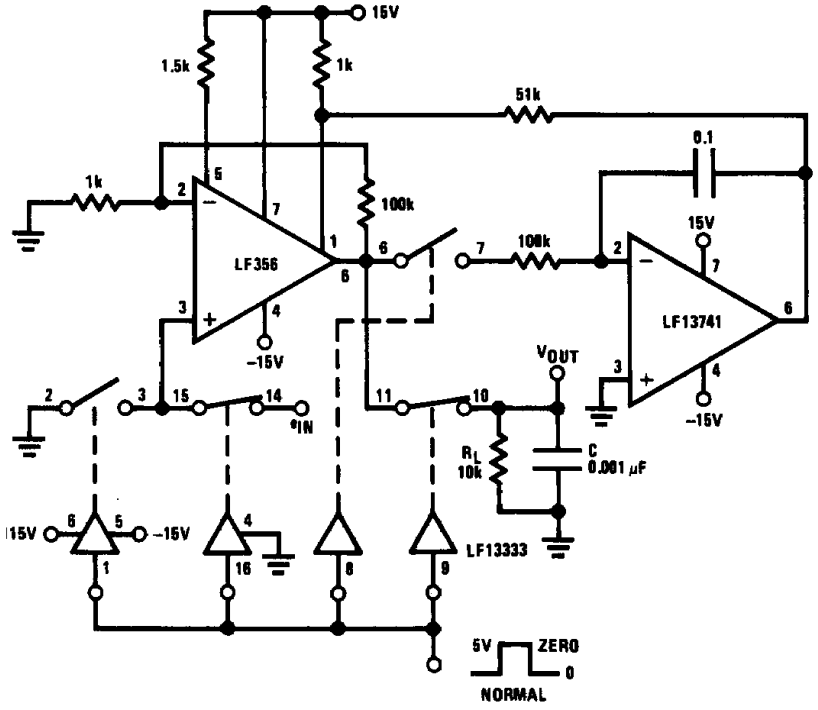
For $R_f > R$

$$V_O = \frac{V_{REF}}{2}\left(\frac{R_F}{R}\right)\left(\frac{\alpha}{1+\alpha}\right)$$

TL/H/9296–15

Typical Applications (Continued)

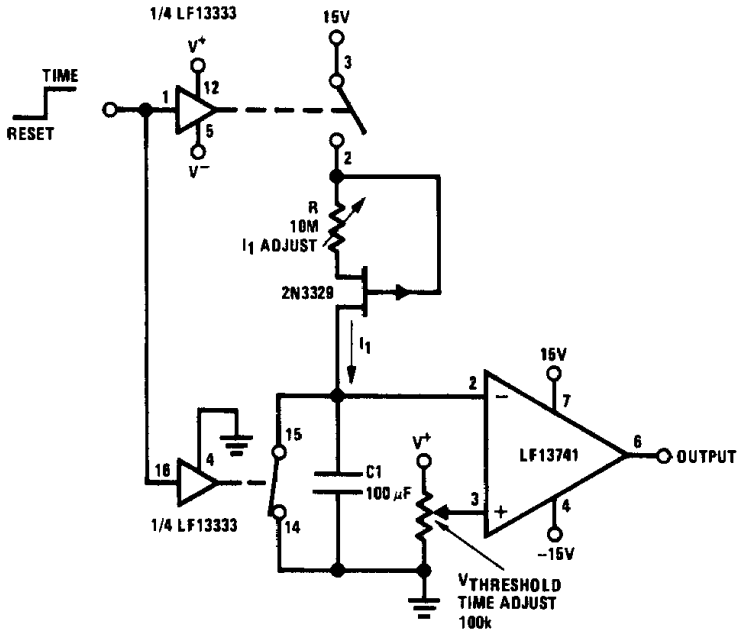
Auto Zero Circuit for LF356



TL/H/9296–16

- With the output having a 10k load resistor minimum pulse width to zero ≈ 800 μs
- The capacitor on the output reduces the output switch glitch

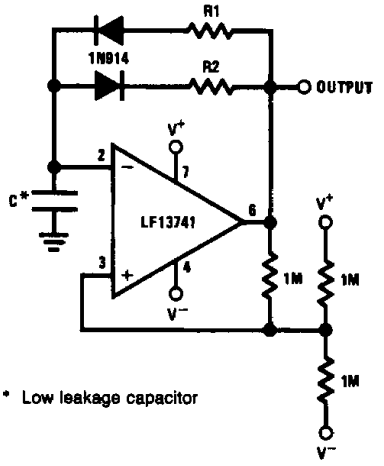
Long Time Timer



TL/H/9296–17

- Time = $\frac{C1}{I_1} V_{THRESHOLD}$
- Output goes high on time out
- Reverse op amp inputs for output low on time out
- C1 low leakage capacitor

Ultra-Low (or High) Duty Cycle Pulse Generator



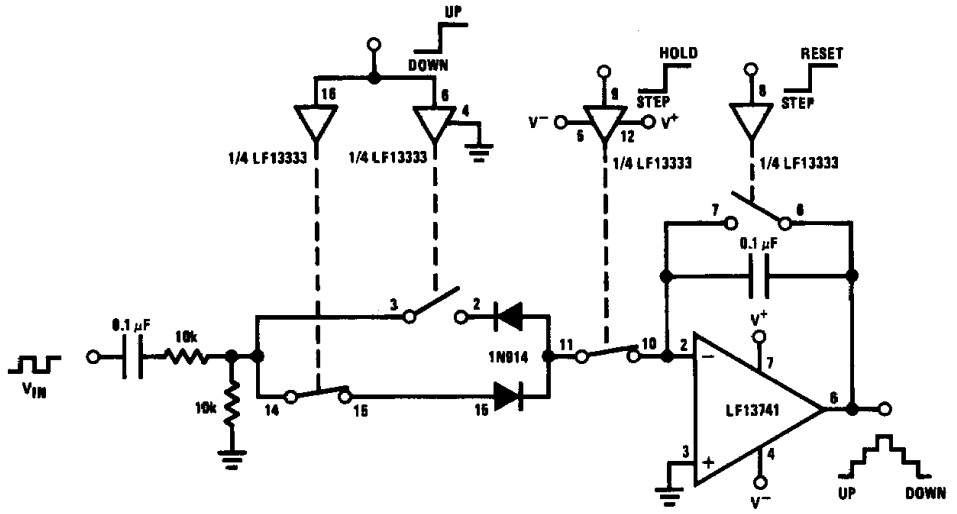
TL/H/9296–18

- Low leakage capacitor
- $t_{OUTPUT\ HIGH} \approx R1C\ \ell n \frac{4.8 - 2V_S}{4.8 - V_S}$
- $t_{OUTPUT\ LOW} \approx R2C\ \ell n \frac{2V_S - 7.8}{V_S - 7.8}$

where $V_S = V^+ + |V^-|$

Typical Applications (Continued)

Up/Down Staircase Generator/Step and Hold



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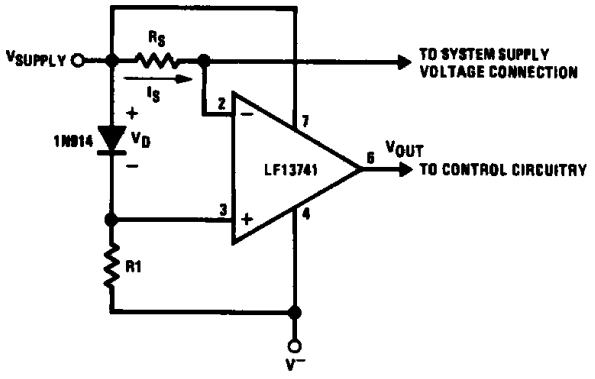
Supply Current Indicator/Limiter



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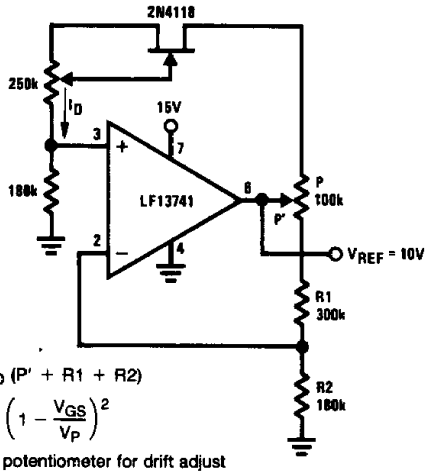
• V_{OUT} switches high when $R_S I_S > V_D$

Low Drift Adjustable Voltage Reference



• $V_{REF} = I_D (P' + R1 + R2)$

$$I_D \cong I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

• Trim 250k potentiometer for drift adjust

• Trim 100k potentiometer for V_{REF} adjust

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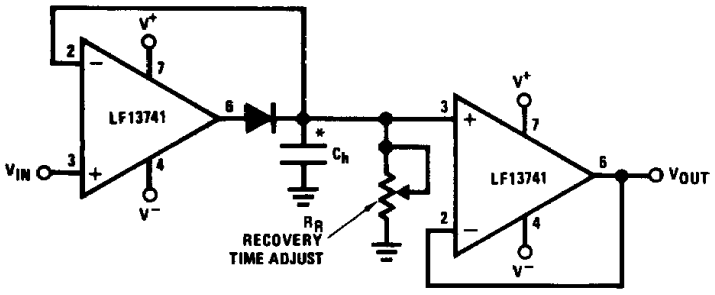
Low Drift Peak Detector



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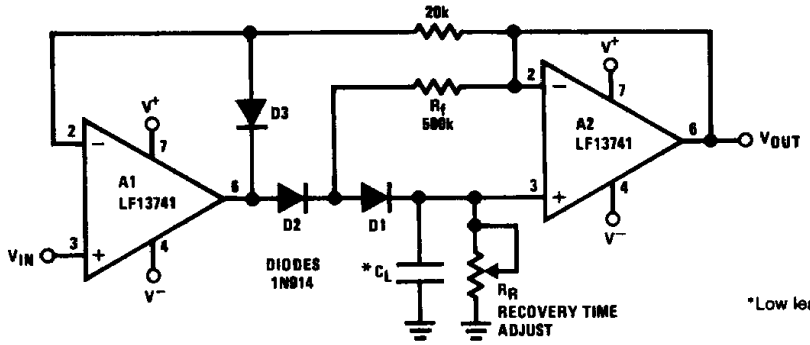
*Low leakage capacitor

Typical Applications (Continued)

Ultra-Low Drift Peak Detector



*Low leakage capacitor

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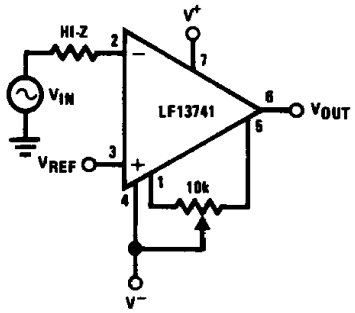
- By adding D1 and R_f, V_{D1} = 0 during hold mode. Leakage of D2 provided by feedback path through R_f.
- Leakage of circuit is I_B plus leakage of C_h.
- D3 clamps V_{OUT} A1 to $V_{IN} - V_{D3}$ to improve speed and to limit the reverse bias of D2.
- Maximum input frequency should be $< \frac{1}{2\pi} R_f C_{D2}$, where C_{D2} is the shunt capacitance of D2.

Comparator with Offset Adjust for Hi-Z Inputs



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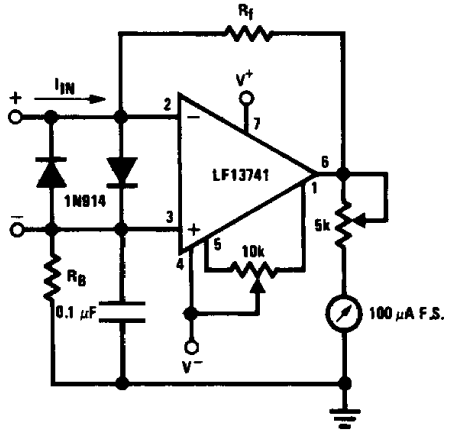
$V^- + 3V \leq V_{IN} \leq V^+ + 0.1V$

Low Current Ammeter



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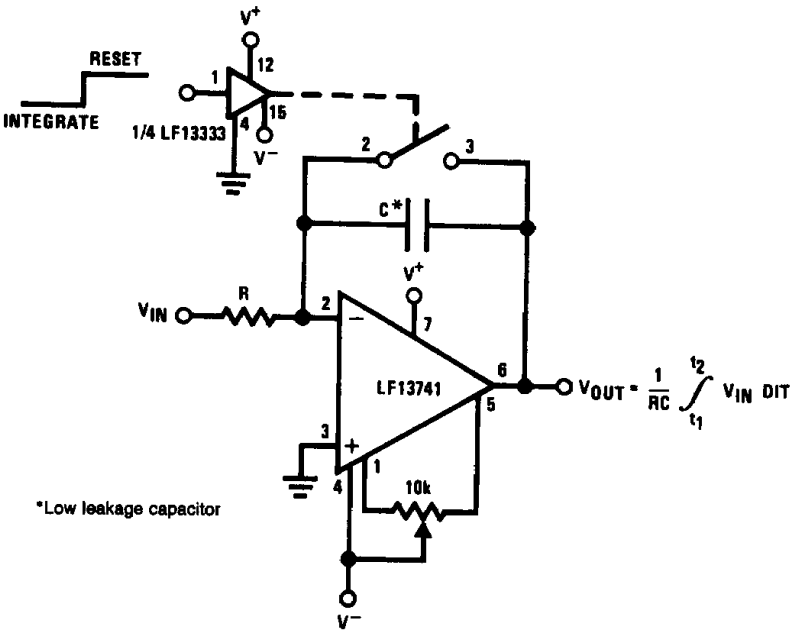
$I_{FULL\ SCALE}$	R_F	R_B
100 nA	1.5M	1.5M
500 nA	300k	300k
1 μA	300k	0
5 μA	60k	0
10 μA	30k	0
50 μA	6k	0
100 μA	3k	0

Typical Applications (Continued)

Long Time Integrator



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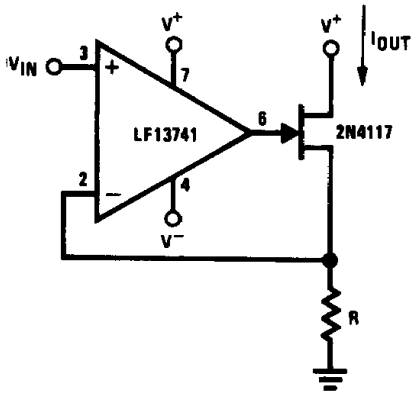
Precision Current Sink



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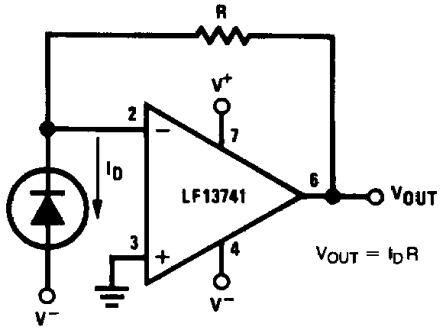
$I_{OUT} = \frac{V_{IN}}{R}$, where $I_{OUT} \leq I_{DSS}$

Photo Cell Amplifier (I to V Converter)



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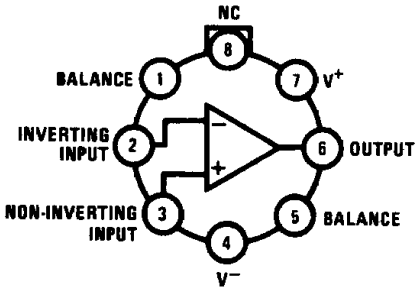
Connection Diagrams (Top Views)

TO-99 Metal Can Package



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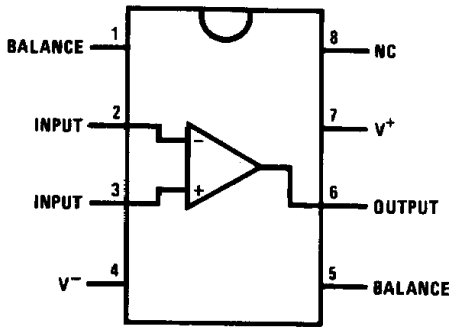
Note: Pin 4 connected to case.

Order Number LF13741H
See NS Package Number H08C

Dual-In-Line Package



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Order Number LF13741N
See NS Package Number N08E