

# DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

## **HEF4508B** **MSI** Dual 4-bit latch

Product specification  
File under Integrated Circuits, IC04

January 1995

# Dual 4-bit latch

# HEF4508B MSI

### DESCRIPTION

The HEF4508B is a dual 4-bit latch, which consists of two identical independent 4-bit latches with separate strobe (ST), master reset (MR), output-enable input (EO) and 3-state outputs (O).

With the ST input in the HIGH state, the data on the D inputs appear at the corresponding outputs provided  $\overline{EO}$  is LOW. Changing the ST input to the LOW state locks the

data into the latch. A HIGH on the reset line forces the outputs to a LOW level regardless of the state of the ST input. The 3-state outputs are controlled by the output-enable input. A HIGH on  $\overline{EO}$  causes the outputs to assume a high impedance OFF-state regardless of other input conditions. This allows the outputs to interface directly with bus orientated systems. When  $\overline{EO}$  is LOW the contents of the latches are available at the outputs.

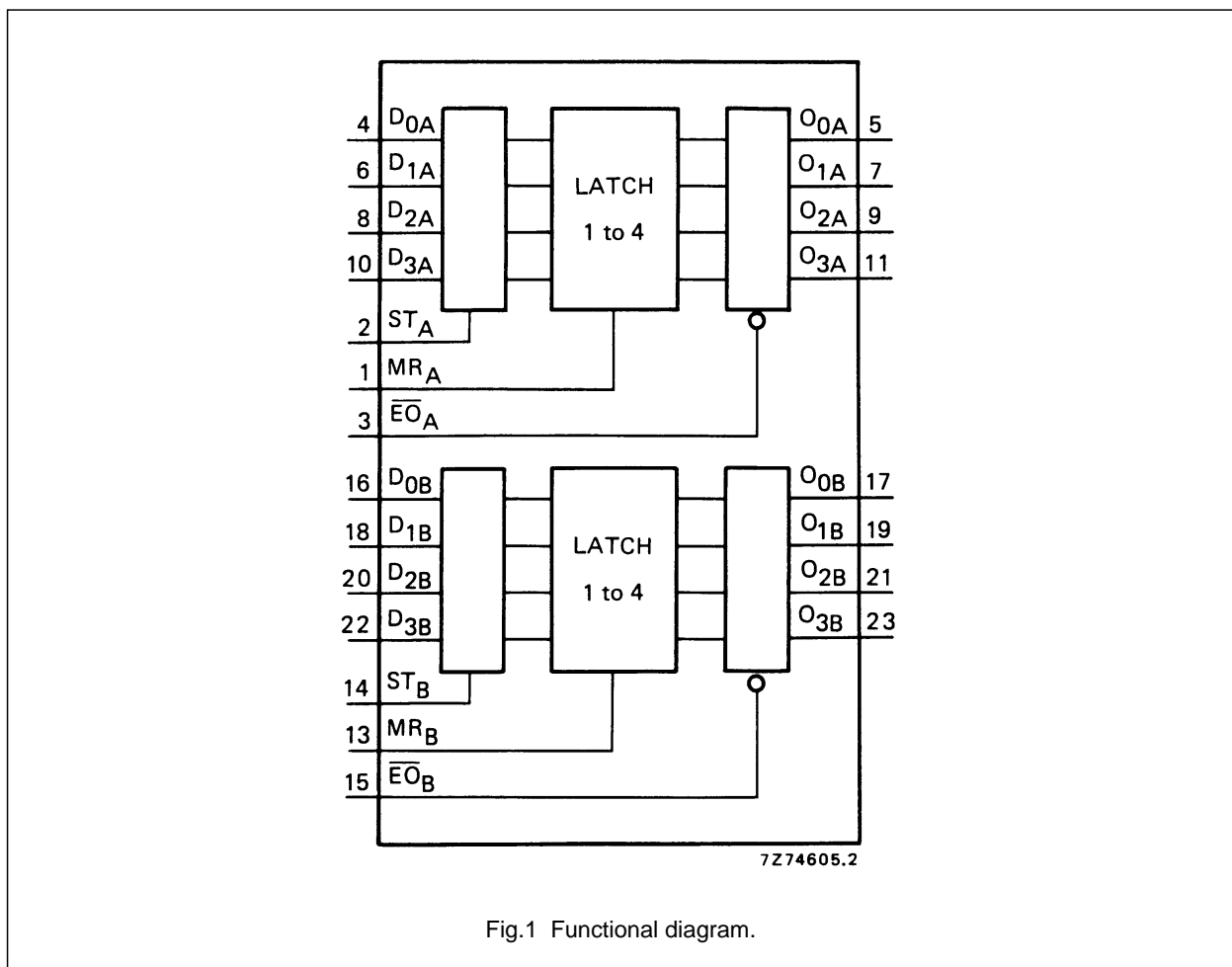
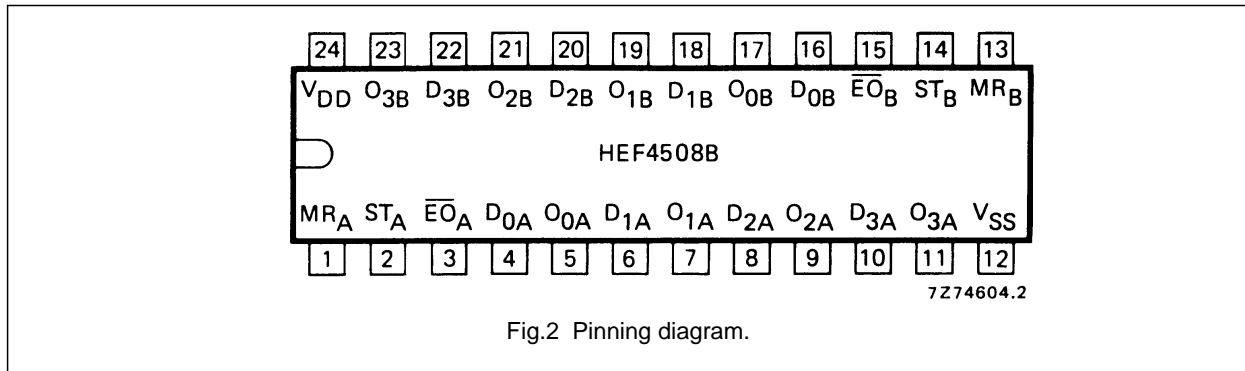


Fig.1 Functional diagram.

### FAMILY DATA, I<sub>DD</sub> LIMITS category MSI

See Family Specifications

## Dual 4-bit latch

HEF4508B  
MSI

- HEF4508BP(N): 24-lead DIL; plastic  
(SOT101-1)
- HEF4508BD(F): 24-lead DIL; ceramic (cerdip)  
(SOT94)
- HEF4508BT(D): 24-lead SO; plastic  
(SOT137-1)
- ( ): Package Designator North America

**PINNING**

- $D_{0A}$  to  $D_{3A}$ ,  $D_{0B}$  to  $D_{3B}$  data inputs
- $ST_A$ ,  $ST_B$  strobe inputs
- $MR_A$ ,  $MR_B$  master reset inputs
- $\overline{EO}_A$ ,  $\overline{EO}_B$  output enable inputs
- $O_{0A}$  to  $O_{3A}$ ,  $O_{0B}$  to  $O_{3B}$  3-state outputs

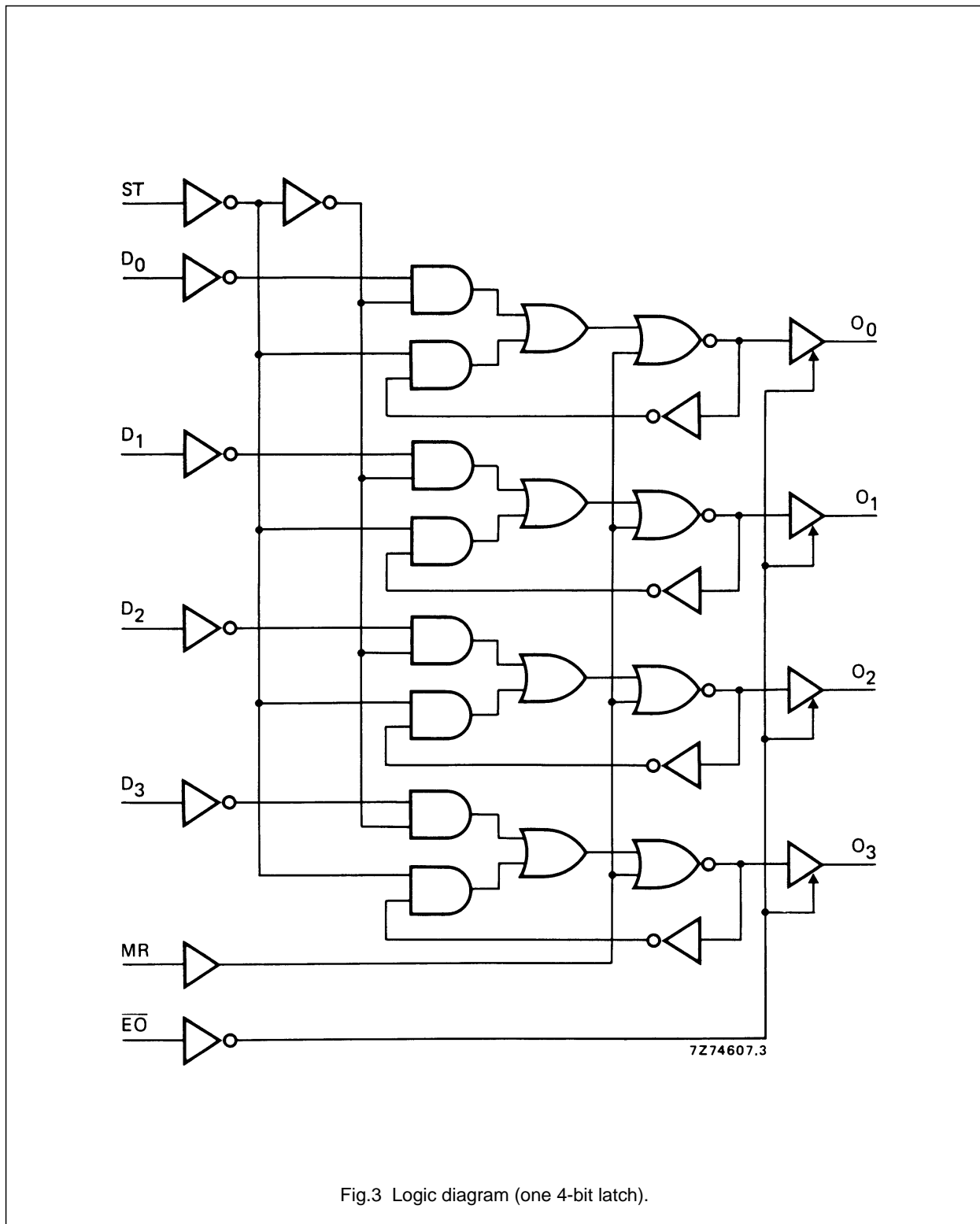
**FUNCTION TABLE**

INPUTS				OUTPUT
MR	ST	$\overline{EO}$	$D_n$	$O_n$
L	H	L	H	H
L	H	L	L	L
L	L	L	X	latched
H	X	L	X	L
X	X	H	X	Z

**Notes**

- H = HIGH state (the more positive voltage)  
L = LOW state (the less positive voltage)  
X = state is immaterial  
Z = high impedance OFF state

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HEF4508B  
MSI



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HEF4508B  
MSI**AC CHARACTERISTICS** $V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ °C}$ ;  $C_L = 50\text{ pF}$ ; input transition times  $\leq 20\text{ ns}$ 

	$V_{DD}$ V	SYMBOL	MIN.	TYP.	MAX.	
Minimum ST pulse width; HIGH	5	$t_{WSTH}$	50	25	ns	see also waveforms Fig.4
	10		30	15	ns	
	15		20	10	ns	
Minimum MR pulse width; HIGH	5	$t_{WMRH}$	40	20	ns	
	10		24	12	ns	
	15		20	10	ns	
Recovery time for MR	5	$t_{RMR}$	20	0	ns	
	10		20	0	ns	
	15		15	0	ns	
Set-up times $D_n \rightarrow ST$	5	$t_{su}$	35	10	ns	
	10		25	5	ns	
	15		20	0	ns	
Hold times $D_n \rightarrow ST$	5	$t_{hold}$	20	0	ns	
	10		20	0	ns	
	15		15	0	ns	

	$V_{DD}$ V	TYPICAL FORMULA FOR P ( $\mu\text{W}$ )	
Dynamic power dissipation per package (P)	5	$2\,000 f_i + \sum (f_o C_L) \times V_{DD}^2$	where $f_i$ = input freq. (MHz) $f_o$ = output freq. (MHz) $C_L$ = load capacitance (pF) $\sum (f_o C_L)$ = sum of outputs $V_{DD}$ = supply voltage (V)
	10	$9\,000 f_i + \sum (f_o C_L) \times V_{DD}^2$	
	15	$25\,000 f_i + \sum (f_o C_L) \times V_{DD}^2$	

Dual 4-bit latch

HEF4508B  
MSI

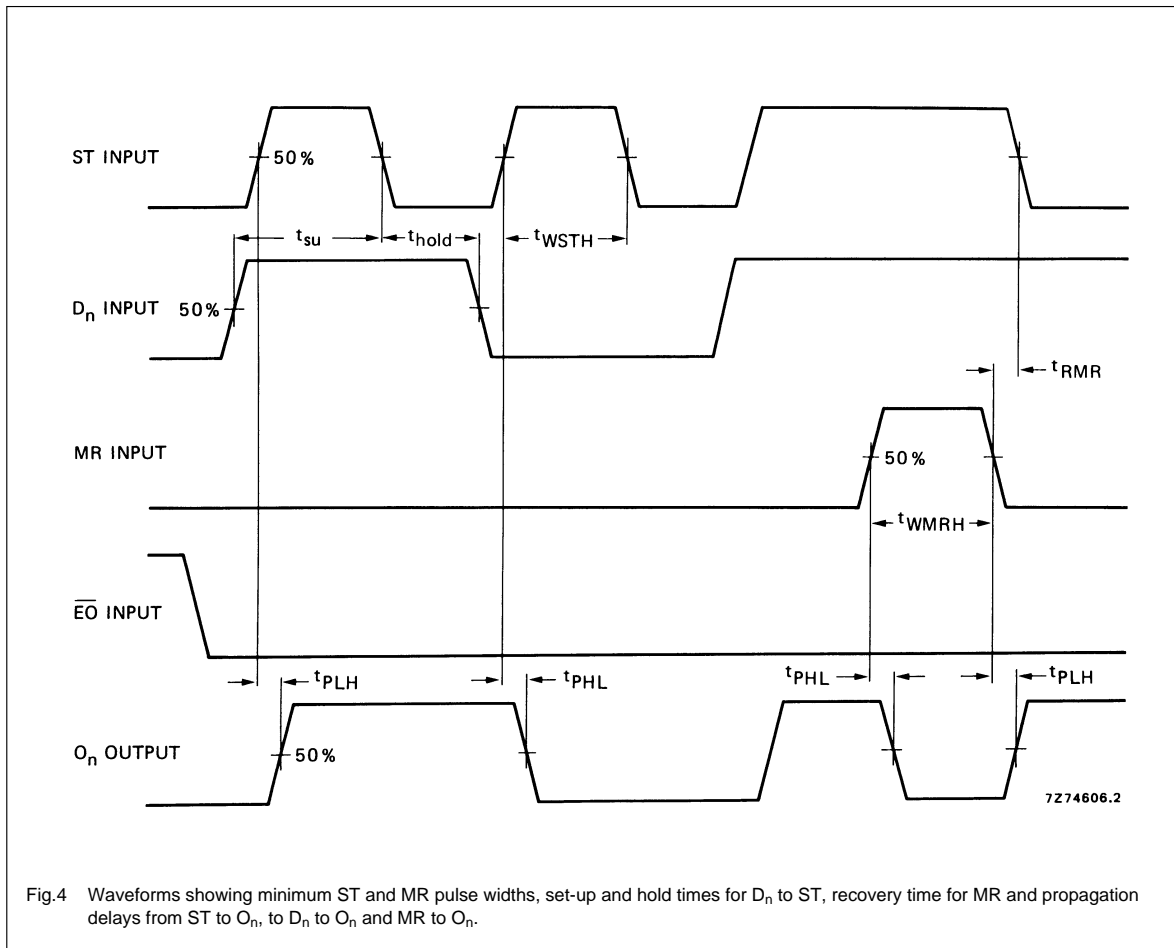


Fig.4 Waveforms showing minimum ST and MR pulse widths, set-up and hold times for D<sub>n</sub> to ST, recovery time for MR and propagation delays from ST to O<sub>n</sub>, to D<sub>n</sub> to O<sub>n</sub> and MR to O<sub>n</sub>.

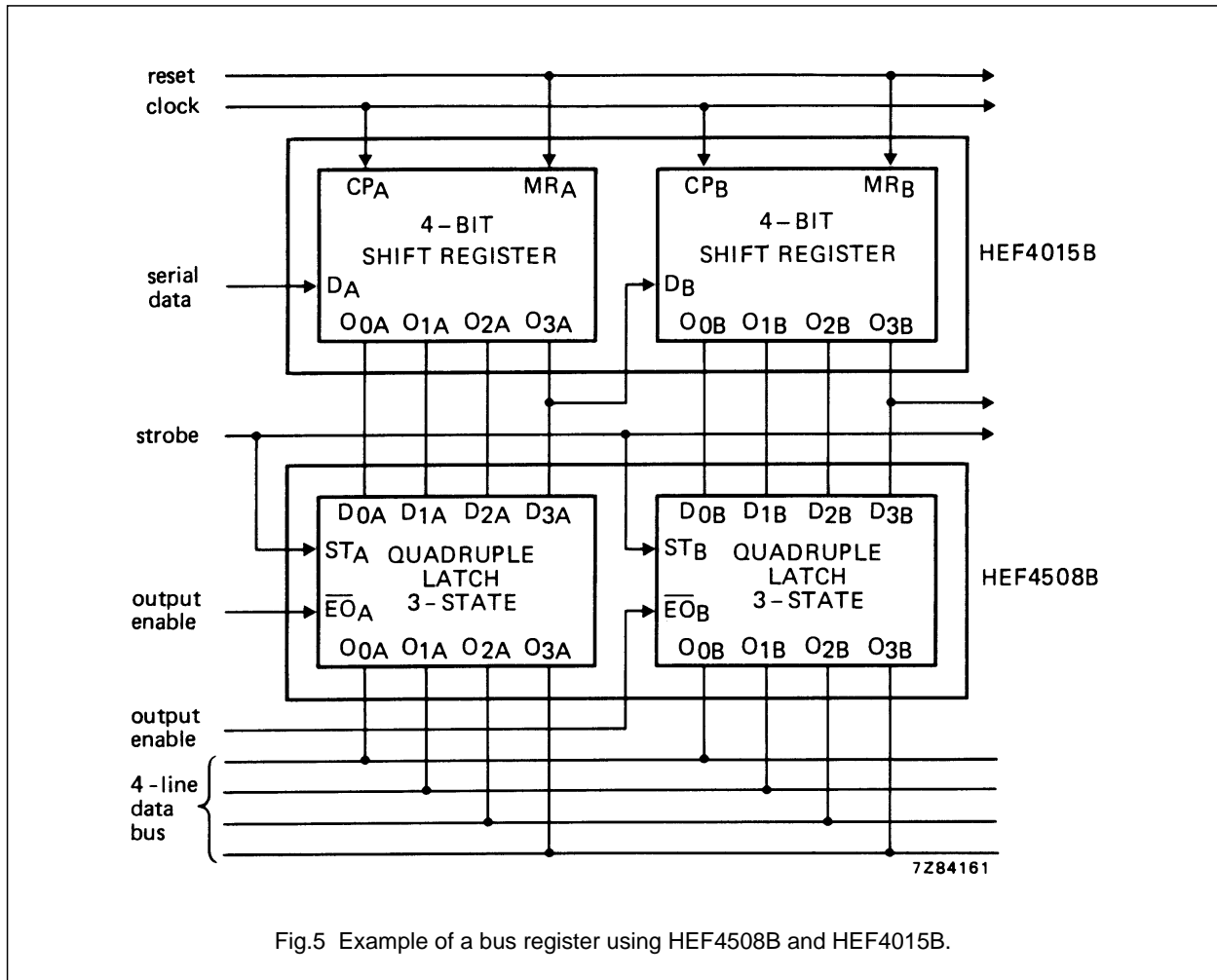
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HEF4508B  
MSI

APPLICATION INFORMATION

Some examples of application for the HEF4508B are:

- Buffer storage
- Holding registers
- Data storage and multiplexing





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HEF4508B  
MSI

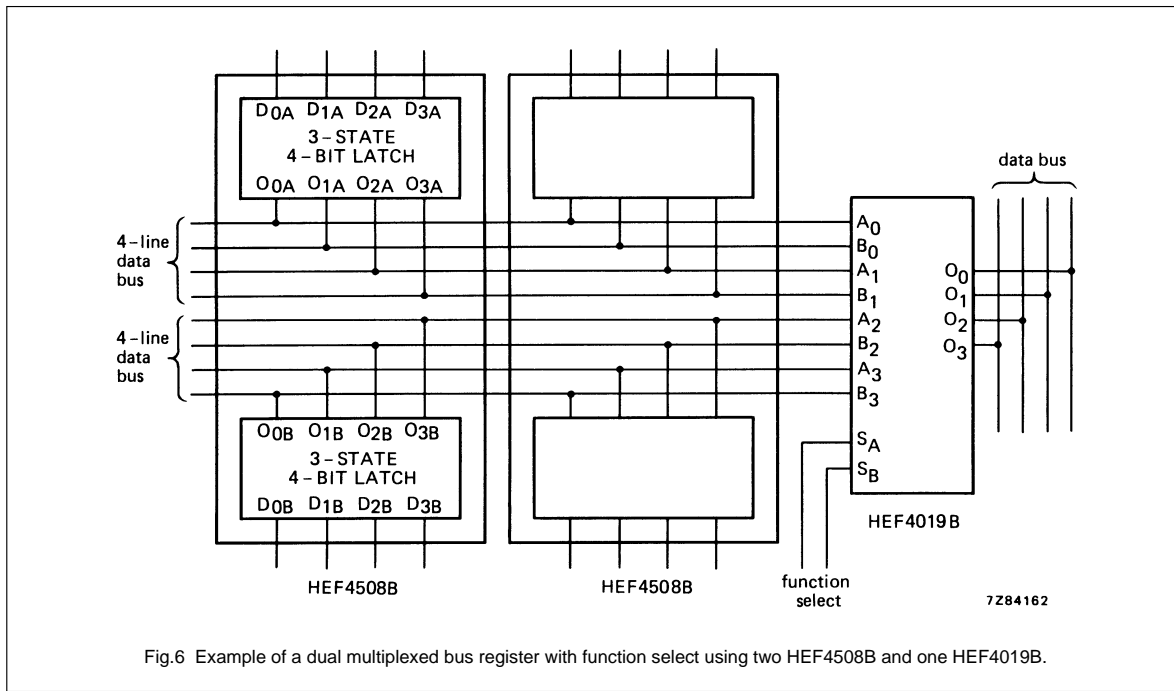


Fig.6 Example of a dual multiplexed bus register with function select using two HEF4508B and one HEF4019B.

FUNCTION SELECT

S <sub>A</sub>	S <sub>B</sub>	FUNCTION
L	L	inhibit (all L)
H	L	select A bus
L	H	select B bus
H	H	A <sub>1</sub> + B <sub>1</sub>