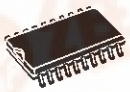
74VHC574

OCTAL D-TYPE FLIP FLOP WITH 3 STATE OUTPUT NON INVERTING

- HIGH SPEED:
  f_{MAX} = 180 MHz (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION:
  I_{CC} = 4 µA (MAX.) at T_A = 25 °C
- HIGH NOISE IMMUNITY:
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- POWER DOWN PROTECTION ON INPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:
  $|I_{OH}| = I_{OL}$ = 8 mA (MIN)
- BALANCED PROPAGATION DELAYS:
  $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:
  V_{CC} (OPR) = 2V to 5.5V
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 574
- IMPROVED LATCH-UP IMMUNITY
- LOW NOISE V_{OLP} = 0.9V (Max.)



M
(Micro Package)

T
(TSSOP Package)

ORDER CODES :

74VHC574M 74VHC574T

DESCRIPTION

The 74VHC574 is an advanced high-speed CMOS OCTAL D-TYPE FLIP FLOP with 3 STATE OUTPUT NON INVERTING fabricated with sub-micron silicon gate and double-layer metal wiring C^2MOS technology.

This 8 bit D-Type flip-flop is controlled by a clock input (CK) and an output enable input ($\overline{OE}$).

On the positive transition of the clock, the Q outputs will be set to logic states that were setup at the D inputs.

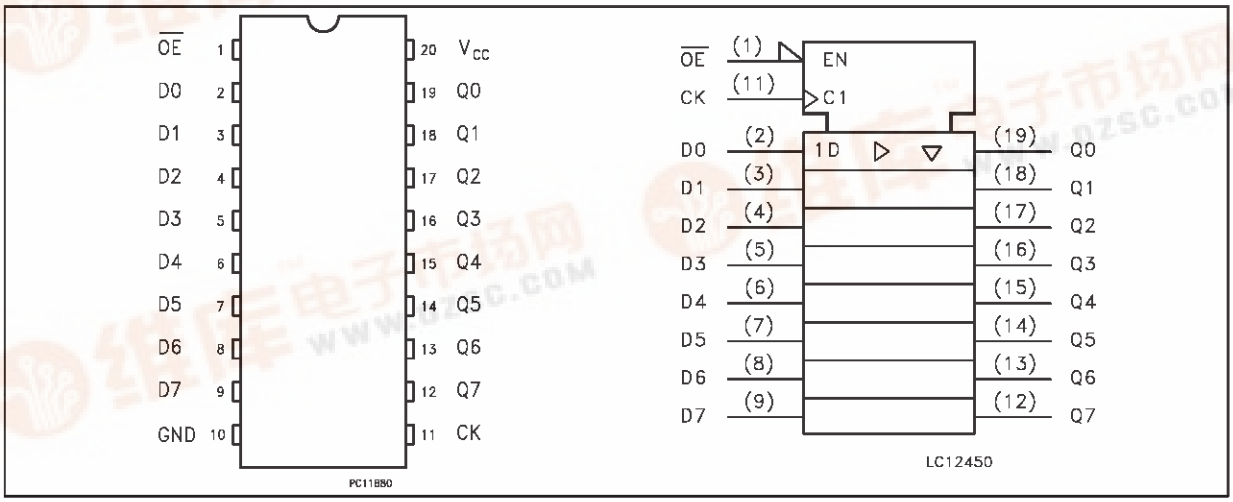
While the $\overline{OE}$ input is low, the 8 outputs will be in a normal logic state (high or low logic level) and, while high level, the outputs will be in a high impedance state.

The output control does not affect the internal operation of flip flop; that is, the old data can be retained or the new data can be entered even while the outputs are off.

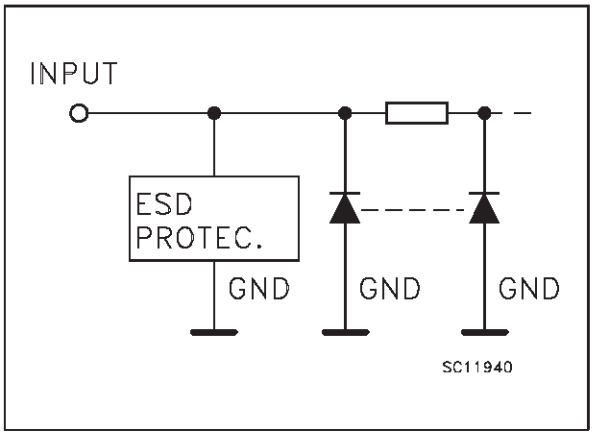
Power down protection is provided on all inputs and 0 to 7V can be accepted on inputs with no regard to the supply voltage. This device can be used to interface 5V to 3V.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS



INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

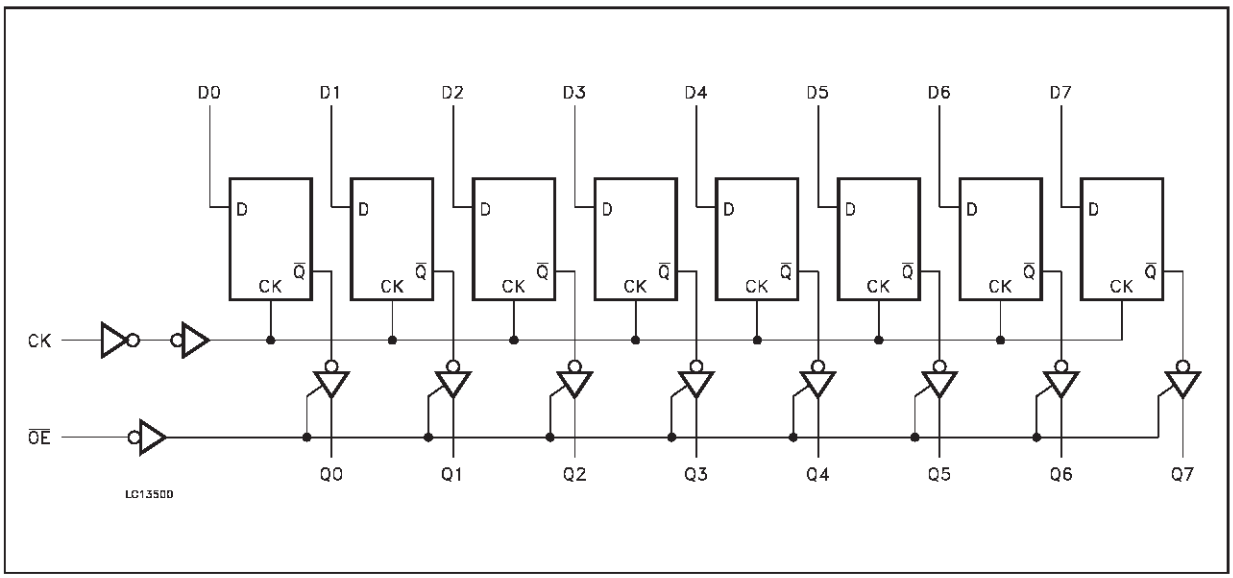
PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3 State Output Enable Input (Active LOW)
2, 3, 4, 5, 6, 7, 8, 9	D0 to D7	Data Inputs
12, 13, 14, 15, 16, 17, 18, 19	Q0 to Q7	3 State Outputs
11	CLOCK	Clock Input (LOW to HIGH, edge triggered)
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

TRUTH TABLE

INPUTS			OUTPUTS
$\overline{OE}$	CK	D	Q
H	X	X	Z
L	↓	X	NO CHANGE
L	↑	L	L
L	↑	H	H

X: Don't Care
Z: High Impedance

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7.0	V
V_I	DC Input Voltage	-0.5 to +7.0	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	- 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 75	mA
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2.0 to 5.5	V
V_I	Input Voltage	0 to 5.5	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature	-40 to +85	°C
dt/dv	Input Rise and Fall Time (see note 1) (V_{CC} = 3.3 ± 0.3V) (V_{CC} = 5.0 ± 0.5V)	0 to 100 0 to 20	ns/V ns/V

1) V_{IN} from 30% to 70% of V_{CC}

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions		Value					Unit
		V_{CC} (V)		T_A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0		1.5			1.5		V
		3.0 to 5.5		0.7V_{CC}			0.7V_{CC}		
V_{IL}	Low Level Input Voltage	2.0				0.5		0.5	V
		3.0 to 5.5				0.3V_{CC}		0.3V_{CC}	
V_{OH}	High Level Output Voltage	2.0	I_O=-50 µA	1.9	2.0		1.9		V
		3.0	I_O=-50 µA	2.9	3.0		2.9		
		4.5	I_O=-50 µA	4.4	4.5		4.4		
		3.0	I_O=-4 mA	2.58			2.48		
		4.5	I_O=-8 mA	3.94			3.8		
V_{OL}	Low Level Output Voltage	2.0	I_O=50 µA		0.0	0.1		0.1	V
		3.0	I_O=50 µA		0.0	0.1		0.1	
		4.5	I_O=50 µA		0.0	0.1		0.1	
		3.0	I_O=4 mA			0.36		0.44	
		4.5	I_O=8 mA			0.36		0.44	
I_{OZ}	High Impedance Output Leakage Current	5.5	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND			±0.25		±2.5	µA
I_I	Input Leakage Current	0 to 5.5	V_I = 5.5V or GND			±0.1		±1.0	µA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND			4		40	µA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3$ ns)

Symbol	Parameter	Test Condition			Value					Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time CK to Q	3.3(*)	15			8.5	13.2	1.0	15.5	ns
		3.3(*)	50			11.0	16.7	1.0	19.0	
		5.0(**)	15			5.6	8.6	1.0	10.0	
		5.0(**)	50			7.1	10.6	1.0	12.0	
t_{PZL} t_{PZH}	Output EnableTime	3.3(*)	15			8.2	12.8	1.0	15.0	ns
		3.3(*)	50			10.7	16.3	1.0	18.5	
		5.0(**)	15			5.9	9.0	1.0	10.5	
		5.0(**)	50			7.4	11.0	1.0	12.5	
t_{PLZ} t_{PHZ}	Output Disable Time	3.3(*)	50			11.0	15.0	1.0	17.0	ns
		5.0(**)	50			7.1	10.1	1.0	11.5	
t_w	Clock Pulse Width HIGH or LOW	3.3(*)					5.0		5.0	ns
		5.0(**)					5.0		5.0	
t_s	Setup Time D to CK HIGH or LOW	3.3(*)					3.5		3.5	ns
		5.0(**)					3.5		3.5	
t_h	Hold Time D to CK HIGH or LOW	3.3(*)					1.5		1.5	ns
		5.0(**)					1.5		1.5	
f_{MAX}	Maximum Clock Frequency	3.3(*)	15		80	125		65		MHz
		3.3(*)	50		50	75		45		
		5.0(**)	15		130	180		110		
		5.0(**)	50		85	115		75		
t_{OSLH} t_{OSHL}	Output to Output Skew Time (note 1)	3.3(*)	50				1.5		1.5	ns
		5.0(**)	50				1.0		1.0	

(*) Voltage range is 3.3V ± 0.3V
(**) Voltage range is 5V ± 0.5V
Note 1: Parameter guaranteed by design. $t_{soLH} = |t_{pLHm} - t_{pLHn}|$, $t_{soHL} = |t_{pHLm} - t_{pHLn}|$

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions	Value					Unit
			T_A = 25 °C			-40 to 85 °C		
			Min.	Typ.	Max.	Min.	Max.	
C_{IN}	Input Capacitance			4	10		10	pF
C_{OUT}	Output Capacitance			6				pF
C_{PD}	Power Dissipation Capacitance (note 1)			28				pF

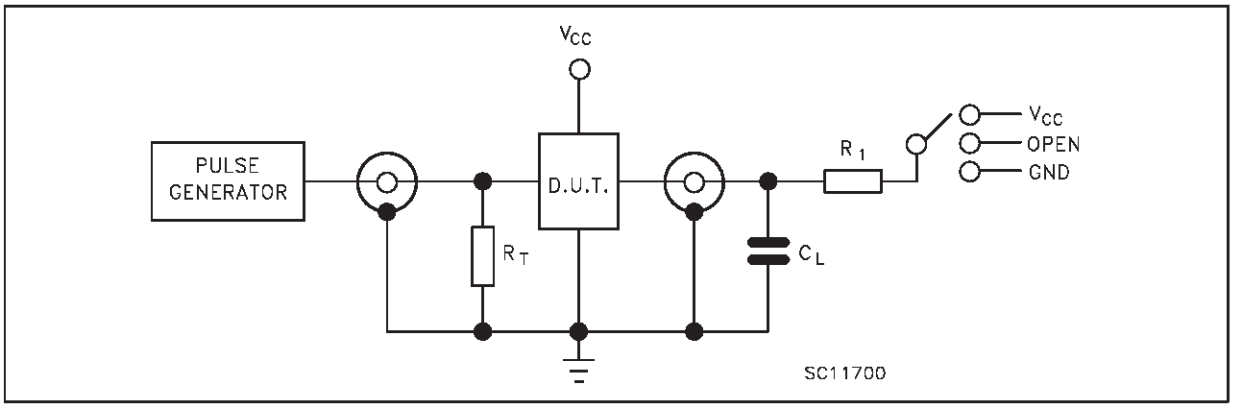
1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \bullet V_{CC} \bullet f_{IN} + I_{CC}/8$ (per Flip-Flop)

DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Conditions		Value					Unit
		V_{CC} (V)		T_A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
V_{OLP}	Dynamic Low Voltage Quiet Output (note 1, 2)	5.0	C_L = 50 pF		0.6	0.9			V
V_{OLV}				-0.9	-0.6				
V_{IHD}	Dynamic High Voltage Input (note 1, 3)	5.0		3.5					
V_{ILD}	Dynamic Low Voltage Input (note 1, 3)	5.0				1.5			

1) Worst case package.
2) Max number of outputs defined as (n). Data inputs are driven 0V to 5.0V, (n -1) outputs switching and one output at GND.
3) Max number of data inputs (n) switching. (n-1) switching 0V to 5.0V. Inputs under test switching: 5.0V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f=1MHz.

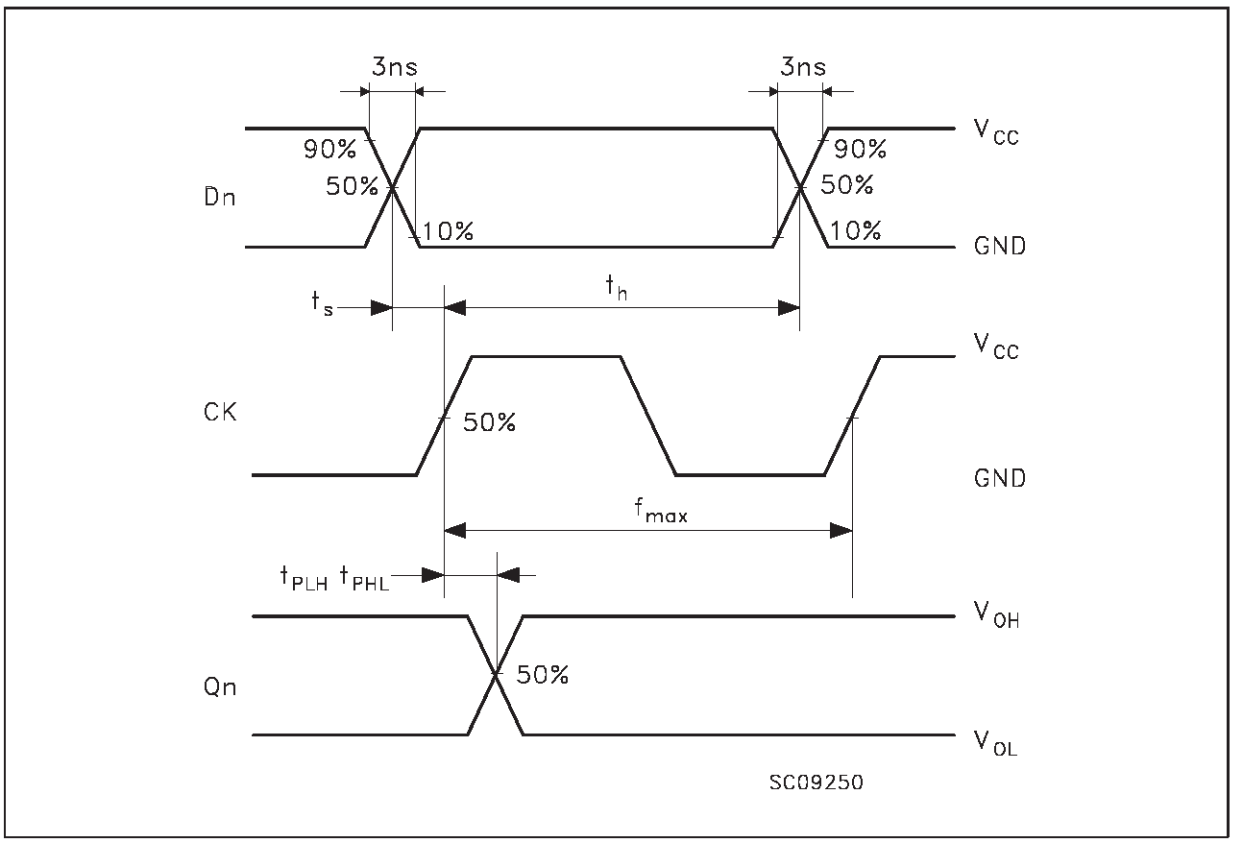
TEST CIRCUIT



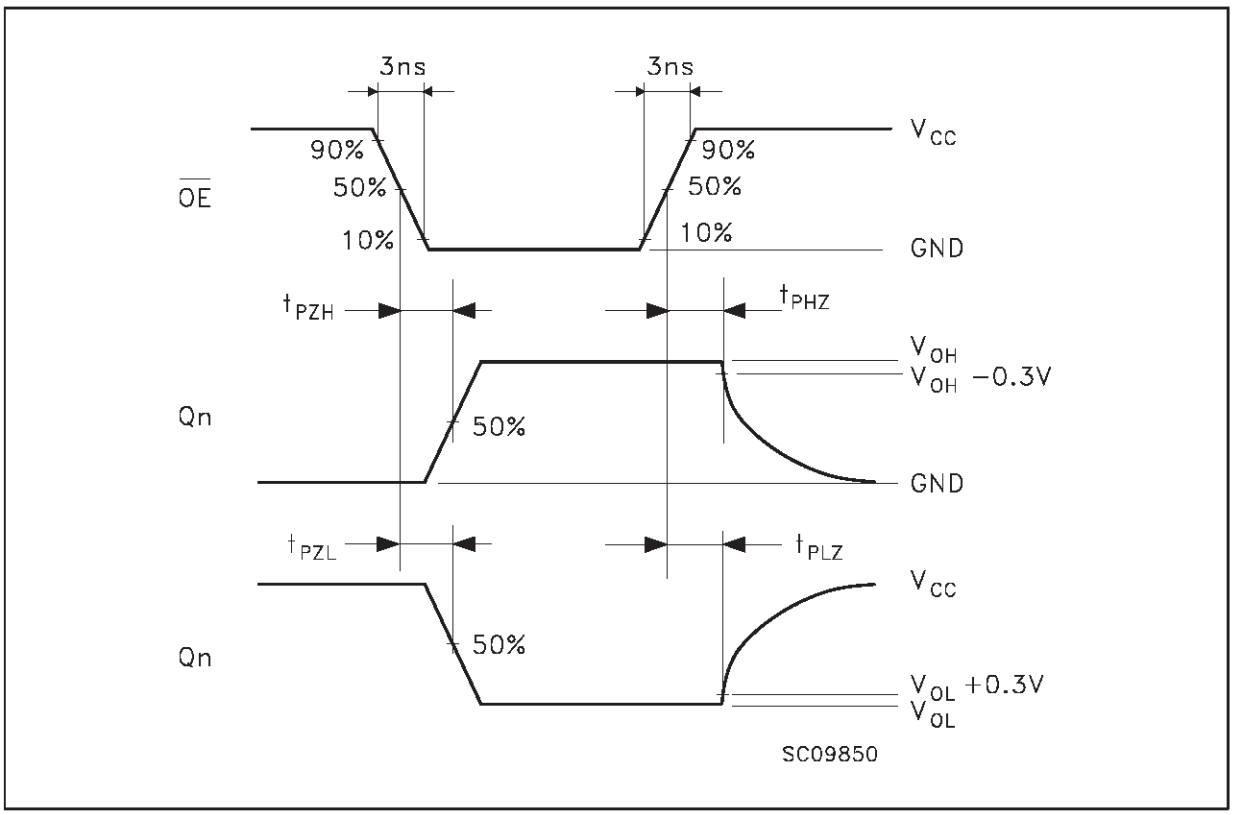
TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	V_{CC}
t_{PZH}, t_{PHZ}	GND

C_L = 15/50 pF or equivalent (includes jig and probe capacitance)
R_L = R_1 = 1KΩ or equivalent
R_T = Z_{OUT} of pulse generator (typically 50Ω)

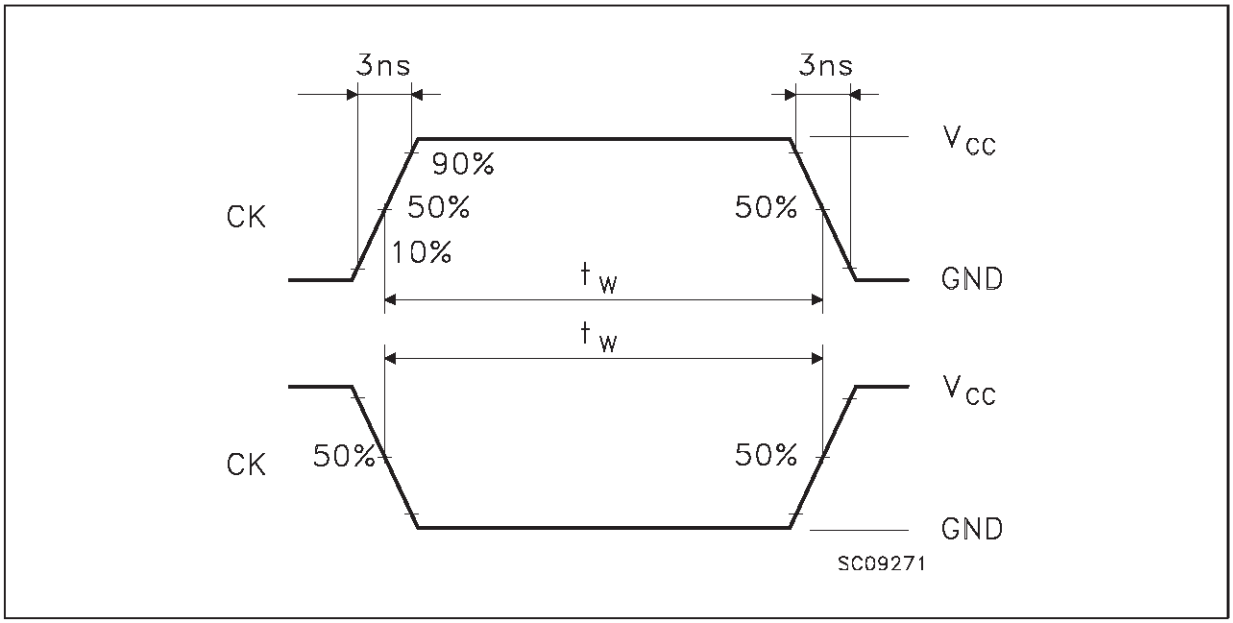
WAVEFORM 1: PROPAGATION DELAYS, SETUP AND HOLD TIMES (f=1MHz; 50% duty cycle)



WAVEFORM 2: OUTPUT ENABLE AND DISABLE TIMES (f=1MHz; 50% duty cycle)

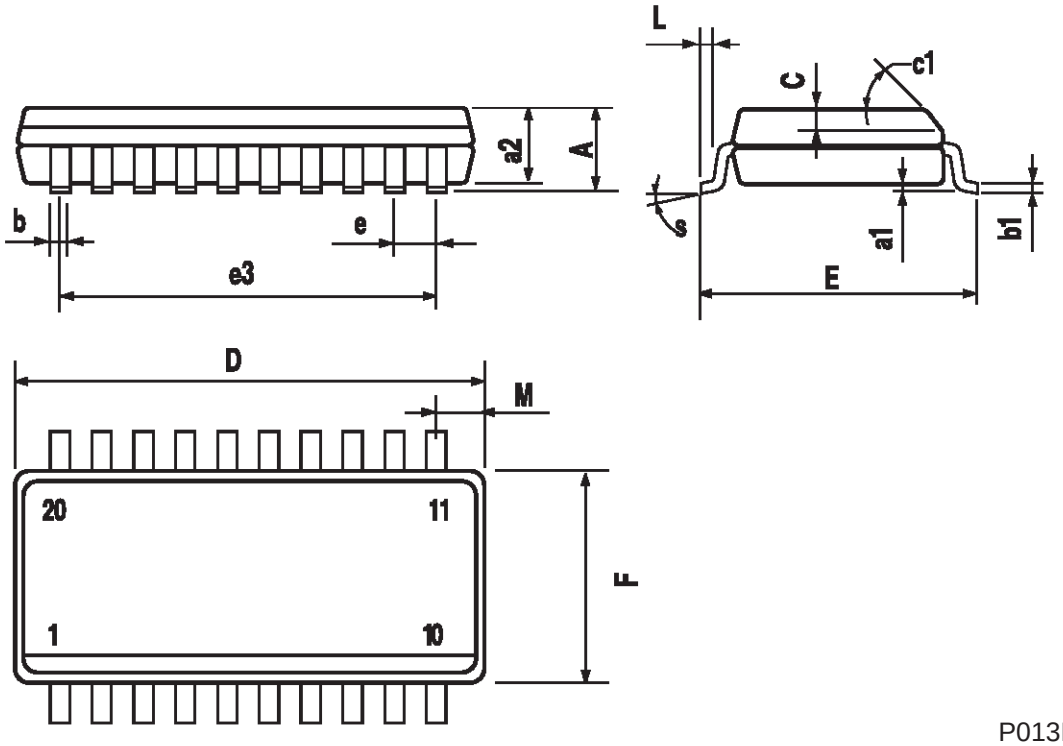


WAVEFORM 3: PULSE WIDTH



SO-20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.10		0.20	0.004		0.007
a2			2.45			0.096
b	0.35		0.49	0.013		0.019
b1	0.23		0.32	0.009		0.012
C		0.50			0.020	
c1	45 (typ.)					
D	12.60		13.00	0.496		0.512
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.40		7.60	0.291		0.299
L	0.50		1.27	0.19		0.050
M			0.75			0.029
S	8 (max.)					



P013L

TSSOP20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.1			0.433
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.85	0.9	0.95	0.335	0.354	0.374
b	0.19		0.30	0.0075		0.0118
c	0.09		0.2	0.0035		0.0079
D	6.4	6.5	6.6	0.252	0.256	0.260
E	6.25	6.4	6.5	0.246	0.252	0.256
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0^o	4^o	8^o	0^o	4^o	8^o
L	0.50	0.60	0.70	0.020	0.024	0.028