

# HD74LV05A

## Hex Inverters with Open Drain Outputs

REJ03D0229-0700

Rev.7.00

Dec 23, 2005

### Description

The HD74LV05A has six inverters with open drain outputs in a 14-pin package.

Low-voltage and high-speed operation is suitable for the battery-powered products (e.g., notebook computers), and the low-power consumption extends the battery life.

### Features

- $V_{CC} = 2.0\text{ V}$  to  $5.5\text{ V}$  operation
- All inputs  $V_{IH}$  (Max.) =  $5.5\text{ V}$  (@ $V_{CC} = 0\text{ V}$  to  $5.5\text{ V}$ )
- All outputs  $V_O$  (Max.) =  $5.5\text{ V}$  (@ $V_{CC} = 0\text{ V}$ )
- All outputs  $V_O$  (Max.) =  $5.5\text{ V}$  (@ $V_{CC} = 2.0\text{ V}$  to  $5.5\text{ V}$ , Output “Z” state)
- Typical  $V_{OL}$  ground bounce <  $0.8\text{ V}$  (@ $V_{CC} = 3.3\text{ V}$ ,  $T_a = 25^\circ\text{C}$ )
- Output current:  $\pm 6\text{ mA}$  (@ $V_{CC} = 3.0\text{ V}$  to  $3.6\text{ V}$ ),  $\pm 12\text{ mA}$  (@ $V_{CC} = 4.5\text{ V}$  to  $5.5\text{ V}$ )
- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LV05AFPEL	SOP-14 pin(JEITA)	PRSP0014DF-B (FP-14DAV)	FP	EL (2,000 pcs/reel)
HD74LV05ARPEL	SOP-14 pin(JEDEC)	PRSP0014DE-A (FP-14DNV)	RP	EL (2,500 pcs/reel)
HD74LV05ATELL	TSSOP-14 pin	PTSP0014JA-B (TTP-14DV)	T	ELL (2,000 pcs/reel)

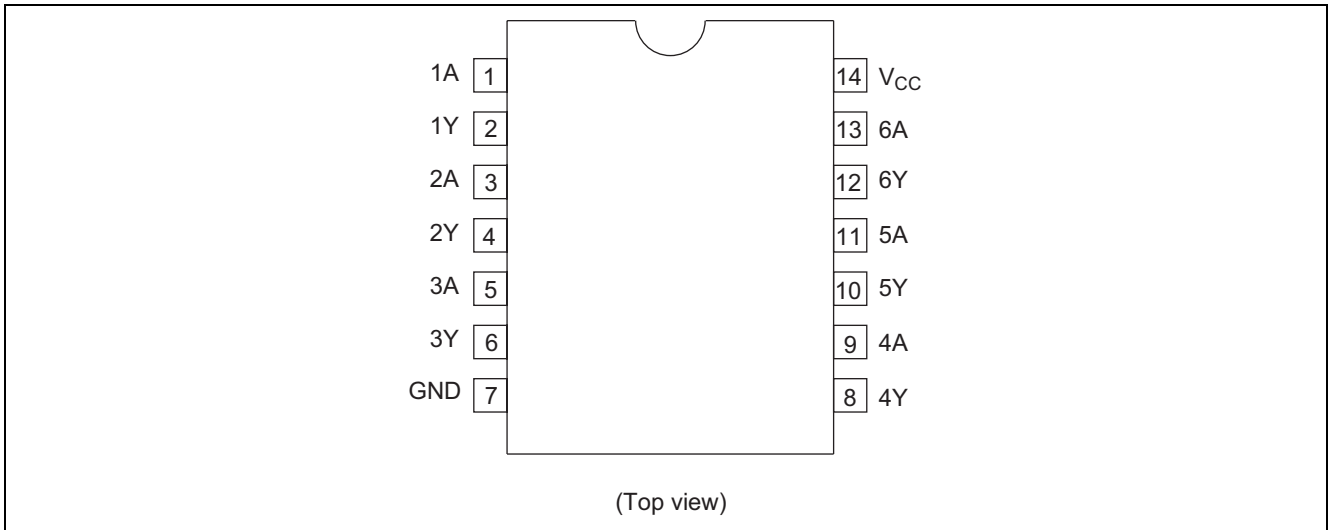
Note: Please consult the sales office for the above package availability.

### Function Table

Input A	Output Y
L	Z
H	L

Note: H: High level  
L: Low level  
Z: High impedance

## Pin Arrangement



## Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage range	$V_{CC}$	-0.5 to 7.0	V	
Input voltage range* <sup>1</sup>	$V_I$	-0.5 to 7.0	V	
Output voltage range* <sup>1, 2</sup>	$V_O$	-0.5 to $V_{CC} + 0.5$	V	Output: L
		-0.5 to 7.0		$V_{CC}$ : OFF or Output: Z
Input clamp current	$I_{IK}$	-20	mA	$V_I < 0$
Output clamp current	$I_{OK}$	$\pm 50$	mA	$V_O < 0$
Continuous output current	$I_O$	$\pm 25$	mA	$V_O = 0$ to $V_{CC}$
Continuous current through $V_{CC}$ or GND	$I_{CC}$ or $I_{GND}$	$\pm 50$	mA	
Maximum power dissipation at $T_a = 25^\circ\text{C}$ (in still air) * <sup>3</sup>	$P_T$	785	mW	SOP
		500		TSSOP
Storage temperature	$T_{stg}$	-65 to 150	$^\circ\text{C}$	

Notes: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

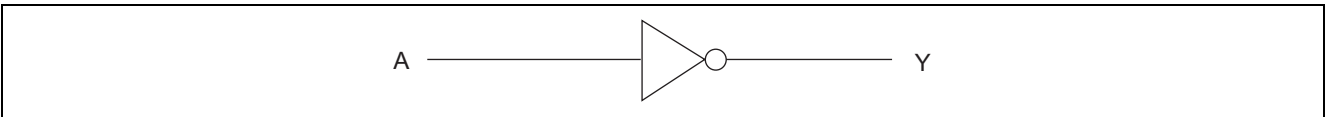
1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 7.0 V maximum.
3. The maximum package power dissipation was calculated using a junction temperature of 150°C.

### Recommended Operating Conditions

Item	Symbol	Min	Max	Unit	Conditions
Supply voltage range	$V_{CC}$	2.0	5.5	V	
Input voltage range	$V_I$	0	5.5	V	
Output voltage range	$V_O$	0	5.5	V	
Output current	$I_{OL}$	—	50	$\mu A$	$V_{CC} = 2.0 V$
		—	2	mA	$V_{CC} = 2.3 \text{ to } 2.7 V$
		—	6		$V_{CC} = 3.0 \text{ to } 3.6 V$
		—	12		$V_{CC} = 4.5 \text{ to } 5.5 V$
Input transition rise or fall rate	$\Delta t / \Delta v$	0	200	ns/V	$V_{CC} = 2.3 \text{ to } 2.7 V$
		0	100		$V_{CC} = 3.0 \text{ to } 3.6 V$
		0	20		$V_{CC} = 4.5 \text{ to } 5.5 V$
Operating free-air temperature	$T_a$	-40	85	$^{\circ}C$	

Note: Unused or floating inputs must be held high or low.

### Logic Diagram



### DC Electrical Characteristics

$T_a = -40 \text{ to } 85^{\circ}C$

Item	Symbol	$V_{CC} (V) *$	Min	Typ	Max	Unit	Test Conditions
Input voltage	$V_{IH}$	2.0	1.5	—	—	V	
		2.3 to 2.7	$V_{CC} \times 0.7$	—	—		
		3.0 to 3.6	$V_{CC} \times 0.7$	—	—		
		4.5 to 5.5	$V_{CC} \times 0.7$	—	—		
	$V_{IL}$	2.0	—	—	0.5		
		2.3 to 2.7	—	—	$V_{CC} \times 0.3$		
		3.0 to 3.6	—	—	$V_{CC} \times 0.3$		
		4.5 to 5.5	—	—	$V_{CC} \times 0.3$		
Output voltage	$V_{OL}$	Min to Max	—	—	0.1	V	$I_{OL} = 50 \mu A$
		2.3	—	—	0.4		$I_{OL} = 2 \text{ mA}$
		3.0	—	—	0.44		$I_{OL} = 6 \text{ mA}$
		4.5	—	—	0.55		$I_{OL} = 12 \text{ mA}$
Input current	$I_{IN}$	0 to 5.5	—	—	$\pm 1$	$\mu A$	$V_{IN} = 5.5 V \text{ or } GND$
Off state output current	$I_{OZ}$	Min to Max	—	—	$\pm 2.5$	$\mu A$	$V_O = 5.5 V$
Quiescent supply current	$I_{CC}$	5.5	—	—	20	$\mu A$	$V_{IN} = V_{CC} \text{ or } GND, I_o = 0$
Output leakage current	$I_{OFF}$	0	—	—	5	$\mu A$	$V_I \text{ or } V_O = 0 \text{ to } 5.5 V$
Input capacitance	$C_{IN}$	3.3	—	2.3	—	pF	$V_I = V_{CC} \text{ or } GND$

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

## Switching Characteristics

$V_{CC} = 2.5 \pm 0.2 \text{ V}$

Item	Symbol	$T_a = 25^\circ\text{C}$			$T_a = -40 \text{ to } 85^\circ\text{C}$		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Propagation delay time	$t_{PLH}$	—	4.7	10.4	1.0	13.0	ns	$C_L = 15 \text{ pF}$	A	Y
		—	9.5	15.2	1.0	18.0		$C_L = 50 \text{ pF}$		
	$t_{PHL}$	—	5.4	10.4	1.0	13.0		$C_L = 15 \text{ pF}$		
		—	7.9	15.2	1.0	18.0		$C_L = 50 \text{ pF}$		

$V_{CC} = 3.3 \pm 0.3 \text{ V}$

Item	Symbol	$T_a = 25^\circ\text{C}$			$T_a = -40 \text{ to } 85^\circ\text{C}$		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Propagation delay time	$t_{PLH}$	—	4.0	7.1	1.0	8.5	ns	$C_L = 15 \text{ pF}$	A	Y
		—	7.3	10.6	1.0	12.0		$C_L = 50 \text{ pF}$		
	$t_{PHL}$	—	4.3	7.1	1.0	8.5		$C_L = 15 \text{ pF}$		
		—	5.8	10.6	1.0	12.0		$C_L = 50 \text{ pF}$		

$V_{CC} = 5.0 \pm 0.5 \text{ V}$

Item	Symbol	$T_a = 25^\circ\text{C}$			$T_a = -40 \text{ to } 85^\circ\text{C}$		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Propagation delay time	$t_{PLH}$	—	3.3	5.5	1.0	6.5	ns	$C_L = 15 \text{ pF}$	A	Y
		—	5.6	7.5	1.0	8.5		$C_L = 50 \text{ pF}$		
	$t_{PHL}$	—	3.4	5.5	1.0	6.5		$C_L = 15 \text{ pF}$		
		—	4.1	7.5	1.0	8.5		$C_L = 50 \text{ pF}$		

## Operating Characteristics

$C_L = 50 \text{ pF}$

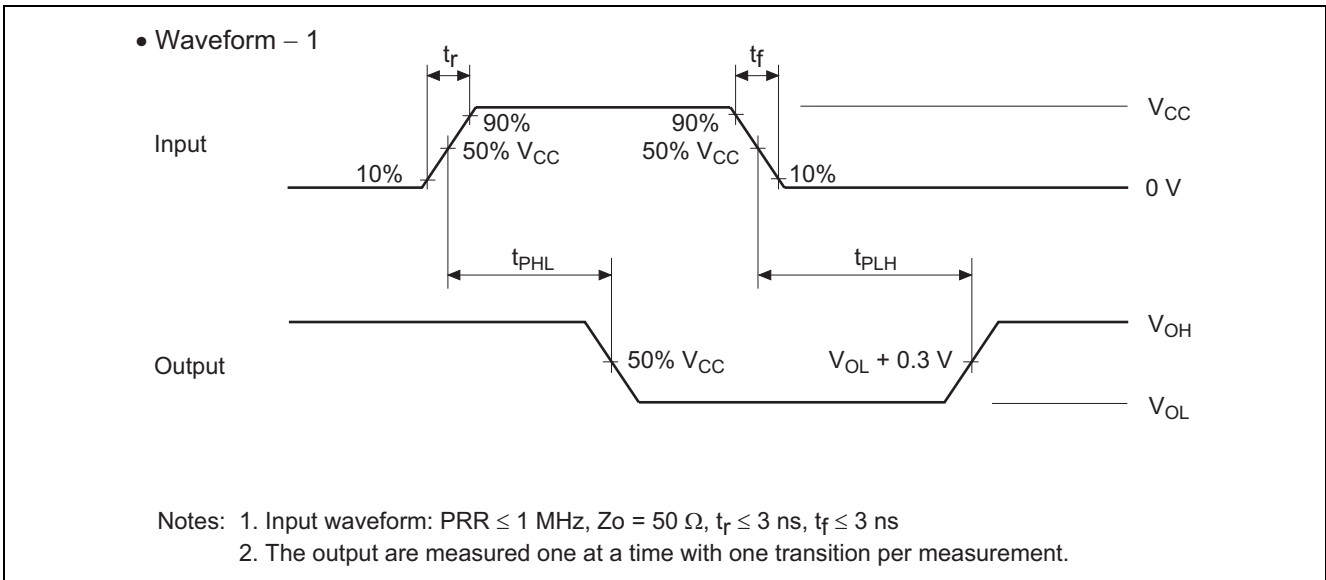
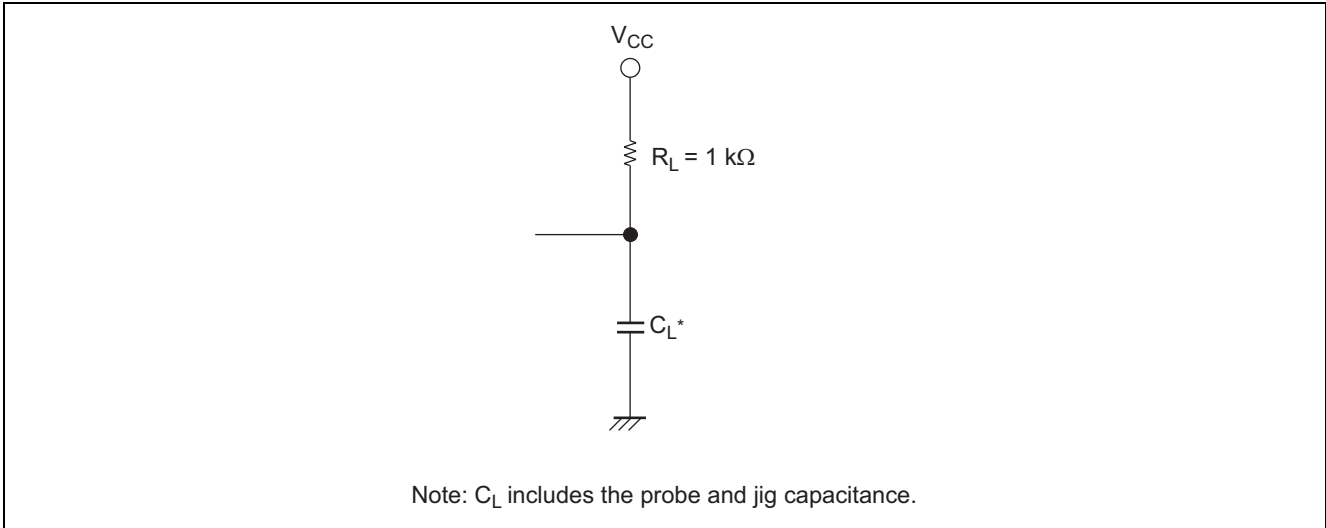
Item	Symbol	$V_{CC} \text{ (V)}$	$T_a = 25^\circ\text{C}$			Unit	Test Conditions
			Min	Typ	Max		
Power dissipation capacitance	$C_{PD}$	3.3	—	2.5	—	pF	$f = 10 \text{ MHz}$
		5.0	—	3.0	—		

## Noise Characteristics

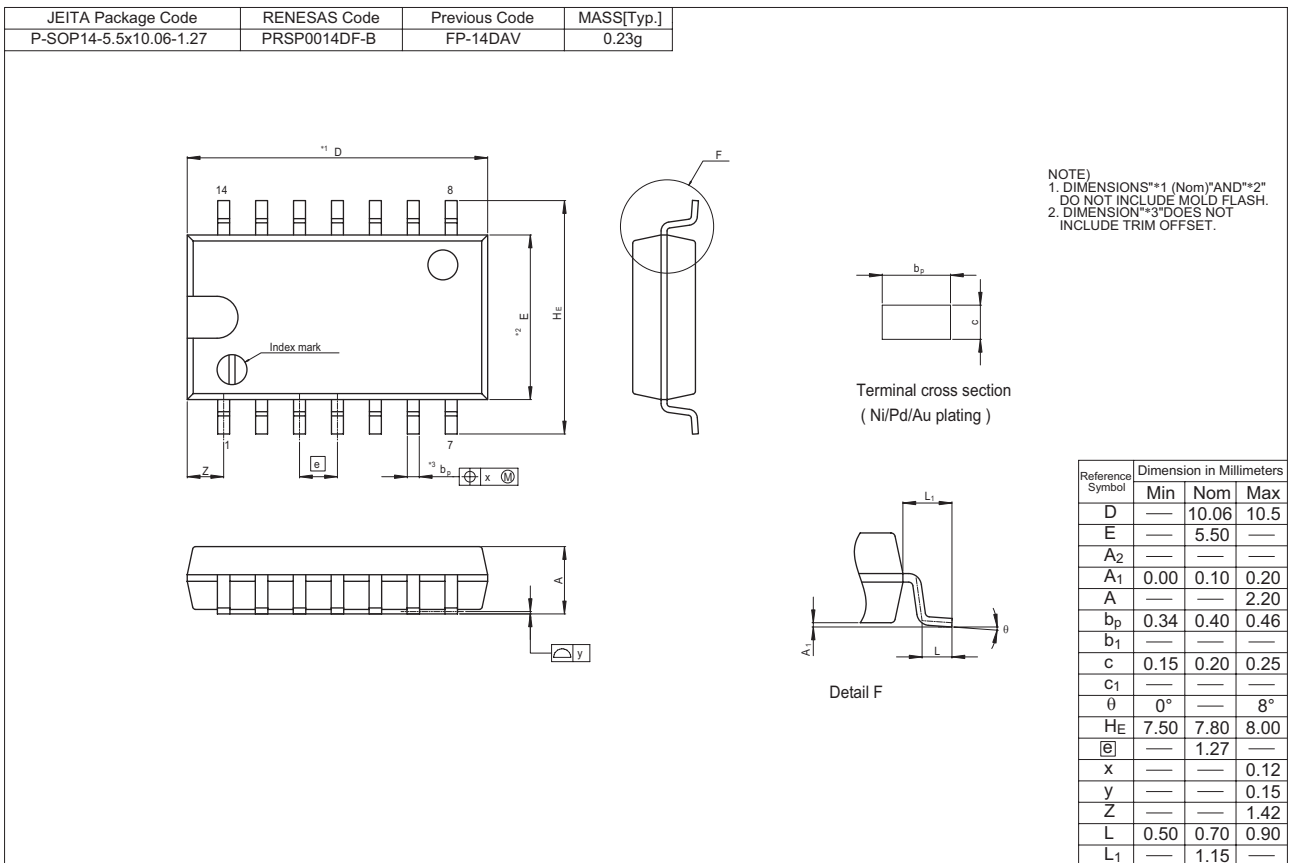
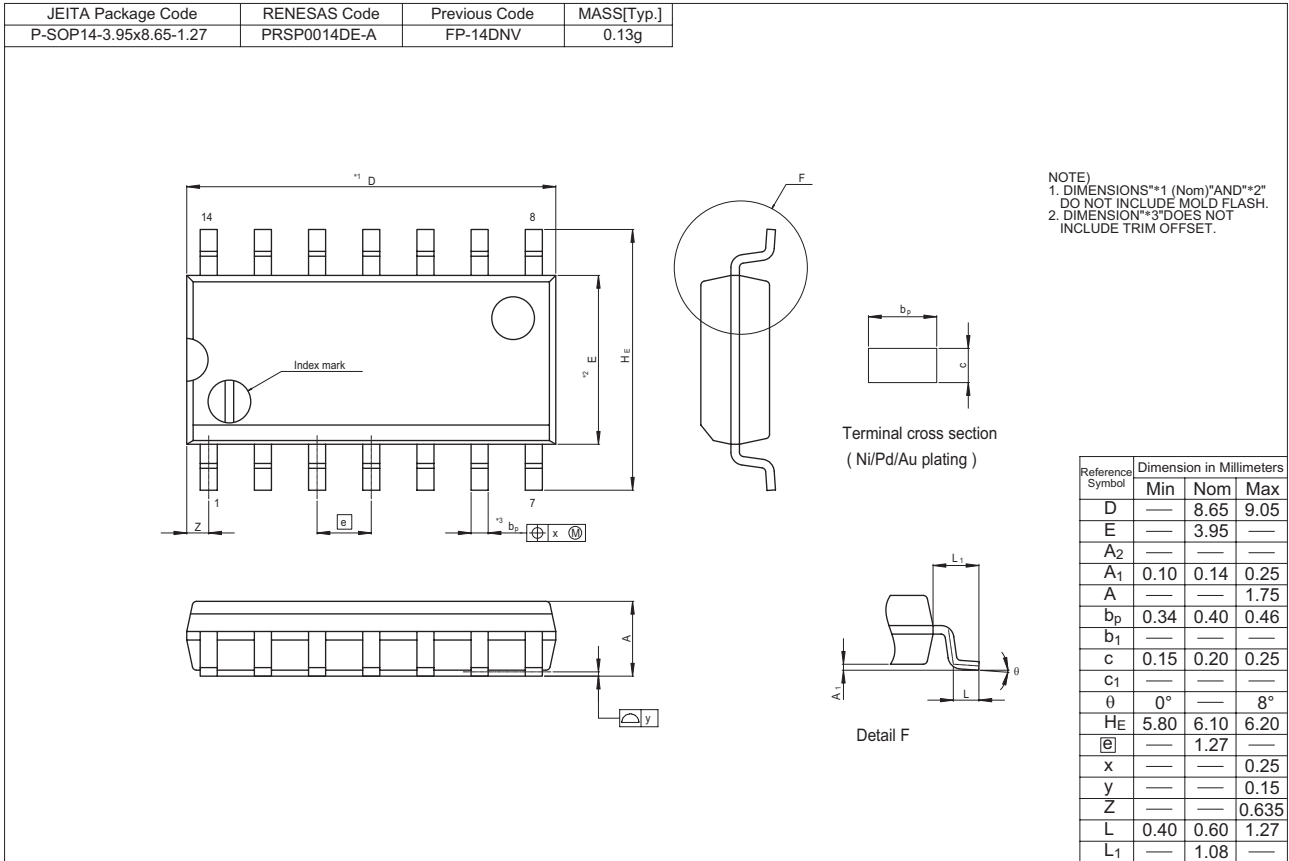
$C_L = 50 \text{ pF}$

Item	Symbol	$V_{CC} \text{ (V)}$	$T_a = 25^\circ\text{C}$			Unit	Test Conditions
			Min	Typ	Max		
Quiet output, maximum dynamic $V_{OL}$	$V_{OL(P)}$	3.3	—	0.3	0.8	V	
Quiet output, minimum dynamic $V_{OL}$	$V_{OL(V)}$	3.3	—	-0.1	-0.8	V	
High-level dynamic input voltage	$V_{IH(D)}$	3.3	2.31	—	—	V	
Low-level dynamic input voltage	$V_{IL(D)}$	3.3	—	—	0.99	V	

Test Circuit

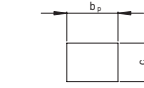
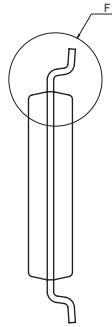
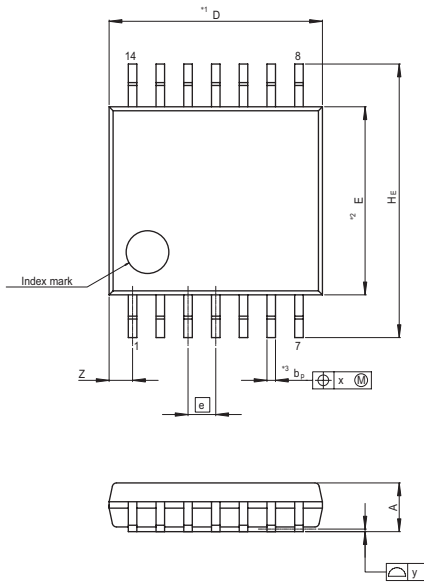


Package Dimensions

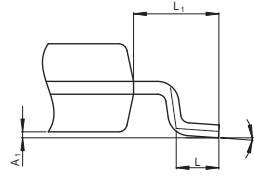


# HD74LV05A

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TSSOP14-4.4x5-0.65	PTSP0014JA-B	TTP-14DV	0.05g



Terminal cross section  
( Ni/Pd/Au plating )



Detail F

NOTE)  
1. DIMENSIONS\*1 (Nom)\*AND\*2\*  
DO NOT INCLUDE MOLD FLASH.  
2. DIMENSION\*3\*DOES NOT  
INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	5.00	5.30
E	—	4.40	—
A <sub>2</sub>	—	—	—
A <sub>1</sub>	0.03	0.07	0.10
A	—	—	1.10
$b_p$	0.15	0.20	0.25
$d_1$	—	—	—
c	0.10	0.15	0.20
$c_1$	—	—	—
$\theta$	0°	—	8°
HE	6.20	6.40	6.60
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z	—	—	0.83
L	0.4	0.5	0.6
L <sub>1</sub>	—	1.0	—

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**Renesas Technology America, Inc.**

450 Holger Way, San Jose, CA 95134-1368, U.S.A  
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

**Renesas Technology Europe Limited**

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.  
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

**Renesas Technology (Shanghai) Co., Ltd.**

Unit 205, AZIA Center, No.133 Yincheng Rd (n), Pudong District, Shanghai 200120, China  
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7898

**Renesas Technology Hong Kong Ltd.**

7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong  
Tel: <852> 2265-6688, Fax: <852> 2730-6071

**Renesas Technology Taiwan Co., Ltd.**

10th Floor, No.99, Fushing North Road, Taipei, Taiwan  
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

**Renesas Technology Singapore Pte. Ltd.**

1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632  
Tel: <65> 6213-0200, Fax: <65> 6278-8001

**Renesas Technology Korea Co., Ltd.**

Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea  
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

**Renesas Technology Malaysia Sdn. Bhd**

Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia  
Tel: <603> 7955-9390, Fax: <603> 7955-9510