National Semiconductor

November 1994

54F/74F109
Dual $J\overline{K}$ Positive Edge-Triggered Flip-Flop

General Description

The 'F109 consists of two high-speed, completely independent transition clocked $J\overline{K}$ flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The $J\overline{K}$ design allows operation as a D flip-flop (refer to 'F74 data sheet) by connecting the J and $\overline{K}$ inputs.

Asynchronous Inputs:

LOW input to $\overline{S}_D$ sets Q to HIGH level

LOW input to $\overline{C}_D$ sets Q to LOW level

Clear and Set are independent of clock

Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

Features

- Guaranteed 4000V minimum ESD protection.

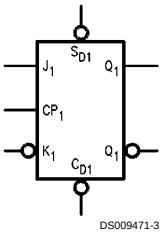
Ordering Code: See Section 0

Commercial	Military	Package Number	Package Description
74F109PC		N16E	16-Lead (0.300" Wide) Molded Dual-in-Line
	54F109DM (Note 2)	J16A	16-Lead Ceramic Dual-in-Line
74F109SC (Note 1)		M16A	16-Lead (0.150" Wide) Molded Small Outline, JEDEC
74F109SJ (Note 1)		M16D	16-Lead (0.300" Wide) Molded Small Outline, EIAJ
	54F109FM (Note 2)	W16A	16-Lead Cerpack
	54F109LM (Note 2)	E20A	16-Lead Ceramic Leadless Chip Carrier, Type C

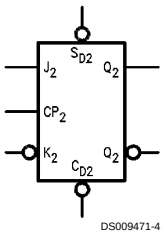
Note 1: Devices also available in 13" reel. Use suffix = SCX and SJX.

Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB.

Logic Symbols

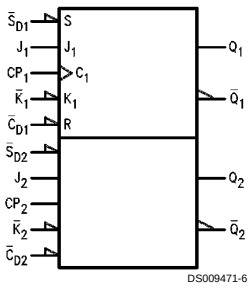


DS009471-3



DS009471-4

IEEE/IEC



DS009471-6

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54F/74F109 Dual $J\overline{K}$ Positive Edge-Triggered Flip-Flop

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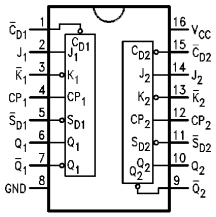
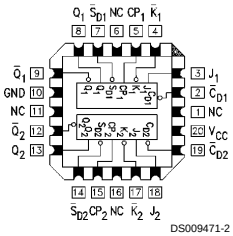
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



Pin Assignment for LCC



Unit Loading/Fan Out

See Section 0 for U.L. definitions

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Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
J_1, J_2, $\overline{K}_1$, $\overline{K}_2$	Data Inputs	1.0/1.0	20 µA/−0.6 mA
CP_1, CP_2	Clock Pulse Inputs (Active Rising Edge)	1.0/1.0	20 µA/−0.6 mA
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs (Active LOW)	1.0/3.0	20 µA/−1.8 mA
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs (Active LOW)	1.0/3.0	20 µA/−1.8 mA
Q_1, Q_2, $\overline{Q}_1$, $\overline{Q}_2$	Outputs	50/33.3	−1 mA/20 mA

Truth Table

Inputs					Outputs	
$\overline{S}_D$	$\overline{C}_D$	CP	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H	H
H	H	⌐	l	l	L	H
H	H	⌐	h	l	Toggle	
H	H	⌐	l	h	Q_0	$\overline{Q}_0$
H	H	⌐	h	h	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

H (h) = HIGH Voltage Level
L (l) = LOW Voltage Level
⌐ = LOW-to-HIGH Transition
X = Immaterial
Q_0 ($\overline{Q}_0$) = Before LOW-to-HIGH Transition of Clock
Lower case letters indicate the state of the referenced output one setup time prior to the LOW-to-HIGH clock transition.

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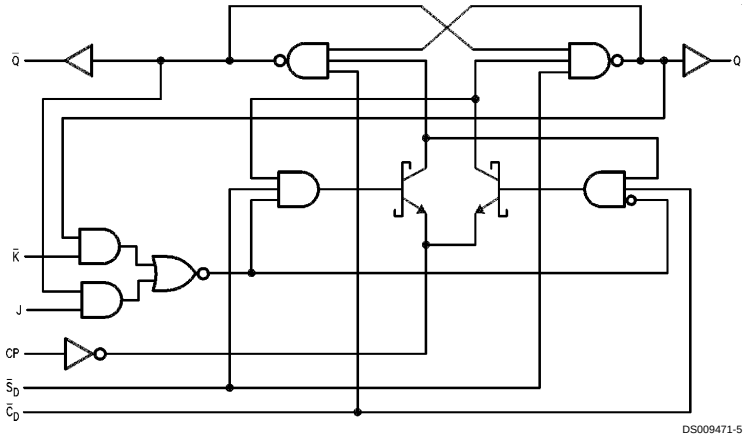
Logic Diagram (One Half Shown)



DS009471-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

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Absolute Maximum Ratings (Note 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature	−65˚C to +150˚C
Ambient Temperature under Bias	−55˚C to +125˚C
Junction Temperature under Bias	−55˚C to +175˚C
Plastic	−55˚C to +150˚C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 4)	−0.5V to +7.0V
Input Current (Note 4)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE® Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55˚C to +125˚C
Commercial	0˚C to +70˚C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

Note 3: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 4: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		54F/74F Min	54F/74F Typ	54F/74F Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54F 10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA
		74F 10% V_{CC}	2.5					I_{OH} = −1 mA
		74F 5% V_{CC}	2.7					I_{OH} = −1 mA
V_{OL}	Output LOW Voltage	54F 10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA
		74F 10% V_{CC}			0.5			I_{OL} = 20 mA
I_{IH}	Input HIGH Current	54F			20.0	µA	Max	V_{IN} = 2.7V
		74F			5.0			
I_{BVI}	Input HIGH Current Breakdown Test	54F			100	µA	Max	V_{IN} = 7.0V
		74F			7.0			
I_{CEX}	Output HIGH Leakage Current	54F			250	µA	Max	V_{OUT} = V_{CC}
		74F			50			
V_{ID}	Input Leakage Test	74F	4.75			V	0.0	I_{ID} = 1.9 µA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current	74F			3.75	µA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V (J_n, $\overline{K}_n$)
					−1.8	mA	Max	V_{IN} = 0.5V ($\overline{C}_{Dn}$, $\overline{S}_{Dn}$)
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V
I_{CC}	Power Supply Current			11.7	17.0	mA	Max	CP = 0V

AC Electrical Characteristics

See Section 0 for Waveforms and Load Configurations

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Symbol	Parameter	74F T_A = +25˚C, V_{CC} = +5.0V, C_L = 50 pF Min	Typ	Max	54F T_A, V_{CC} = Mil, C_L = 50 pF Min	Max	74F T_A, V_{CC} = Com, C_L = 50 pF Min	Max	Units	Fig. No.
f_{max}	Maximum Clock Frequency	100	125		70		90		MHz	♦♦-♦♦

DSXXX

AC Electrical Characteristics (Continued)

See Section 0 for Waveforms and Load Configurations

Symbol	Parameter	74F T_A = +25°C V_{CC} = +5.0V C_L = 50 pF			54F T_A, V_{CC} = Mil C_L = 50 pF		74F T_A, V_{CC} = Com C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.8	5.3	7.0	3.8	9.0	3.8	8.0	ns	♦♦-♦♦
t_{PHL}	CP_n to Q_n or $\overline{Q}_n$	4.4	6.2	8.0	4.4	10.5	4.4	9.2		
t_{PLH}	Propagation Delay	3.2	5.2	7.0	3.2	9.0	3.2	8.0		
t_{PHL}	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	3.5	7.0	9.0	3.5	11.5	3.5	10.5	ns	♦♦-♦♦

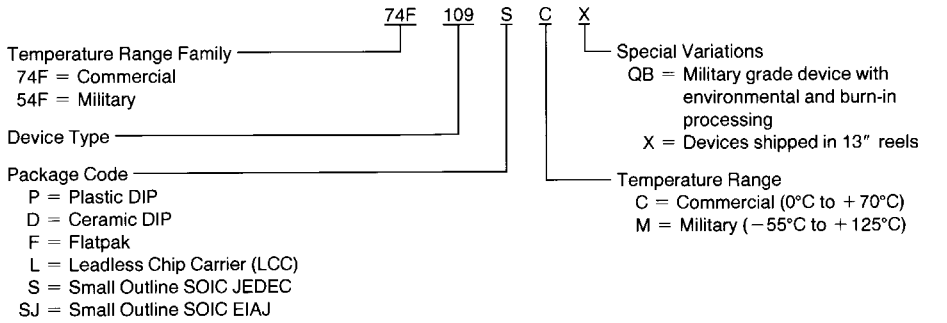
AC Operating Requirements

See Section 0 for Waveforms

Symbol	Parameter	74F T_A = +25°C V_{CC} = +5.0V		54F T_A, V_{CC} = Mil		74F T_A, V_{CC} = Com		Units	Fig. No.
		Min	Max	Min	Max	Min	Max		
$t_s(H)$	Setup Time, HIGH or LOW	3.0		3.0		3.0			
$t_s(L)$	J_n or $\overline{K}_n$ to CP_n	3.0		4.0		3.0		ns	♦♦-♦♦
$t_h(H)$	Hold Time, HIGH or LOW	1.0		1.0		1.0			
$t_h(L)$	J_n or $\overline{K}_n$ to CP_n	1.0		1.0		1.0			
$t_w(H)$	CP_n Pulse Width	4.0		4.0		4.0		ns	♦♦-♦♦
$t_w(L)$	HIGH or LOW	5.0		5.0		5.0			
$t_w(L)$	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width, LOW	4.0		4.0		4.0		ns	♦♦-♦♦
t_{rec}	Recovery Time $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP	2.0		2.0		2.0		ns	♦♦-♦♦

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



DS009471-7

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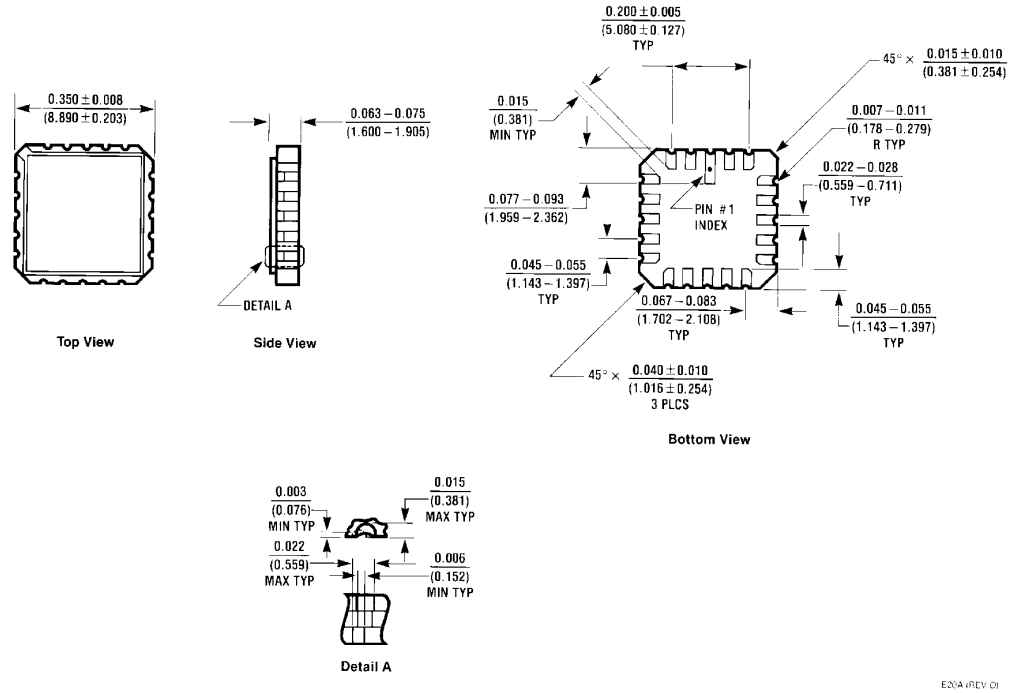
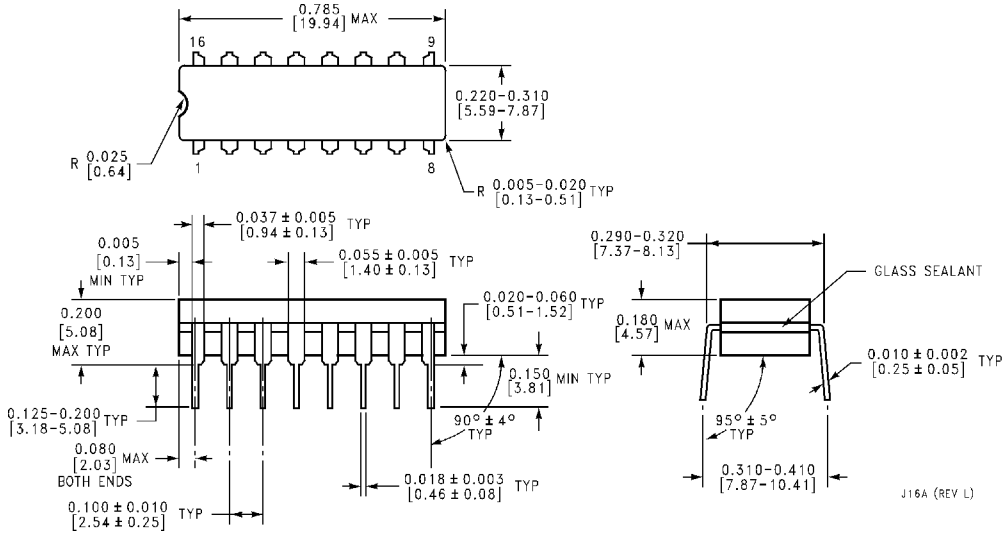
Physical Dimensions inches (millimeters) unless otherwise noted

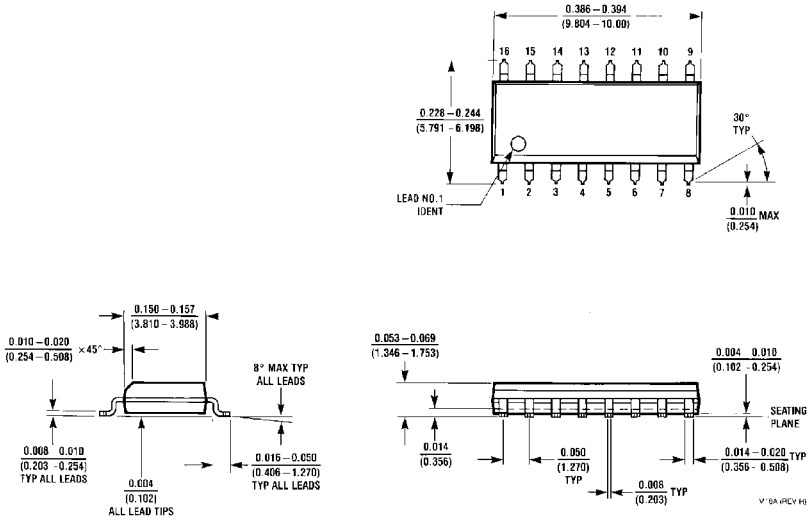


20-Lead Ceramic Leadless Chip Carrier (L)
NS Package Number E20A

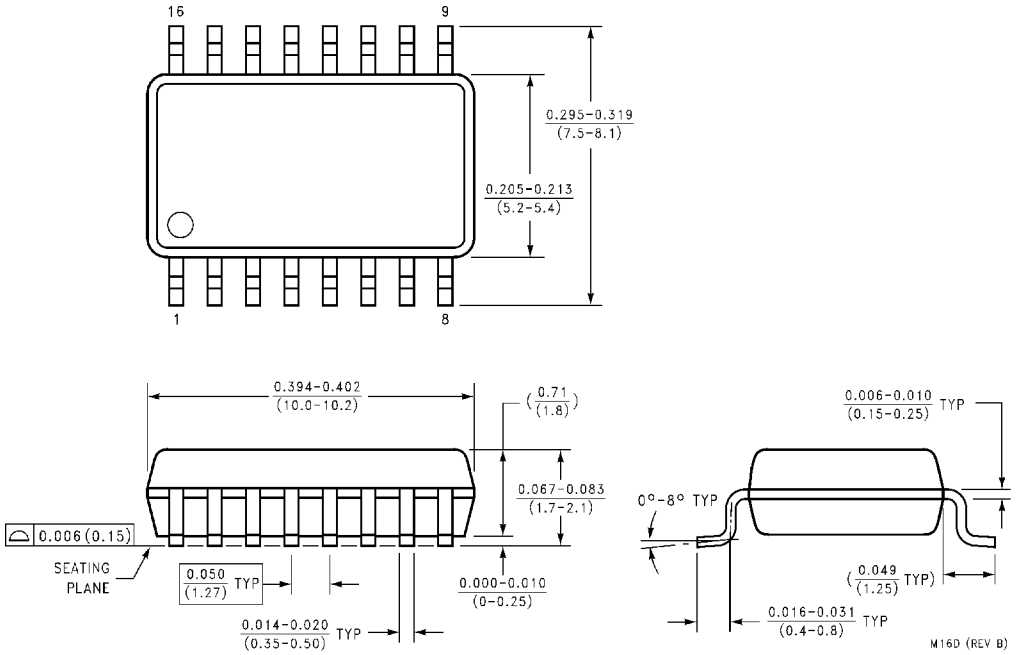


16-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead (0.150" Wide) Molded Small Outline Package, JEDEC (S)
NS Package Number M16A



16-Lead (0.300" Wide) Molded Small Outline Package, EIAJ (SJ)
NS Package Number M16D

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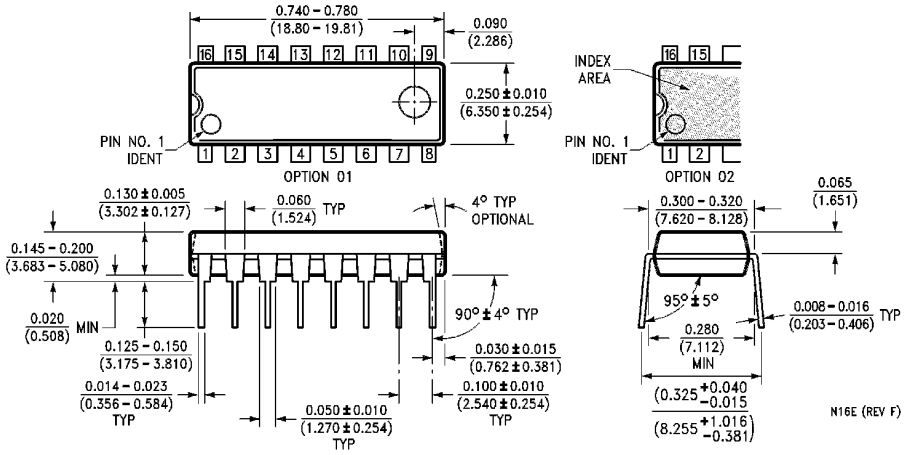
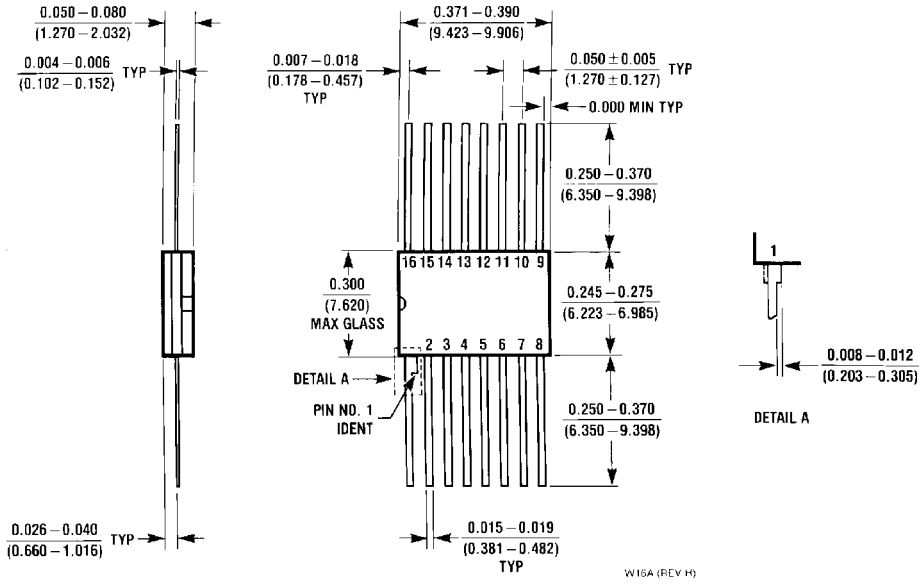
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead (0.300" Wide) Molded Dual-In-Line Package (P)
NS Package Number N16E



16-Lead Ceramic Flatpak (F)
NS Package Number W16A

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