

# DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

## HEF4016B

### gates

### Quadruple bilateral switches

Product specification  
File under Integrated Circuits, IC04

January 1995

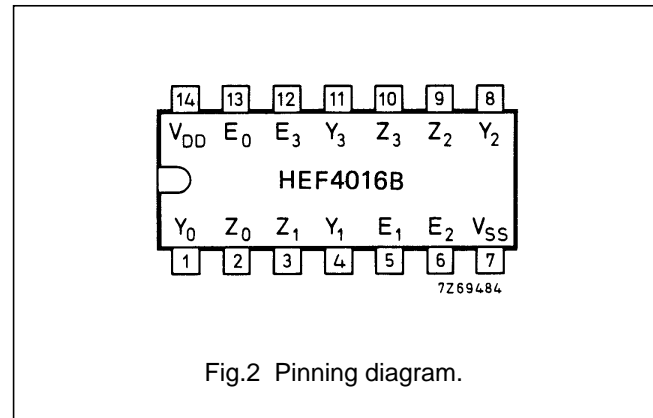
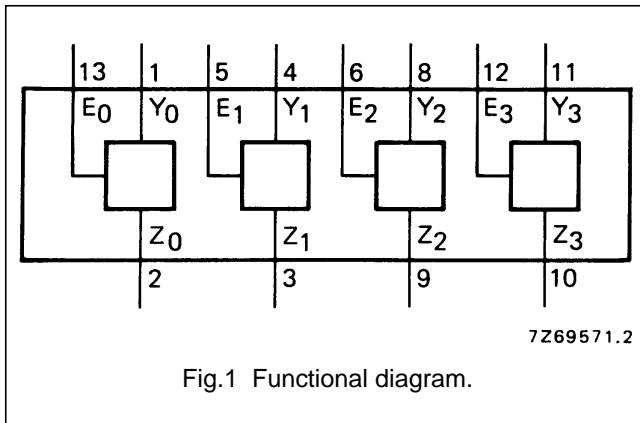
# Quadruple bilateral switches

# HEF4016B gates

### DESCRIPTION

The HEF4016B has four independent analogue switches (transmission gates). Each switch has two input/output terminals (Y/Z) and an active HIGH enable input (E). When E is connected to  $V_{DD}$  a low impedance bidirectional path between Y and Z is established (ON condition). When E is connected to  $V_{SS}$  the switch is disabled and a high

impedance between Y and Z is established (OFF condition). Current through a switch will not cause additional  $V_{DD}$  current provided the voltage at the terminals of the switch is maintained within the supply voltage range;  $V_{DD} \geq (V_Y, V_Z) \geq V_{SS}$ . Inputs Y and Z are electrically equivalent terminals.



### PINNING

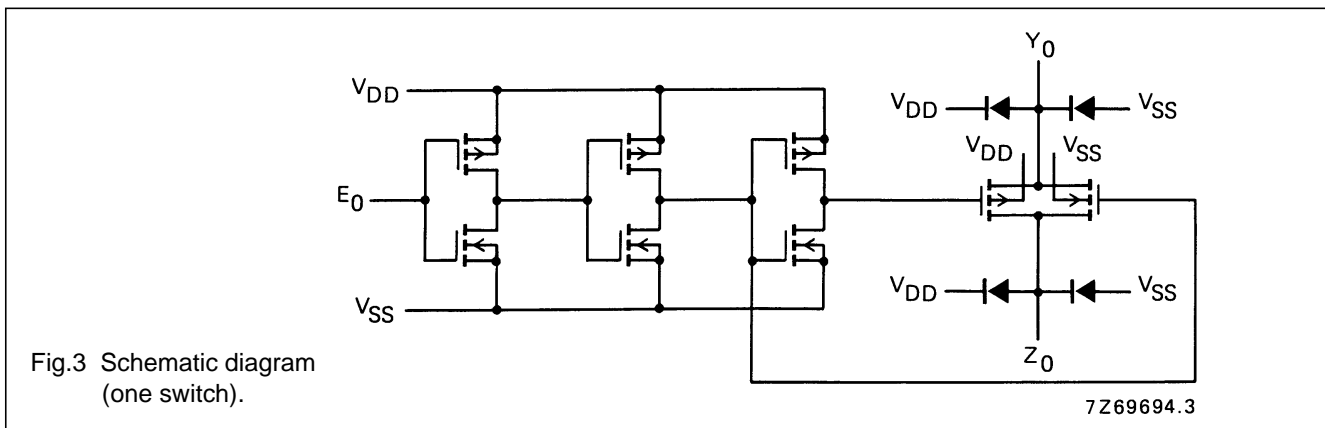
- $E_0$  to  $E_3$  enable inputs
- $Y_0$  to  $Y_3$  input/output terminals
- $Z_0$  to  $Z_3$  input/output terminals

- HEF4016BP(N): 14-lead DIL; plastic (SOT27-1)
- HEF4016BD(F): 14-lead DIL; ceramic (cerdip) (SOT73)
- HEF4016BT(D): 14-lead SO; plastic (SOT108-1)
- ( ) : Package Designator North America

### APPLICATION INFORMATION

Some examples of applications for the HEF4016B are:

- Signal gating
- Modulation
- Demodulation
- Chopper



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## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Power dissipation per switch P max. 100 mW

For other RATINGS see Family Specifications

## DC CHARACTERISTICS

$T_{amb} = 25\text{ °C}$ ;  $V_{SS} = 0\text{ V}$  (unless otherwise specified)

PARAMETER	$V_{DD}$ V	SYMBOL	TYP.	MAX.	UNIT	CONDITIONS
ON resistance	5	$R_{ON}$	8000	–	$\Omega$	$E_n$ at $V_{IH}$ ; $V_{is} = 0$ to $V_{DD}$ ; see Fig.4
	10		230	690	$\Omega$	
	15		115	350	$\Omega$	
ON resistance	5	$R_{ON}$	140	425	$\Omega$	$E_n$ at $V_{IH}$ ; $V_{is} = V_{SS}$ ; see Fig.4
	10		65	195	$\Omega$	
	15		50	145	$\Omega$	
ON resistance	5	$R_{ON}$	170	515	$\Omega$	$E_n$ at $V_{IH}$ ; $V_{is} = V_{DD}$ ; see Fig.4
	10		95	285	$\Omega$	
	15		75	220	$\Omega$	
' $\Delta$ ' ON resistance between any two channels	5	$\Delta R_{ON}$	200	–	$\Omega$	$E_n$ at $V_{IH}$ ; $V_{is} = 0$ to $V_{DD}$ ; see Fig.4
	10		15	–	$\Omega$	
	15		10	–	$\Omega$	

PARAMETER	$V_{DD}$ V	SYMBOL	$T_{amb}$ (°C)						UNIT	CONDITION
			–40		+ 25		+ 85			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Quiescent device current	5	$I_{DD}$	–	1,0	–	1,0	–	7,5	$\mu\text{A}$	$V_{SS} = 0$ ; all valid input combinations; $V_I = V_{SS}$ or $V_{DD}$
	10		–	2,0	–	2,0	–	15,0	$\mu\text{A}$	
	15		–	4,0	–	4,0	–	30,0	$\mu\text{A}$	
Input leakage current at $E_n$	15	$\pm I_{IN}$	–	–	–	300	–	1000	nA	$E_n$ at $V_{SS}$ or $V_{DD}$
OFF-state leakage current, any channel OFF	5	$I_{OZ}$	–	–	–	–	–	–	nA	$E_n$ at $V_{IL}$ ; $V_{is} = V_{SS}$ or $V_{DD}$ ; $V_{os} = V_{DD}$ or $V_{SS}$
	10		–	–	–	–	–	–	nA	
	15		–	–	–	200	–	–	nA	
$E_n$ input voltage LOW	5	$V_{IL}$	–	1,5	–	1,5	–	1,5	V	switch OFF; see Fig.9 for $I_{OZ}$
	10		–	3,0	–	3,0	–	3,0	V	
	15		–	4,0	–	4,0	–	4,0	V	
$E_n$ input voltage HIGH	5	$V_{IH}$	3,5	–	3,5	–	3,5	–	V	low-impedance between Y and Z (ON condition) see $R_{ON}$ switch
	10		7,0	–	7,0	–	7,0	–	V	
	15		11,0	–	11,0	–	11,0	–	V	

Quadruple bilateral switches

HEF4016B  
gates

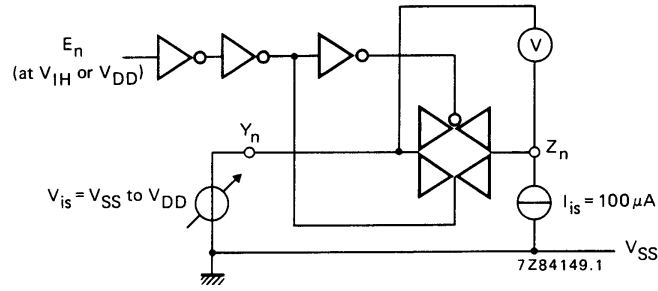
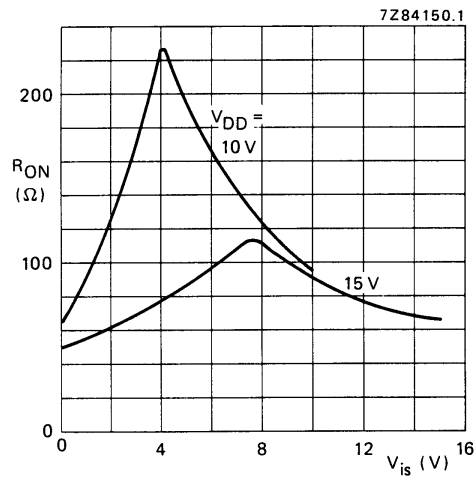


Fig.4 Test set-up for measuring  $R_{ON}$ .



$E_n > V_{IH}$   
 $I_{is} = 100 \mu A$   
 $V_{SS} = 0 V$

Fig.5 Typical  $R_{ON}$  as a function of input voltage.

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## AC CHARACTERISTICS

$V_{SS} = 0$  V;  $T_{amb} = 25$  °C; input transition times  $\leq 20$  ns

	$V_{DD}$ V	SYMBOL	TYP.	MAX.		
Propagation delays $V_{is} \rightarrow V_{os}$ HIGH to LOW	5		25	50	ns	note 1
	10	$t_{PHL}$	10	20	ns	
	15		5	10	ns	
LOW to HIGH	5		20	40	ns	note 1
	10	$t_{PLH}$	10	20	ns	
	15		5	10	ns	
Output disable times $E_n \rightarrow V_{os}$ HIGH	5		90	130	ns	note 2
	10	$t_{PHZ}$	80	110	ns	
	15		75	100	ns	
LOW	5		85	120	ns	note 2
	10	$t_{PLZ}$	75	100	ns	
	15		75	100	ns	
Output enable times $E_n \rightarrow V_{os}$ HIGH	5		40	80	ns	note 2
	10	$t_{PZH}$	20	40	ns	
	15		15	30	ns	
LOW	5		40	80	ns	note 2
	10	$t_{PZL}$	20	40	ns	
	15		15	30	ns	
Distortion, sine-wave response	5		–	–	%	note 3
	10		0,08	–	%	
	15		0,04	–	%	
Crosstalk between any two channels	5		–	–	MHz	note 4
	10		1	–	MHz	
	15		–	–	MHz	
Crosstalk; enable input to output	5		–	–	mV	note 5
	10		50	–	mV	
	15		–	–	mV	
OFF-state feed-through	5		–	–	MHz	note 6
	10		1	–	MHz	
	15		–	–	MHz	
ON-state frequency response	5		–	–	MHz	note 7
	10		90	–	MHz	
	15		–	–	MHz	

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## HEF4016B gates

### Notes

$V_{is}$  is the input voltage at a Y or Z terminal, whichever is assigned as input.

$V_{os}$  is the output voltage at a Y or Z terminal, whichever is assigned as output.

- $R_L = 10 \text{ k}\Omega$  to  $V_{SS}$ ;  $C_L = 50 \text{ pF}$  to  $V_{SS}$ ;  $E_n = V_{DD}$ ;  $V_{is} = V_{DD}$  (square-wave); see Figs 6 and 10.
- $R_L = 10 \text{ k}\Omega$ ;  $C_L = 50 \text{ pF}$  to  $V_{SS}$ ;  $E_n = V_{DD}$  (square-wave);  
 $V_{is} = V_{DD}$  and  $R_L$  to  $V_{SS}$  for  $t_{PHZ}$  and  $t_{PZH}$ ;  
 $V_{is} = V_{SS}$  and  $R_L$  to  $V_{DD}$  for  $t_{PLZ}$  and  $t_{PZL}$ ; see Figs 6 and 11.
- $R_L = 10 \text{ k}\Omega$ ;  $C_L = 15 \text{ pF}$ ;  $E_n = V_{DD}$ ;  $V_{is} = \frac{1}{2}V_{DD(p-p)}$  (sine-wave, symmetrical about  $\frac{1}{2}V_{DD}$ );  
 $f_{is} = 1 \text{ kHz}$ ; see Fig. 7.
- $R_L = 1 \text{ k}\Omega$ ;  $V_{is} = \frac{1}{2}V_{DD(p-p)}$  (sine-wave, symmetrical about  $\frac{1}{2}V_{DD}$ );

$$20 \log \frac{V_{os} (B)}{V_{is} (A)} = -50 \text{ dB}; E_n (A) = V_{SS}; E_n (B) = V_{DD}; \text{ see Fig. 8.}$$

- $R_L = 10 \text{ k}\Omega$  to  $V_{SS}$ ;  $C_L = 15 \text{ pF}$  to  $V_{SS}$ ;  $E_n = V_{DD}$  (square-wave); crosstalk is  $|V_{os}|$  (peak value); see Fig. 6.
- $R_L = 1 \text{ k}\Omega$ ;  $C_L = 5 \text{ pF}$ ;  $E_n = V_{SS}$ ;  $V_{is} = \frac{1}{2}V_{DD(p-p)}$  (sine-wave, symmetrical about  $\frac{1}{2}V_{DD}$ );

$$20 \log \frac{V_{os}}{V_{is}} = -50 \text{ dB}; \text{ see Fig. 7.}$$

- $R_L = 1 \text{ k}\Omega$ ;  $C_L = 5 \text{ pF}$ ;  $E_n = V_{DD}$ ;  $V_{is} = \frac{1}{2}V_{DD(p-p)}$  (sine-wave, symmetrical about  $\frac{1}{2}V_{DD}$ );

$$20 \log \frac{V_{os}}{V_{is}} = -3 \text{ dB}; \text{ see Fig. 7.}$$

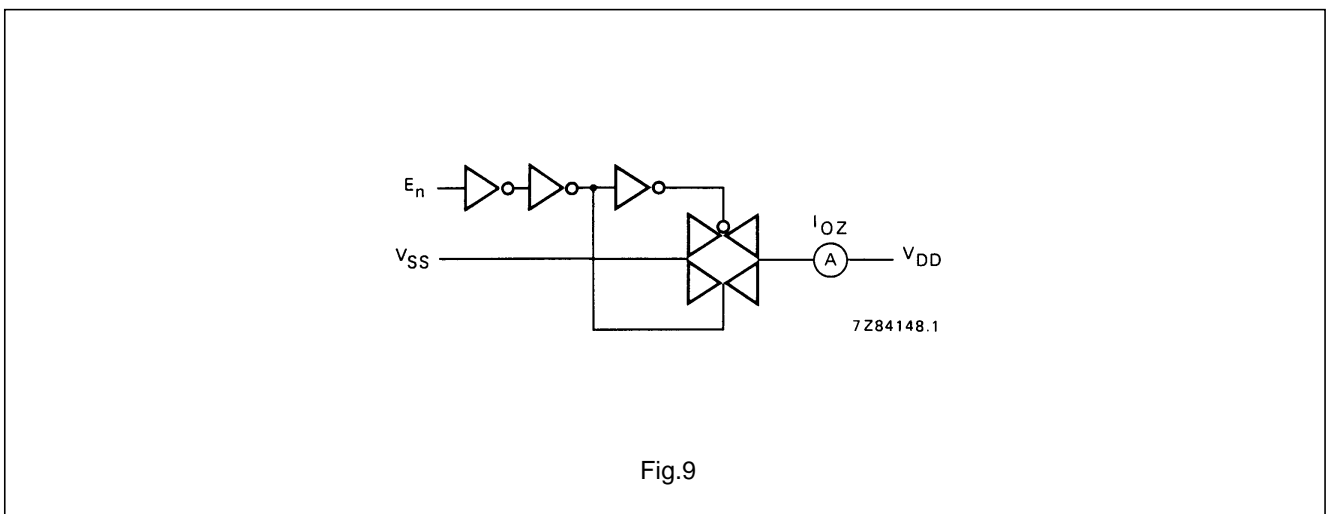
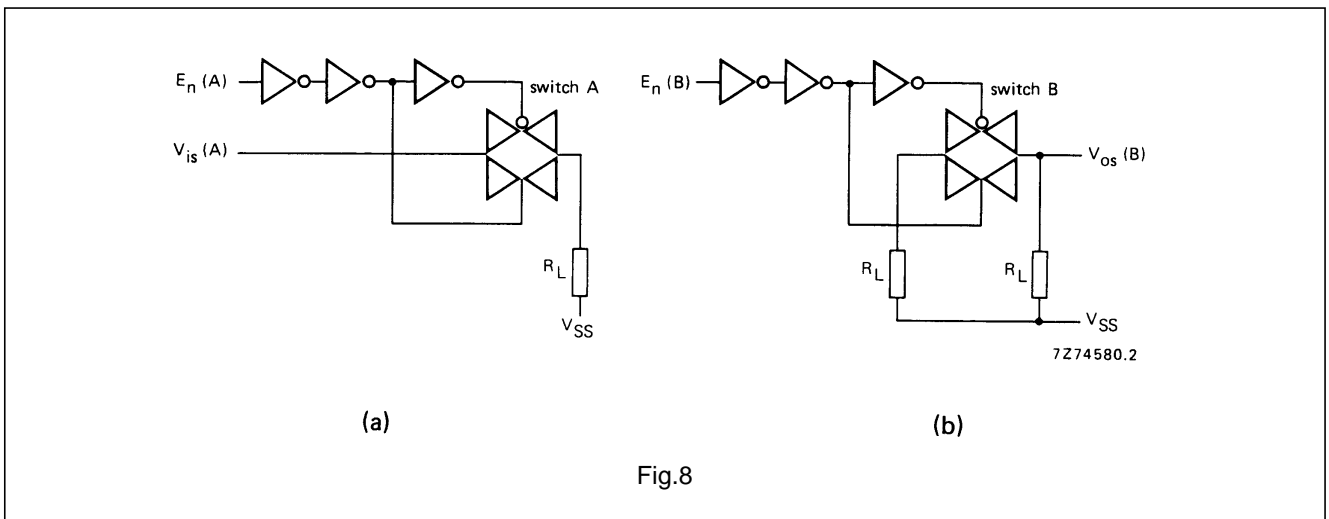
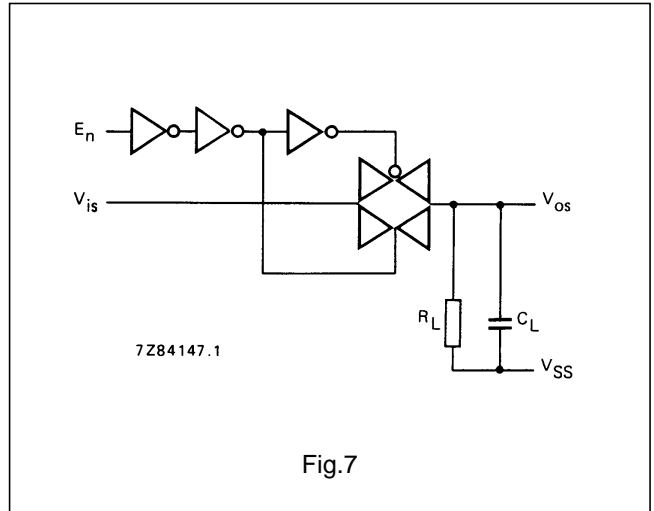
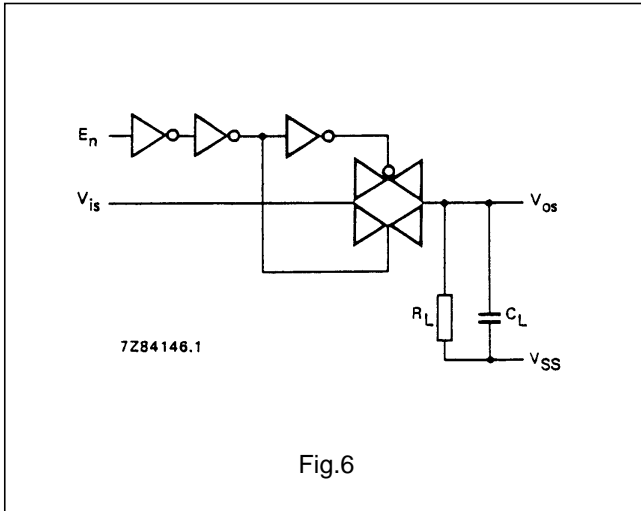
	$V_{DD}$ V	TYPICAL FORMULA FOR P ( $\mu$ W)	
Dynamic power dissipation per package (P) <sup>(1)</sup>	5 10 15	$550 f_i + \sum (f_o C_L) \times V_{DD}^2$ $2\ 600 f_i + \sum (f_o C_L) \times V_{DD}^2$ $6\ 500 f_i + \sum (f_o C_L) \times V_{DD}^2$	where $f_i$ = input freq. (MHz) $f_o$ = output freq. (MHz) $C_L$ = load capacitance (pF) $\sum (f_o C_L)$ = sum of outputs $V_{DD}$ = supply voltage (V)

### Note

- All enable inputs switching.

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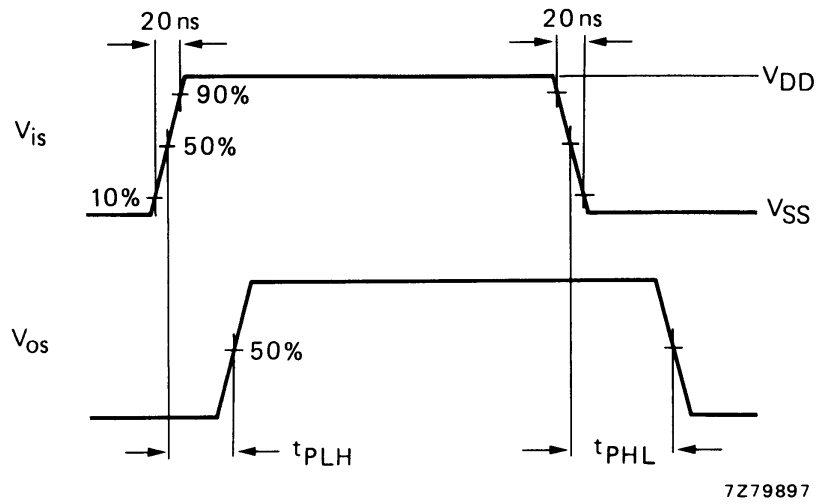
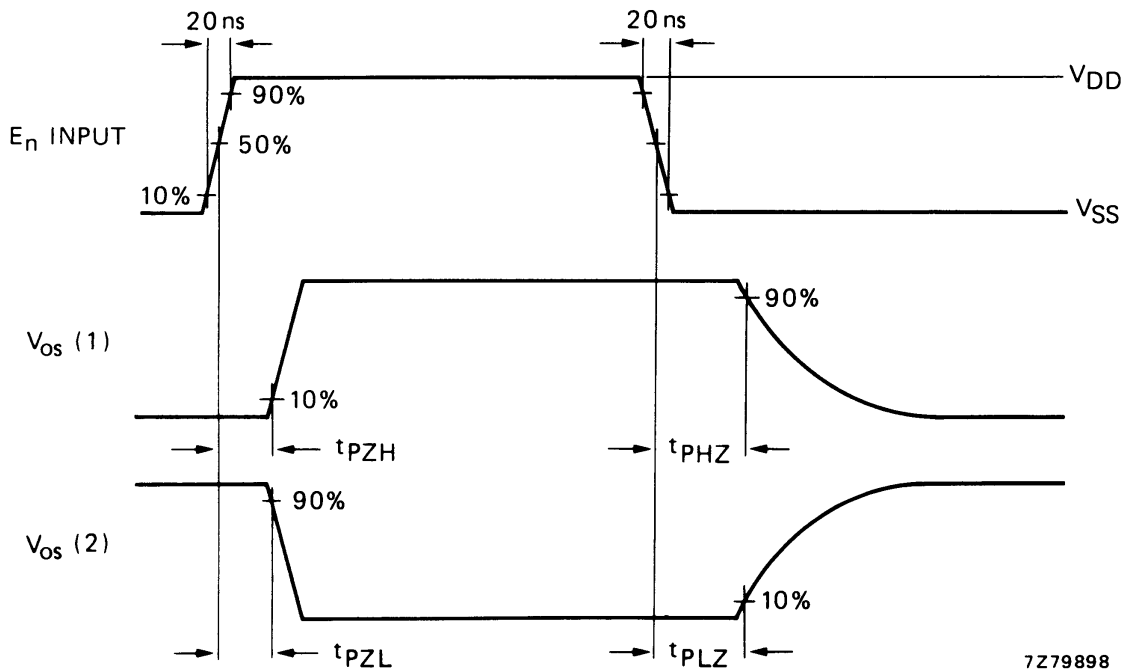


Fig.10 Waveforms showing propagation delays from  $V_{is}$  to  $V_{os}$ .



- (1)  $V_{is}$  at  $V_{DD}$
- (2)  $V_{is}$  at  $V_{SS}$

Fig.11 Waveforms showing output disable and enable times.