FAST CMOS OCTAL BIDIRECTIONAL TRANSCEIVER

IDT54/74FCT245/A/C

FEATURES:

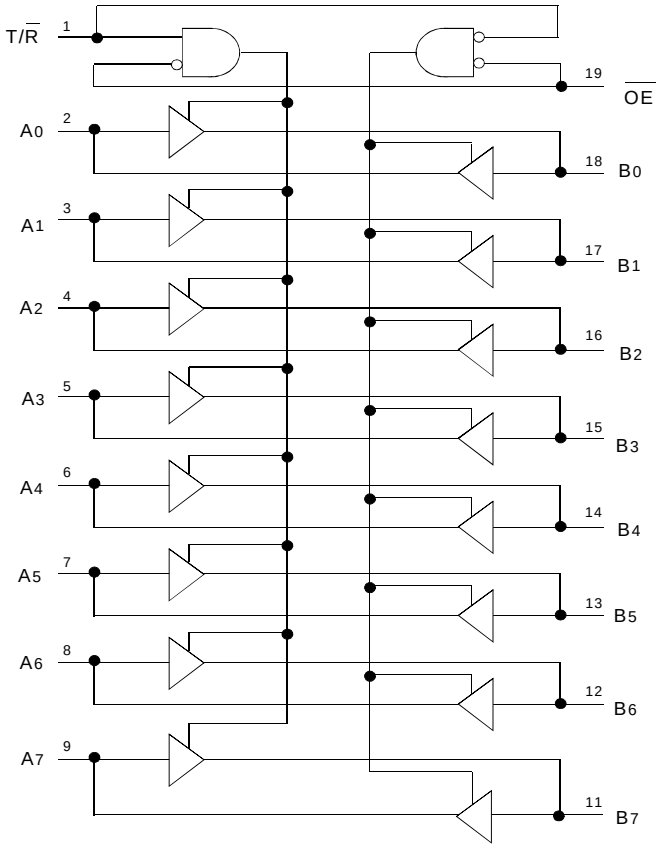
- IDT54/74FCT245 equivalent to FAST™ speed
- IDT54/74FCT245A 25% faster than FAST
- IDT54/74FCT245C 40% faster than FAST
- TTL input and output level compatible
- CMOS output level compatible
- I_{OL} = 64mA (commercial) and 48mA (military)
- Input current levels only 5µA max.
- CMOS power levels (2.5mW typ. static)
- Direction control and over-riding 3-state control
- Military product compliant to MIL-STD-883, Class B and DESC listed
- Meets or exceeds JEDEC Standard 18 specifications
- Available in the following packages:
  - Commercial: SOIC
  - Military: CERDIP, LCC, CERPACK

DESCRIPTION:

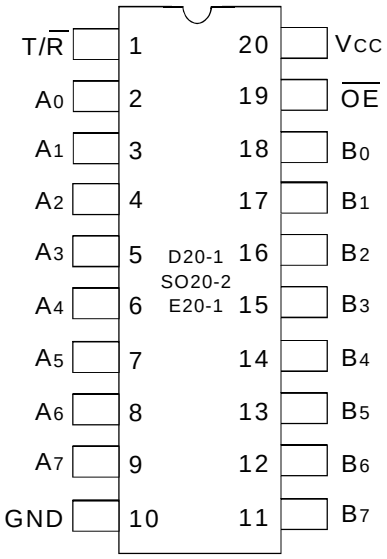
The IDT octal bidirectional transceivers are built using an advanced dual metal CMOS technology. The FCT245 is designed for asynchronous two-way communication between data buses. The transmit/receive ($T/\overline{R}$) input determines the direction of data flow through the bidirectional transceiver. Transmit (active high) enables data from A ports to B ports, and receive (active low) from B ports to A ports. The output enable ($\overline{OE}$) input, when high, disables both A and B ports by placing them in High-Z condition.

The FCT245 transceivers have non-inverting outputs.

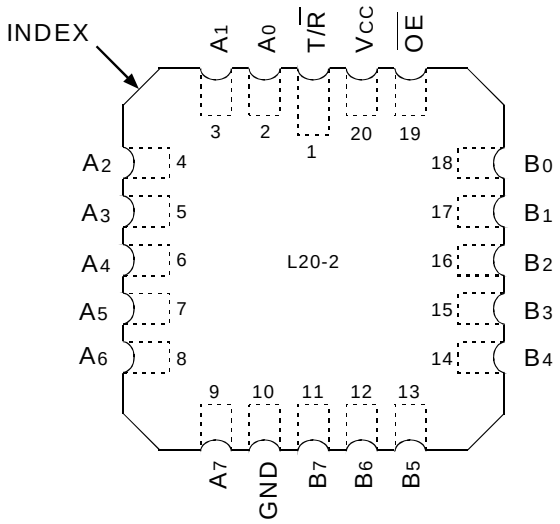
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



DIP/ SOIC/ CERPACK
TOP VIEW



LCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7	–0.5 to +7	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

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NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}$	Output Enable Input (Active LOW)
T/$\overline{R}$	Transmit/Receive Input
A_0-A_7	Side A Inputs or 3-State Outputs
B_0-B_7	Side B Inputs or 3-State Outputs

FUNCTION TABLE (1)

Inputs		Outputs
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

NOTE:

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	—	—	5	µA
	(Except I/O pins)		V_I = 2.7V	—	—	5[4]	
I_{IL}	Input LOW Current		V_I = 0.5V	—	—	–5[4]	
	(Except I/O pins)		V_I = GND	—	—	–5	
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	—	—	15	µA
	(I/O pins only)		V_I = 2.7V	—	—	15[4]	
I_{IL}	Input LOW Current		V_I = 0.5V	—	—	–15[4]	
	(I/O pins only)		V_I = GND	—	—	–15	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min.	I_{OH} = –300µA	V_{HC}	V_{CC}	—	
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL.	2.4	4.3	—	
			I_{OH} = –15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
	(Port A and Port B)	V_{CC} = Min.	I_{OL} = 300µA	—	GND	V_{LC}[4]	
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL.	—	0.3	0.55	
			I_{OL} = 64mA COM'L.	—	0.3	0.55	

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.5	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND T/$\overline{R}$ = GND or V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/MHz
I_C	Total Power Supply Current [6]	V_{CC} = Max. Outputs Open fi = 10MHz	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	2	4	mA
		50% Duty Cycle T/$\overline{R}$ = $\overline{OE}$ = GND One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	2.3	5	
		V_{CC} = Max. Outputs Open fi = 2.5MHz	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	3.5	6.5[5]	
		50% Duty Cycle T/$\overline{R}$ = $\overline{OE}$ = GND Eight Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	5.5	14.5[5]	

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

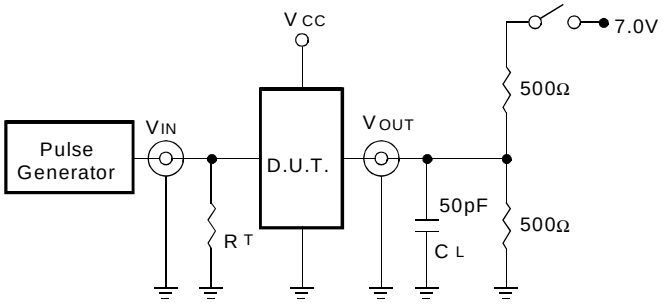
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	54/74FCT245				54/74FCT245A				54/74FCT245C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay A to B, B to A	C_L = 50 pF R_L = 500Ω	1.5	7	1.5	7.5	1.5	4.6	1.5	4.9	1.5	4.1	1.5	4.5	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to A or B		1.5	9.5	1.5	10	1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.2	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to A or B		1.5	7.5	1.5	10	1.5	5	1.5	6	1.5	4.8	1.5	5.2	ns
t_{PZH} t_{PZL}	Output Enable Time T/$\overline{R}$ to A or B[3]		1.5	9.5	1.5	10	1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.2	ns
t_{PHZ} t_{PLZ}	Output Disable Time T/$\overline{R}$ to A or B[3]		1.5	7.5	1.5	10	1.5	5	1.5	6	1.5	4.8	1.5	5.2	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



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SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

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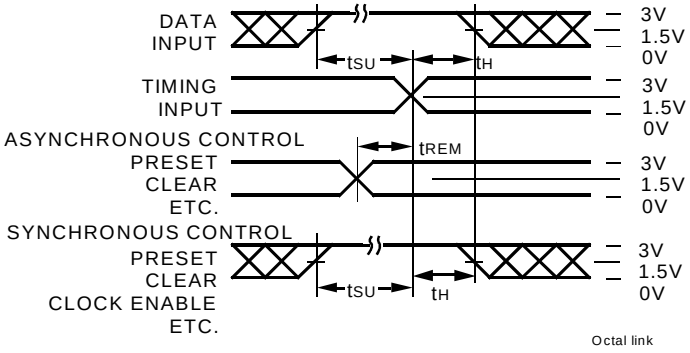
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD, AND RELEASE TIMES



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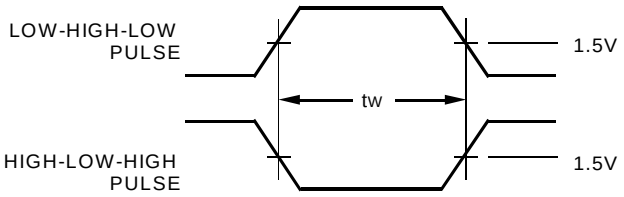
PULSE WIDTH



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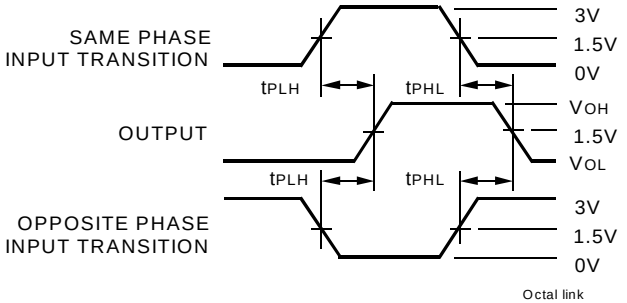
PROPAGATION DELAY



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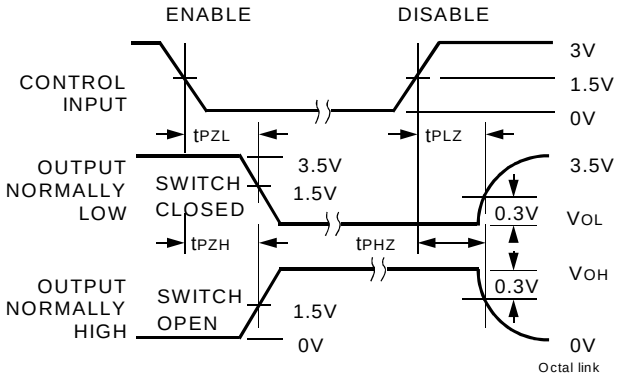
ENABLE AND DISABLE TIMES



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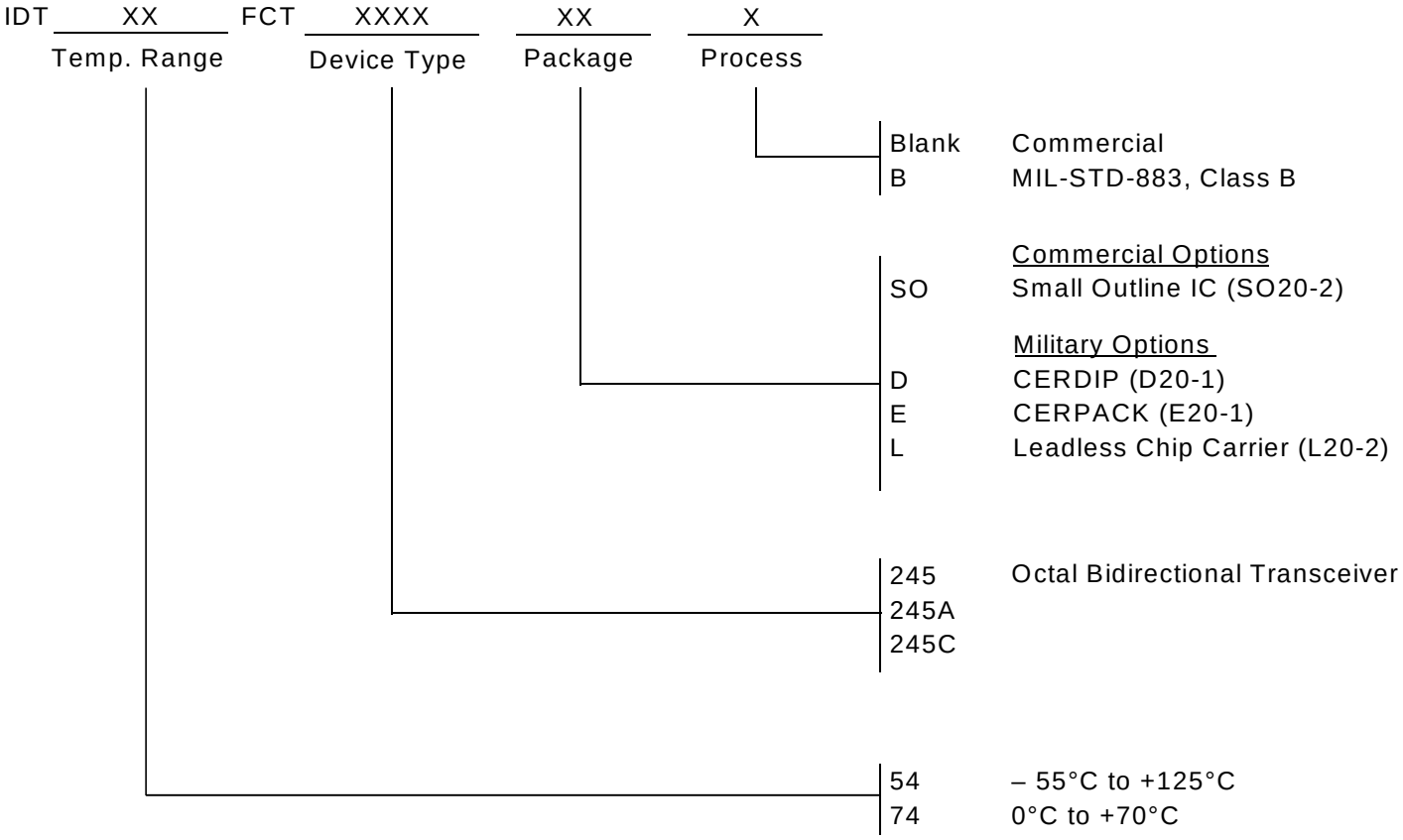
NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

ORDERING INFORMATION



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