REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add logic diagram. Correct the parameters in waveforms, figure 4. Update boilerplate to MIL-PRF-38535 requirements. Editorial changes throughout. - jak	04-01-15	Thomas M. Hess

REV																				
SHEET																				
REV																				
SHEET																				

REV STATUS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A	
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	

PMIC N/A

PREPARED BY
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DEFENSE SUPPLY CENTER COLUMBUS

COLUMBUS, OHIO 43216
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Ray Monnin

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
88-11-10

MICROCIRCUIT, DIGITAL, FAST CMOS, 9-BIT NONINVERTING REGISTER, TTL COMPATIBLE INPUTS, MONOLITHIC SILICON

REVISION LEVEL	SIZE	CAGE CODE	
A	**A**	**67268**	**5962-88656**

SHEET 1 OF 13

DSCC FORM 2233
APR 97

5962-E076-04

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-88656	01	K	A
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54FCT823A	9-bit non-inverting register with clock enable and clear, TTL compatible inputs
02	54FCT823B	9-bit non-inverting register with clock enable and clear, TTL compatible inputs

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
K	GDFP2-F24 or CDFP3-F24	24	Flat pack
L	GDFP3-T24 or CDIP4-T24	24	Dual-in-line package
3	CQCC1-N28	28	Square chip carrier package

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings. 1/

Supply voltage range ..... -0.5 V dc to +6.0 V dc
Input voltage range ..... -0.5 V dc to V_{CC} + 0.5 V dc
Output voltage range ..... -0.5 V dc to V_{CC} + 0.5 V dc
DC input diode current (I_{IK}) ..... -20 mA
DC output diode current (I_{OK}) ..... -50 mA
DC output current ..... ±100 mA
Maximum power dissipation (P_D) 2/ ..... 500 mW
Thermal resistance, junction-to-case (θ_{JC}) ..... See MIL-STD-1835
Storage temperature range ..... -65°C to +150°C
Junction temperature (T_J) ..... +175°C
Lead temperature (soldering, 10 seconds) ..... +300°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}) ..... +4.5 V dc to +5.5 V dc
Maximum low level input voltage (V_{IL}) ..... 0.8 V dc
Minimum high level input voltage (V_{IH}) ..... 2.0 V dc
Case operating temperature range (T_C) ..... -55°C to +125°C

1/ All voltages referenced to GND.
2/ Must withstand the added P_D due to short circuit test, e.g.; I_{OS}.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 5.0 V dc ±10% unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
High level output voltage	V_{OH}	V_{CC} = 4.5 V V_{IL} = 0.8 V V_{IH} = 2.0 V	I_{OH} = -300 µA	1, 2, 3	All	4.3		V
			I_{OH} = -15 mA	1, 2, 3	All	2.4		
Low level output voltage	V_{OL}	V_{CC} = 4.5 V V_{IL} = 0.8 V V_{IH} = 2.0 V	I_{OL} = 300 µA	1, 2, 3	All		0.2	V
			I_{OL} = 32 mA	1, 2, 3	All		0.5	
Input clamp voltage	V_{IK}	V_{CC} = 4.5 V, I_{IN} = -18 mA		1	All		-1.2	V
High level input current	I_{IH}	V_{CC} = 5.5 V, V_{IN} = 5.5 V		1, 2, 3	All		5.0	µA
Low level input current	I_{IL}	V_{CC} = 5.5 V, V_{IN} = GND		1, 2, 3	All		-5.0	µA
High impedance current, output high	I_{OZH}	V_{CC} = 5.5 V, V_{IN} = 5.5 V		1, 2, 3	All		10.0	µA
High impedance current, output low	I_{OZL}	V_{CC} = 5.5 V, V_{IN} = GND		1, 2, 3	All		-10.0	µA
Short circuit output current	I_{OS}	V_{CC} = 5.5 V 1/		1, 2, 3	All	-75		mA
Quiescent power supply current (CMOS inputs)	I_{CCQ}	$V_{IN} \le 0.2$ V or $V_{IN} \ge 5.3$ V V_{CC} = 5.5 V f_i = 0 MHz		1, 2, 3	All		1.5	mA
Quiescent power supply current (TTL inputs)	ΔI_{CC}	V_{CC} = 5.5 V V_{IN} = 3.4 V 2/		1, 2, 3	All		2.0	mA
Dynamic power supply current	I_{CCD}	V_{CC} = 5.5 V, $\overline{OE}$ = GND $V_{IN} \ge 5.3$ V or $V_{IN} \le 0.2$ V Outputs open, One bit toggling 50% duty cycle		3/	All		0.25	mA/ MHz
Total power supply current	I_{CC} 4/	$V_{IN} \ge 5.3$ V or $V_{IN} \le 0.2$ V V_{CC} = 5.5 V, f_i = 10 MHz $\overline{OE}$ = GND Outputs open One bit toggling, 50% duty cycle		1, 2, 3	All		4.0	mA
		V_{IN} = 3.4 V or V_{IN} = GND V_{CC} = 5.5 V, f_i = 10 MHz $\overline{OE}$ = GND Outputs open One bit toggling, 50% duty cycle		1, 2, 3	All		6.0	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 5.0 V dc ±10% unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Input capacitance	C_{IN}	See 4.3.1c		4	All		10	pF
Output capacitance	C_{OUT}	See 4.3.1c		4	All		12	pF
Functional tests		See 4.3.1d		7, 8	All			
Propagation delay time, CP to Yn	t_{PLH1}, t_{PHL1}	R_L = 500Ω See figure 4 OE = low	C_L = 50 pF	9, 10, 11	01		12.0	ns
					02		8.5	
			C_L = 300 pF 5/	9, 10, 11	01		20.0	ns
					02		16	
Propagation delay time , output enable, $\overline{OE}$ to Yn	t_{PZH}, t_{PZL}	R_L = 500Ω See figure 4	C_L = 50 pF	9, 10, 11	01		15.0	ns
					02		9.0	
			C_L = 300 pF 5/	9, 10, 11	01		25.0	ns
					02		16.0	
Propagation delay time, output disable, $\overline{OE}$ to Yn	t_{PHZ}, t_{PLZ}	R_L = 500Ω See figure 4	C_L = 50 pF	9, 10, 11	01		18.0	ns
					02		8.0	
			C_L = 5.0 pF 5/	9, 10, 11	01		10.0	ns
					02		7.0	
Propagation delay time, CLR to Yn	t_{PHL2}	C_L = 50 pF R_L = 500Ω See figure 4		9, 10, 11	01		20.0	ns
					02		9.5	
Dn to CP setup time	t_{s1}			9, 10, 11	01	4.0		ns
					02	3.0		
Dn to CP hold time	t_{h1}			9, 10, 11	01	2.0		ns
					02	1.5		
$\overline{OE}$ (low-to-high) to CP setup time	t_{s2}			9, 10, 11	01	4.0		ns
					02	3.0		
$\overline{OE}$ to CP hold time	t_{h2}			9, 10, 11	01	2.0		ns
					02	0.0		
$\overline{CLR}$ recovery time (low-to-high)	t_{s3}			9, 10, 11	01	7.0		ns
					02	6.0		
CP pulse width	t_{w1}			9, 10, 11	01	7.0		ns
					02	6.0		
$\overline{CLR}$ pulse width, ($\overline{CLR}$ = low)	t_{w2}			9, 10, 11	01	7.0		ns
					02	6.0		

1/ Not more than one output should be shorted at one time, and the duration of the short circuit condition should not exceed one second.

2/ TTL driven input (V_{IN} = 3.4 V); all other inputs at V_{CC} or GND.

3/ This parameter is not directly testable, but is derived for use in total power supply calculations.

4/ $I_{CC} = I_{CCQ} + (\Delta I_{CC} \times D_H \times N_T) + (I_{CCD} (f_I \times N_I + f_{CP}/2))$
Where: D_H = Duty cycle for TTL inputs high.
N_T = Number of TTL inputs at D_H.
f_I = Input frequency in MHz.
N_I = Number of inputs at f_I.
f_{CP} = clock frequency in MHz

5/ This parameter is guaranteed, if not tested, to the specified limits.

Device types	01 and 02	
Case outlines	K and L	3
Terminal number	Terminal symbol	
1	$\overline{OE}$	NC
2	D0	$\overline{OE}$
3	D1	D0
4	D2	D1
5	D3	D2
6	D4	D3
7	D5	D4
8	D6	NC
9	D7	D5
10	D8	D6
11	$\overline{CLR}$	D7
12	GND	D8
13	$\overline{CP}$	$\overline{CLR}$
14	$\overline{EN}$	GND
15	Y8	NC
16	Y7	$\overline{CP}$
17	Y6	$\overline{EN}$
18	Y5	Y8
19	Y4	Y7
20	Y3	Y6
21	Y2	Y5
22	Y1	NC
23	Y0	Y4
24	V_{CC}	Y3
25	- - -	Y2
26	- - -	Y1
27	- - -	Y0
28	- - -	V_{CC}

NC = No connection.

Terminal description	
Symbol	Description
Dn (n = 0 to 8)	Data inputs
$\overline{CLR}$	Clear input. For both inverting and noninverting registers, when the clear input is low and $\overline{OE}$ is low, the Qn outputs on the flip-flop are low. When the clear input is high, data can be entered into the register.
CP	Clock pulse for the register; enters data into the register on the low-to-high transition.
Yn (n = 0 to 8)	Register output
$\overline{EN}$	Clock enable. When the clock enable is low, data on the Dn input is transferred to the Qn output of the flip-flop on the low-to-high transition of the clock. When the clock enable is high, the Qn outputs do not change state regardless of the data or clock input transitions.
$\overline{OE}$	Output enable control input. When the $\overline{OE}$ input is high, the Yn outputs are in the high impedance state. When the $\overline{OE}$ input is low, the true regisiter data is present at the Yn outputs.
Qn (n = 0 to 8)	Internal outputs of the flip-flop.

FIGURE 1. Terminal connections.

Inputs					Internal outputs	Outputs	Function
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	Dn	CP	Qn	Yn	
H	X	L	L	↑	L	Z	High Z
H	X	L	H	↑	H	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	H	X	NC	Z	Hold
L	H	H	H	X	NC	NC	
H	H	L	L	↑	L	Z	Load
H	H	L	H	↑	H	Z	
L	H	L	L	↑	L	L	
L	H	L	H	↑	H	H	

L = Low voltage level
H = High voltage level
X = Irrelevant
NC = No change
Z = High impedance state
↑ = Low-to-high transition

FIGURE 2. Truth table.

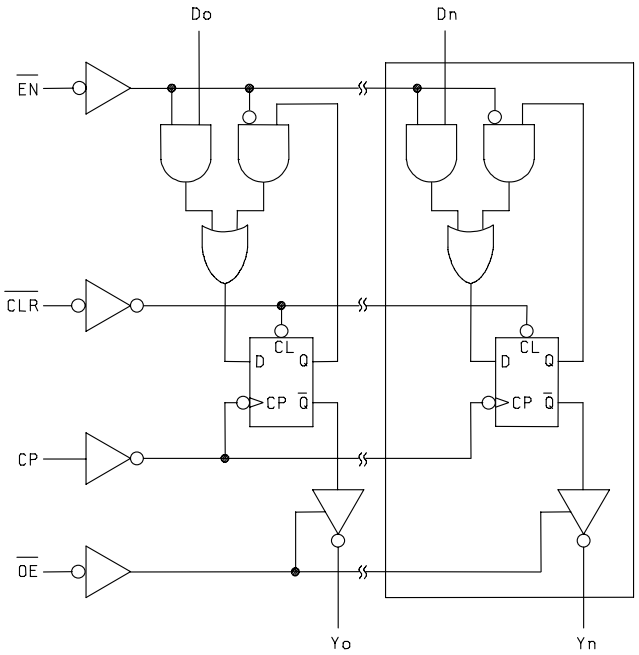


FIGURE 3. Logic diagram.

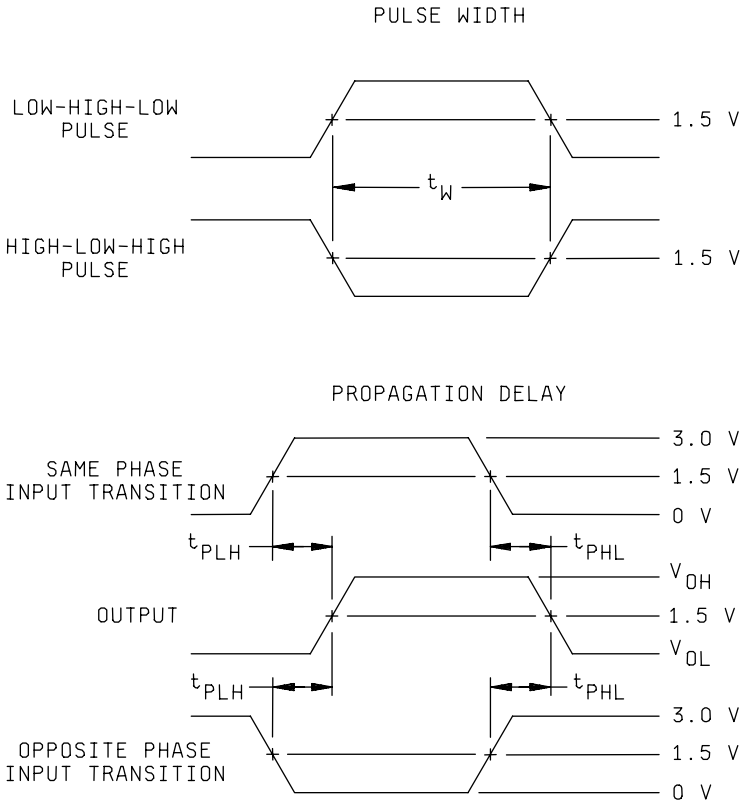
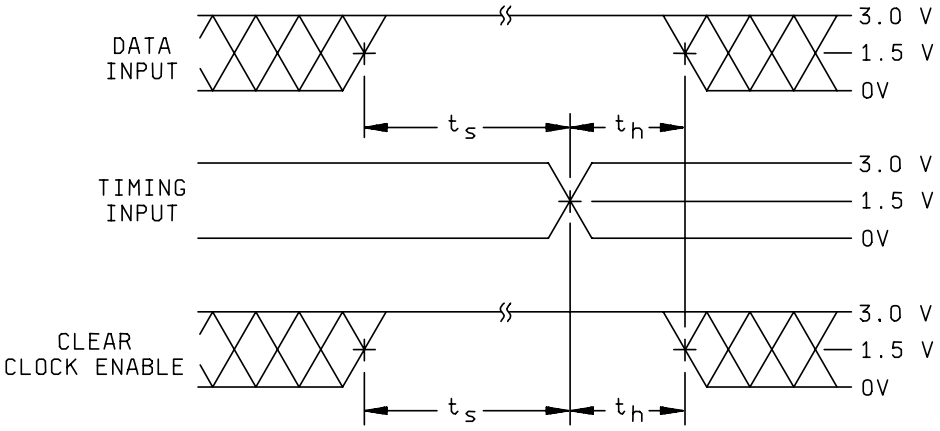
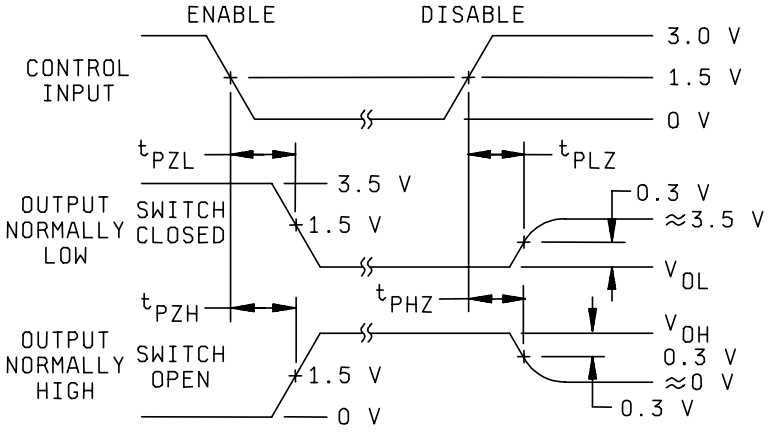


FIGURE 4. Switching waveforms and test circuit.

SETUP AND HOLD TIMES

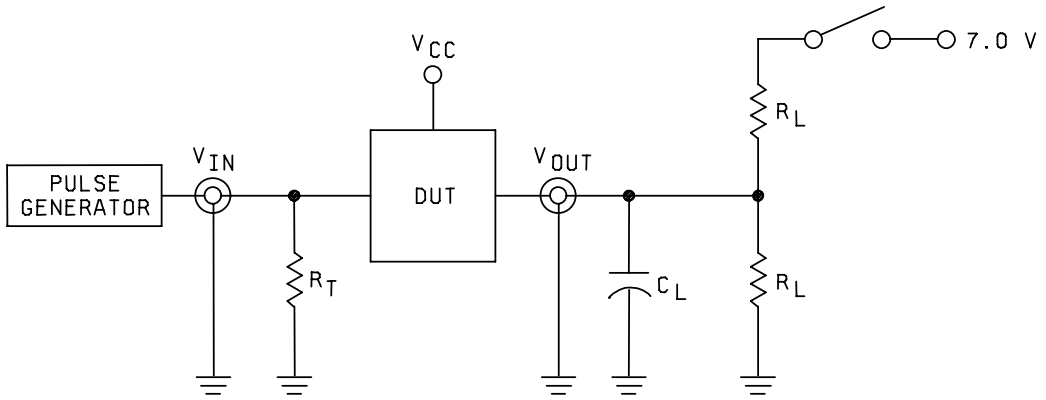


ENABLE AND DISABLE TIMES



NOTES:
1. Diagram shown for input control enable – low and input control disable – high.
2. Pulse generator for all pulses: $t_f \leq 2.5$ ns, $t_r \leq 2.5$ ns.

FIGURE 4. Switching waveforms and test circuit – Continued.



Test	Switch
t_{PLZ}	Closed
t_{PZL}	Closed
All other	Open

NOTES:
1/ $R_L = 500\Omega$.
2/ Load capacitance includes jig and probe capacitance. See characteristics in table I for values.
3/ R_T = Termination should be equal to Z_{OUT} of pulse generators.

FIGURE 4. Switching waveforms and test circuit - Continued.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	----
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect input capacitance. Test all applicable pins on five devices with zero failures.

d. Subgroups 7 and 8 shall include verification of the truth table as specified on figure 2 herein.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 04-01-15

Approved sources of supply for SMD 5962-88656 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8865601KA	3/	54FCT823AEB
5962-8865601LA	61772	IDT54FCT823ADB
5962-88656013A	61772	IDT54FCT823ALB
5962-8865602KA	3/	54FCT245BEB
5962-8865602LA	61772	IDT54FCT823BDB
5962-88656023A	61772	IDT54FCT823BLB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
61772	Integrated Device Technology, Inc. 2975 Stender Way Santa Clara, CA 95054