ISOFACE™ 4DIRx4xxHA family

Robust digital isolators with AEC-Q100 qualification

Description

The ISOFACE™ 4DIRx4xxHA quad-channel digital isolator family is AEC-Q100 qualified for automotive applications. It supports data rates up to 40 Mbps and ensures robust data communication over a wide ambient operating temperature range (-40°C to +125°C). Infineon's robust Coreless Transformer (CT) technology provides high immunity against system noise (CMTI of min. 100 kV/µs) and withstands up to 5700 V_{rms} isolation voltage (V_{ISO}). Four data channels in a PG-DSO-16 wide-body 300 mil package allow simplified and high power density designs and improve system efficiency with low power consumption. Product variants with different channel configurations and fail-safe default output states are available.

Features

- AEC-Q100 qualification for Grade 1 (-40°C to +125°C) ambient operating temperature range
- Data rates up to 40 Mbps
- Wide operating supply voltage 2.7 V - 6.5 V
- Low current consumption (max. 1.6 mA/ch @ 1 Mbps, 3.3 V, 15 pF)
- High CMTI of min. 100 kV/µs
- Propagation delay typ 26 ns with 3 ns channel-to-channel mismatch
- Max 3 ns pulse width distortion @ 3.3 V
- Variable CMOS input thresholds with default output high or low options
- RoHS compliant PG-DSO-16 wide-body 300 mil package

Isolation and safety certificates

- UL 1577 (Ed. 5) with V_{ISO} = 5700 V_{rms} (*certification n. E311313*)
- VDE 0884-17 [1] and IEC 60747-17 with V_{IOTM} = 8000 V_{pk}, V_{IORM} = 1767 V_{pk}, V_{IOSM} = 10400 V_{pk} [2]
- EN and CQC certification for IEC 62368-1, IEC 60601-1, IEC 61010-1, GB 4943.1 system standards [2]

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

Potential applications

- Isolated Serial Peripheral Interface (SPI)
- Hybrid, electric and powertrain systems (EV/HEV)
  - On-Board Charger (OBC)
  - Traction inverter
  - DC/DC converter
  - Inverter and motor control

1 IEC 60747-17 and its German equivalent VDE 0884-17
2 Certification planned

ISOFACE™ 4DIRx4xxHA product portfolio

Part number	Channel configuration	Default output state	Output enable	Isolation rating	Package
4DIR0400HA	4 forward 0 reverse (4+0)	Low	Active-high	V_{ISO} = 5700 V_{rms} (UL1577 Ed. 5)	PG-DSO-16 wide-body 300 mil 10.3 x 10.3 mm
4DIR0401HA		High			
4DIR1400HA	3 forward 1 reverse (3+1)	Low			
4DIR1401HA		High			
4DIR2400HA	2 forward 2 reverse (2+2)	Low			
4DIR2401HA		High			
4DIR1420HA	3 forward 1 reverse (3+1)	Low	Active-low[1)]		
4DIR1421HA		High			

1) Ideal for shared SPI bus

Application examples

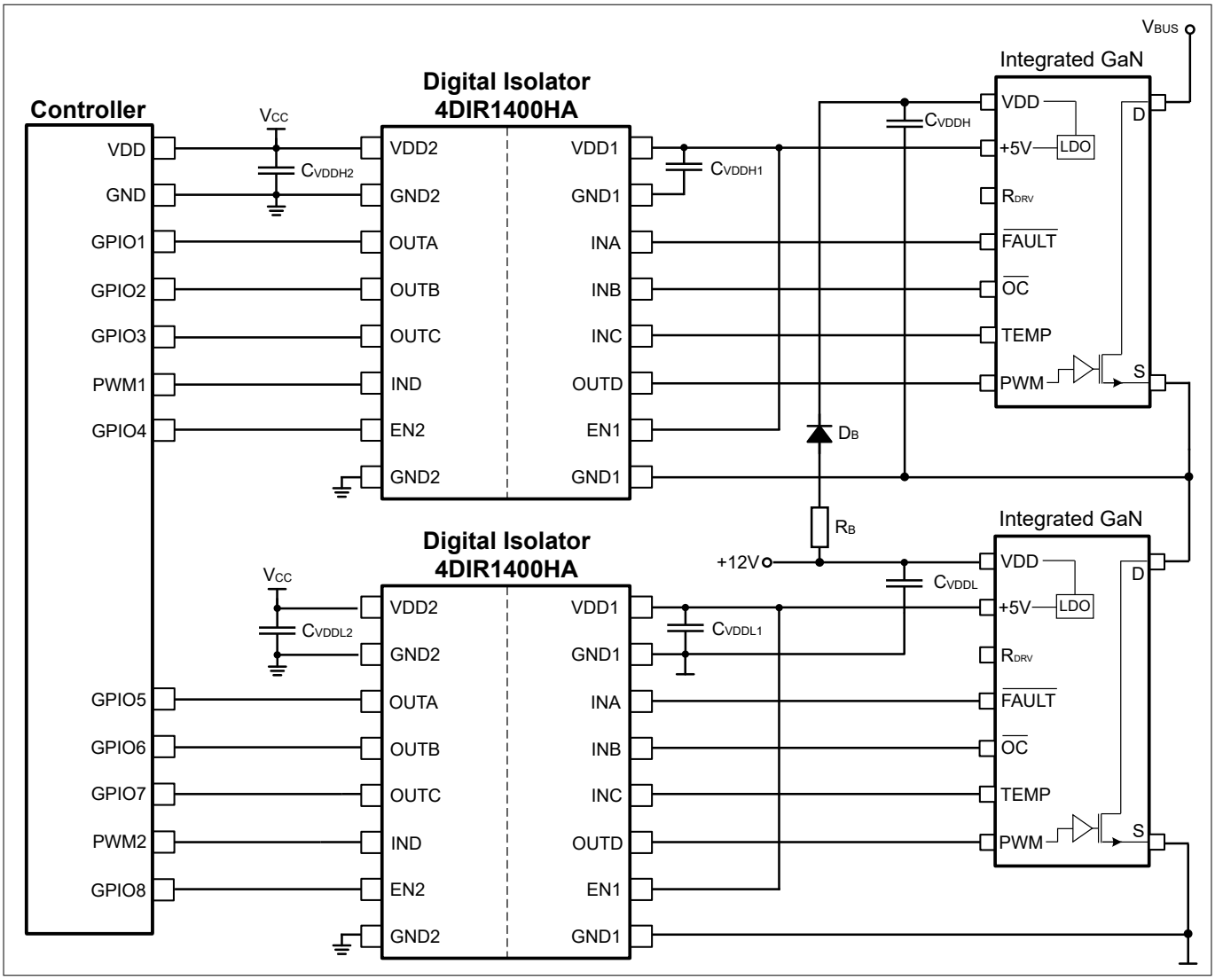

Figure 1 **Typical application driving half-bridge using GaN integrated power stage (IPS)**

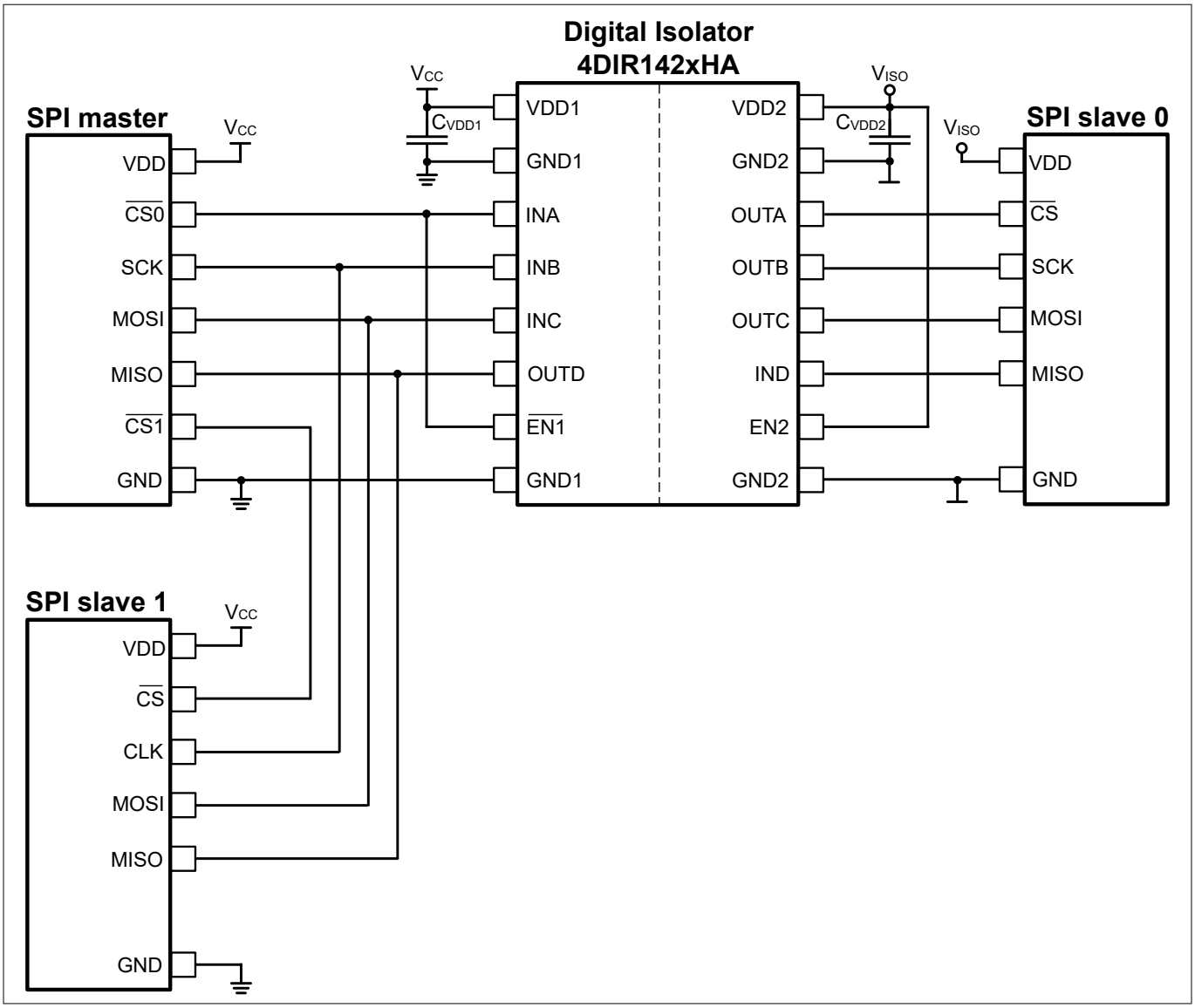

Figure 2 Typical application - Isolated SPI bus

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1 Functional block diagram

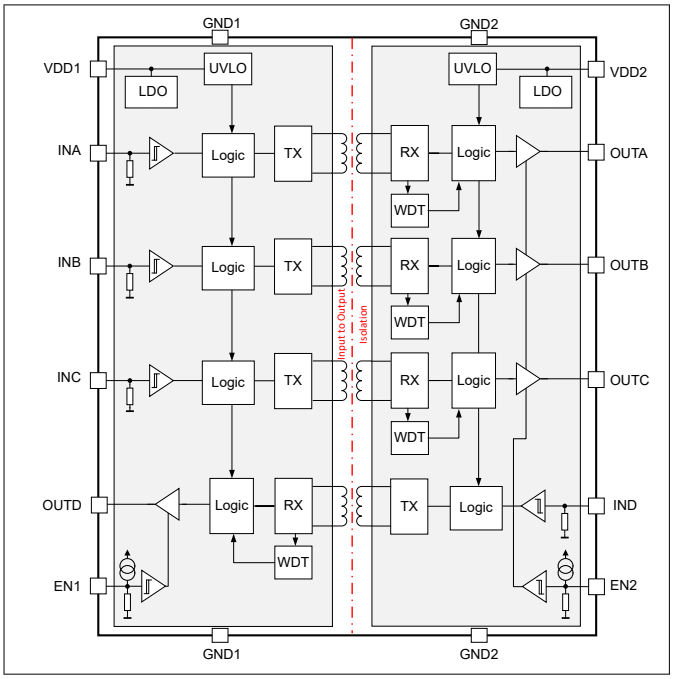

Figure 3 3+1 digital isolator (4DIR140xHA)

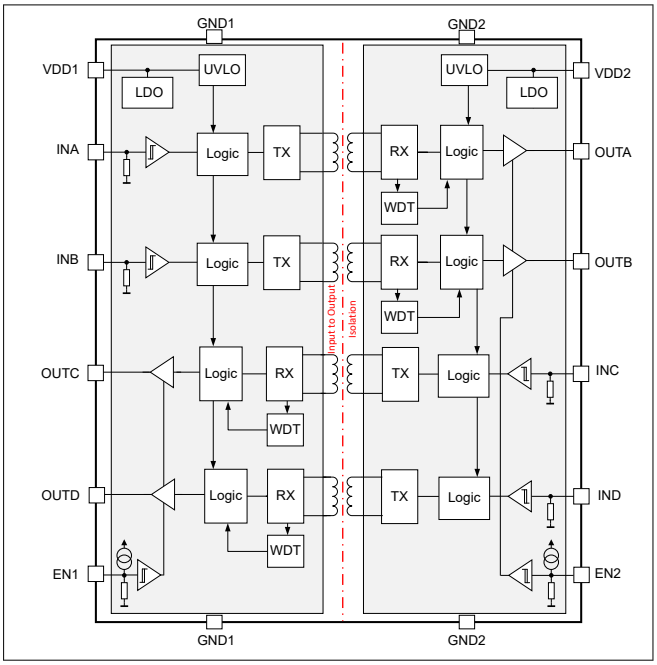

Figure 4 2+2 digital isolator (4DIR240xHA)

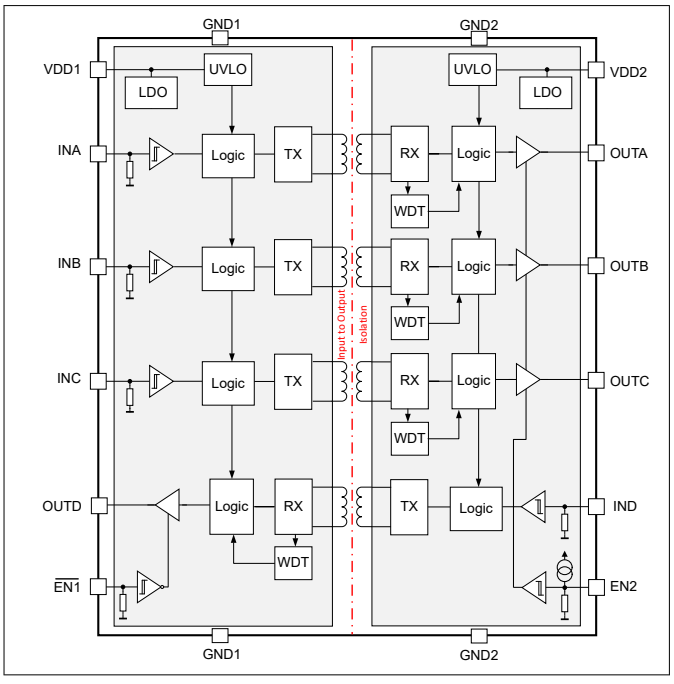

Figure 5 3+1 EN1 neg. digital isolator (4DIR142xHA)

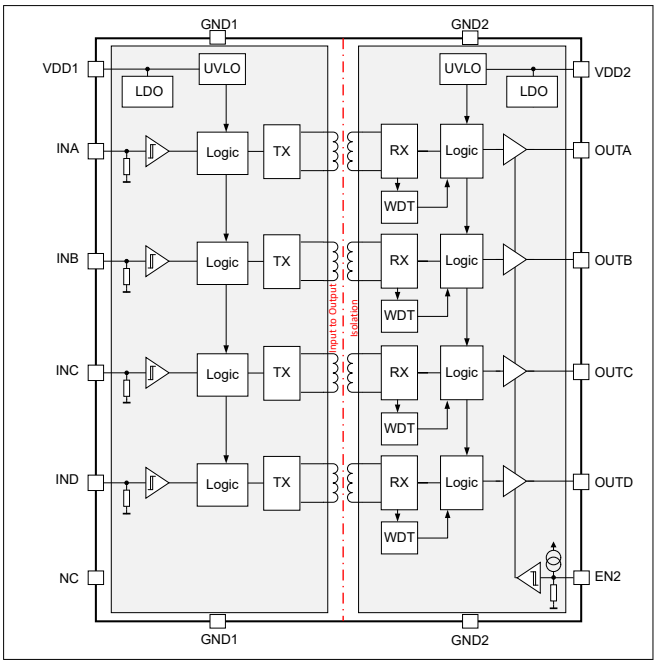

Figure 6 4+0 digital isolator (4DIR040xHA)

Output enable for the side 1 ($\overline{EN1}$) of the 4DIR142xHA is active-low, making it ideal for isolating a port on a shared SPI bus since the CS signal can directly enable the MISO signal on the isolator.

2 Pin configuration

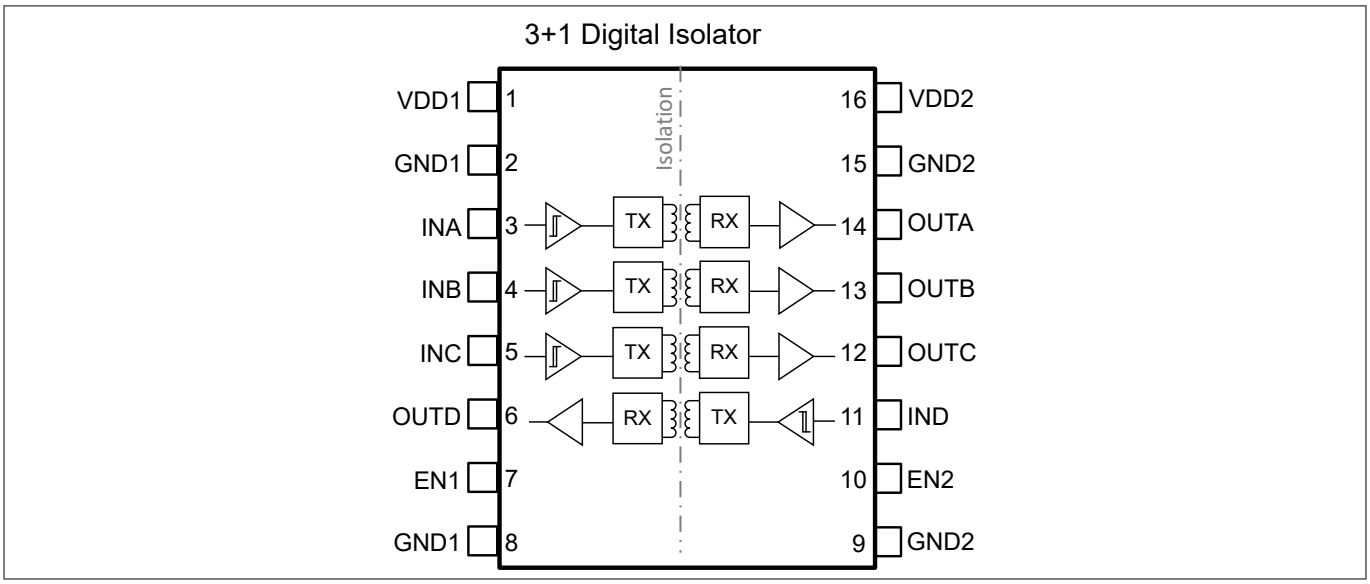

Figure 7 Pin-out for 4DIR140xHA

Table 1 Pin definitions and functions for 4DIR140xHA

Name	Pin	Type	Function
VDD1	1	I	Positive supply voltage 1
GND1	2	-	Ground 1
INA	3	I	Channel A input
INB	4	I	Channel B input
INC	5	I	Channel C input
OUTD	6	O	Channel D output
EN1	7	I	Enable 1 (internally pulled-up). Output pins on side 1 are enabled when EN1 is high or open and in high-impedance state when EN1 is low. Do not leave open. Connect to VDD1 to enable outputs or to GND1 to put outputs in high-impedance
GND1	8	-	Ground 1
GND2	9	-	Ground 2
EN2	10	I	Enable 2 (internally pulled-up). Output pins on side 2 are enabled when EN2 is high or open and in high-impedance state when EN2 is low. Do not leave open. Connect to VDD2 to enable outputs or to GND2 to put outputs in high-impedance
IND	11	I	Channel D input
OUTC	12	O	Channel C output
OUTB	13	O	Channel B output
OUTA	14	O	Channel A output
GND2	15	-	Ground 2
VDD2	16	I	Positive supply voltage 2

2 Pin configuration

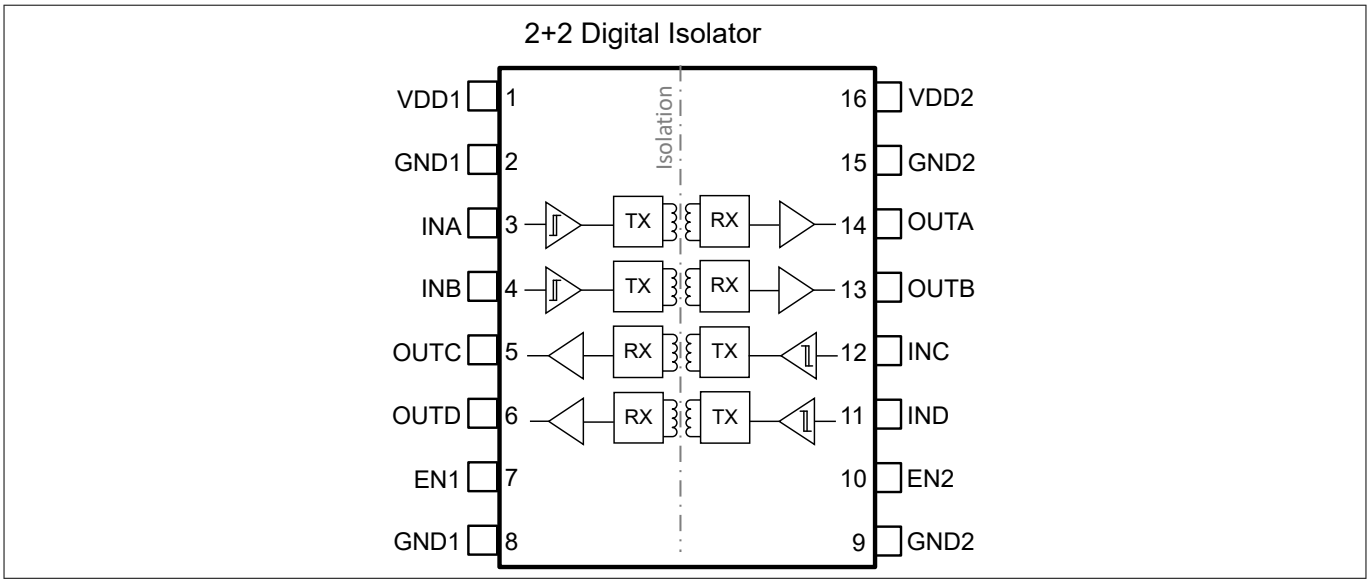

Figure 8 Pin-out for 4DIR240xHA

Table 2 Pin definitions and functions for 4DIR240xHA

Name	Pin	Type	Function
VDD1	1	I	Positive supply voltage 1
GND1	2	-	Ground 1
INA	3	I	Channel A input
INB	4	I	Channel B input
OUTC	5	O	Channel C output
OUTD	6	O	Channel D output
EN1	7	I	Enable 1 (internally pulled-up). Output pins on side 1 are enabled when EN1 is high or open and in high-impedance state when EN1 is low. Do not leave open. Connect to VDD1 to enable outputs or to GND1 to put outputs in high-impedance
GND1	8	-	Ground 1
GND2	9	-	Ground 2
EN2	10	I	Enable 2 (internally pulled-up). Output pins on side 2 are enabled when EN2 is high or open and in high-impedance state when EN2 is low. Do not leave open. Connect to VDD2 to enable outputs or to GND2 to put outputs in high-impedance
IND	11	I	Channel D input
INC	12	I	Channel C input
OUTB	13	O	Channel B output
OUTA	14	O	Channel A output
GND2	15	-	Ground 2
VDD2	16	I	Positive supply voltage 2

2 Pin configuration

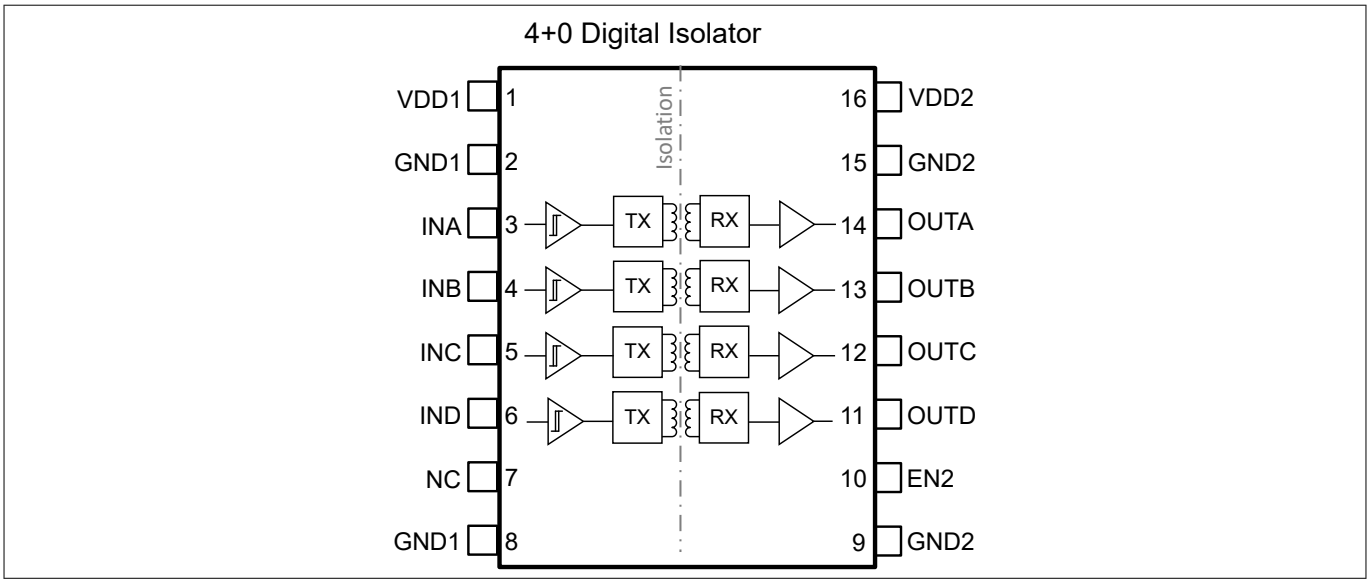

Figure 9 Pin-out for 4DIR040xHA

Table 3 Pin definitions and functions for 4DIR040xHA

Name	Pin	Type	Function
VDD1	1	I	Positive supply voltage 1
GND1	2	-	Ground 1
INA	3	I	Channel A input
INB	4	I	Channel B input
INC	5	I	Channel C input
IND	6	I	Channel D input
NC	7	-	No connect. Leave this pin floating
GND1	8	-	Ground 1
GND2	9	-	Ground 2
EN2	10	I	Enable 2 (internally pulled-up). Output pins on side 2 are enabled when EN2 is high or open and in high-impedance state when EN2 is low. Do not leave open. Connect to VDD2 to enable outputs or to GND2 to put outputs in high-impedance
OUTD	11	O	Channel D output
OUTC	12	O	Channel C output
OUTB	13	O	Channel B output
OUTA	14	O	Channel A output
GND2	15	-	Ground 2
VDD2	16	I	Positive supply voltage 2

2 Pin configuration

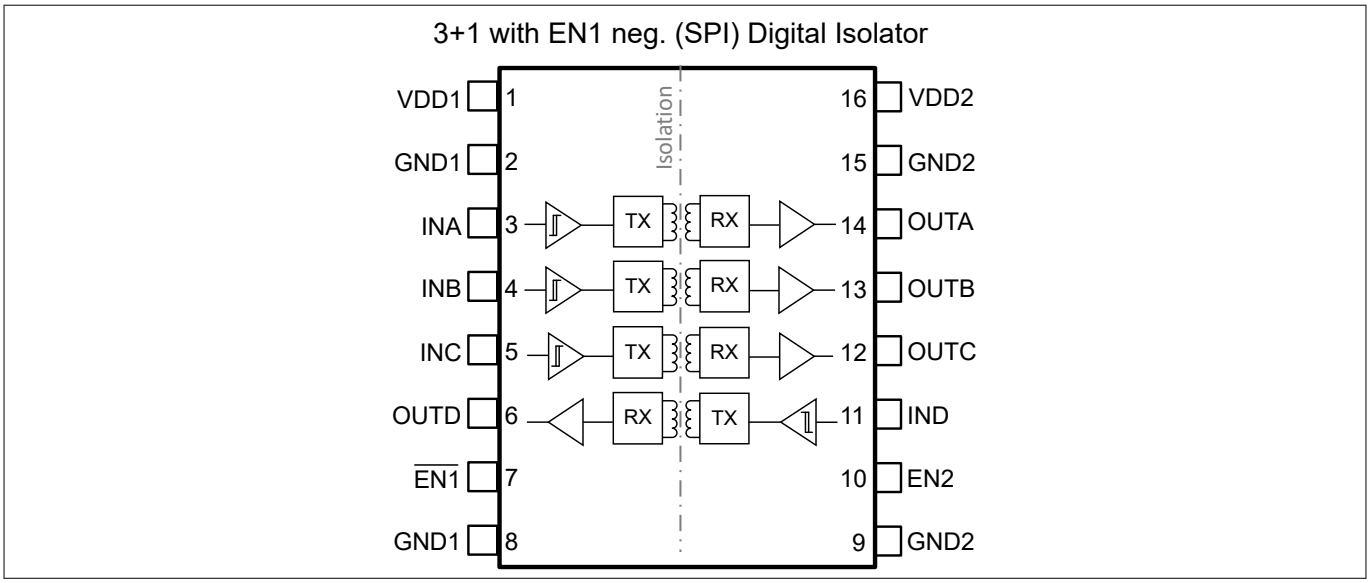

Figure 10 Pin-out for 4DIR142xHA

Table 4 Pin definitions and functions for 4DIR142xHA

Name	Pin	Type	Function
VDD1	1	I	Positive supply voltage 1
GND1	2	-	Ground 1
INA	3	I	Channel A input
INB	4	I	Channel B input
INC	5	I	Channel C input
OUTD	6	O	Channel D output
$\overline{EN1}$	7	I	Negated enable 1 (internally pulled-down). Output pins on side 1 are enabled when $\overline{EN1}$ is low or open and in high-impedance state when $\overline{EN1}$ is high. Do not leave open. Connect to GND1 to enable outputs or to VDD1 to put outputs in high-impedance
GND1	8	-	Ground 1
GND2	9	-	Ground 2
EN2	10	I	Enable 2 (internally pulled-up). Output pins on side 2 are enabled when EN2 is high or open and in high-impedance state when EN2 is low. Do not leave open. Connect to VDD2 to enable outputs or to GND2 to put outputs in high-impedance
IND	11	I	Channel D input
OUTC	12	O	Channel C output
OUTB	13	O	Channel B output
OUTA	14	O	Channel A output
GND2	15	-	Ground 2
VDD2	16	I	Positive supply voltage 2

3 Functional description

This chapter provides a summary of the integrated functions and features, and describes the relationships between them. The parameters and equations are based on typical values at T_A = 25 °C.

3.1 Truth tables

Table 5 Truth table for 4-channel Digital Isolator

V_{DDI}	V_{DDO}	V_{ENX} [1]	V_{INX}	V_{OUTX}
Powered	Powered	H or NC [2]	H	H
			L	L
		L	X [3]	Z [4]
Unpowered	Powered	H or NC	X	Default [5]
		L	X	Z
X	Unpowered	X	X	Z

1) EN1 controls the output on side 1 and EN2 controls the outputs on side 2
2) Not connected
3) X means "irrelevant"
4) Z means "high-impedance"
5) Refer to product variants

Table 6 Truth table for 4-channel Digital Isolator (3+1 EN1 neg. digital isolator)

V_{DDI}	V_{DDO}	$V_{\overline{EN1}}$ [1]	V_{EN2} [2]	V_{INX}	V_{OUTX}
Powered	Powered	L or NC	H or NC	H	H
				L	L
		H	L	X	Z
Unpowered	Powered	L or NC	H or NC	X	Default
		H	L	X	Z
X	Unpowered	X	X	X	Z

1) Controls the outputs on side 1
2) Controls the outputs on side 2

3.2 Timing diagrams

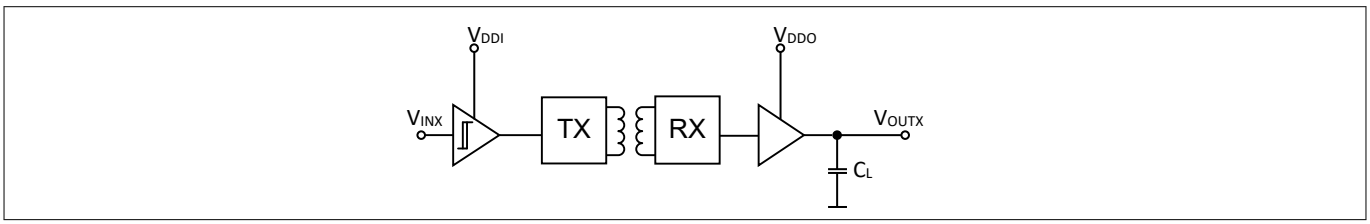

Figure 11 Test circuit

Figure 12 illustrates the input-to-output propagation delays as observed at the capacitively loaded output.

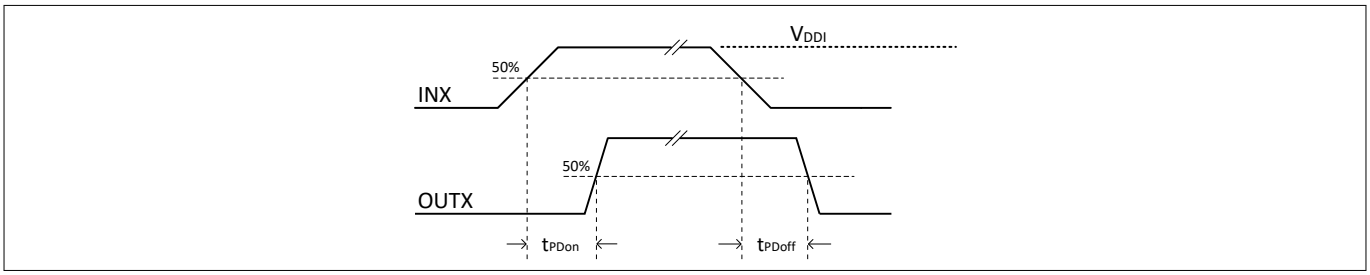

Figure 12 Propagation delays

Figure 13 illustrates the rise and fall time as observed at the capacitively loaded output.

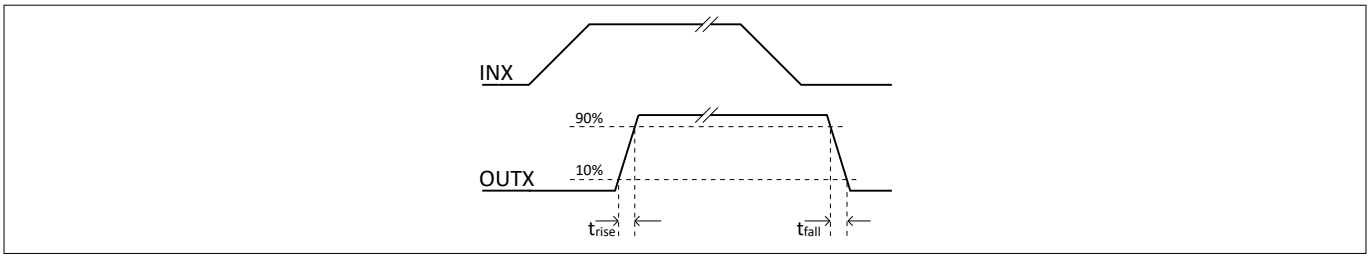

Figure 13 Rise, fall times

Figure 14 illustrates the output behavior to supply UVLO events when $V_{DD1/2}$ crosses the UVLO thresholds during rising or falling transitions (power-up, power-down, supply noise). Note that the input (V_{DD1}) and output (V_{DD2}) supplies are rising and falling at the same time.

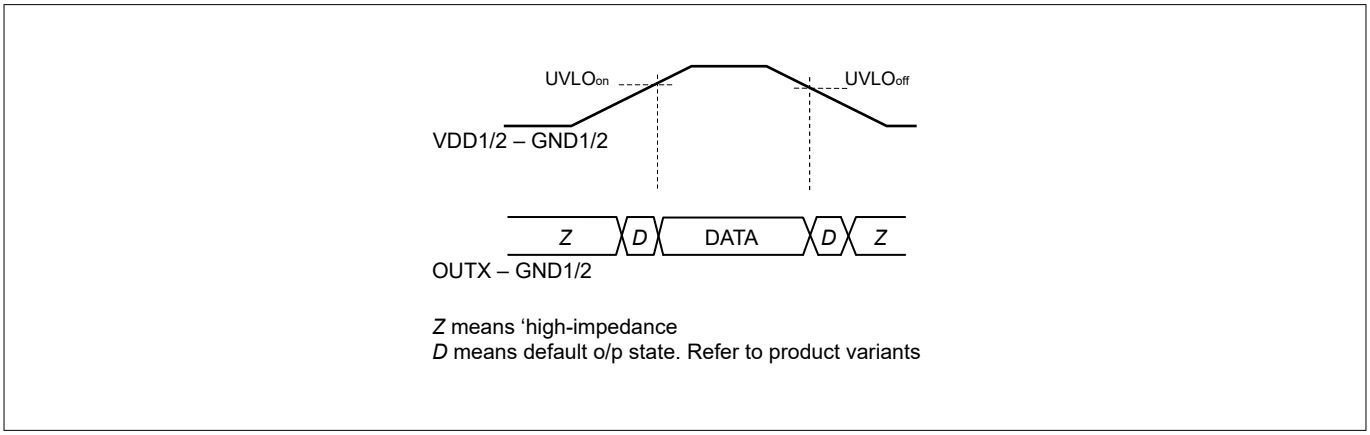

Figure 14 Undervoltage lockout

Figure 15 illustrates the propagation delay between the rising and falling edges of the EN signal to the output following the input signal.

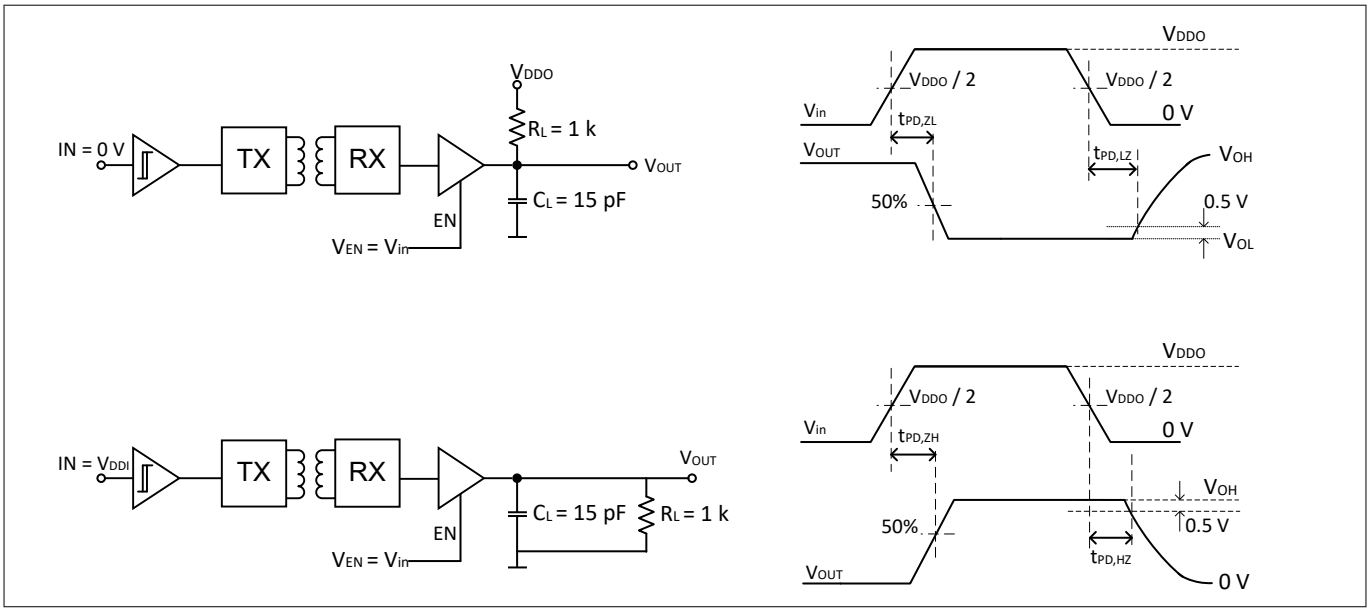

Figure 15 Output enable/disable propagation delays

Figure 16 illustrates the time to default output state when the input loses supply.

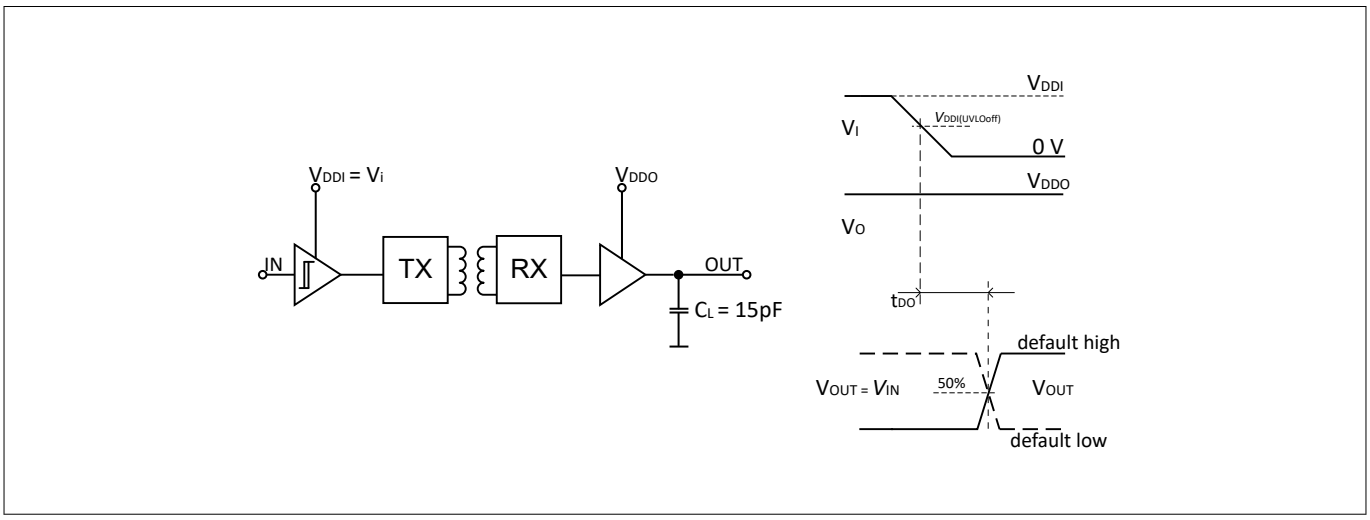

Figure 16 Default output delay time

Figure 17 illustrates the output behavior when input and output side supplies have different power-up timings where the power-up time is t_{PU}=max{t_{PU1}, t_{PU2}}.

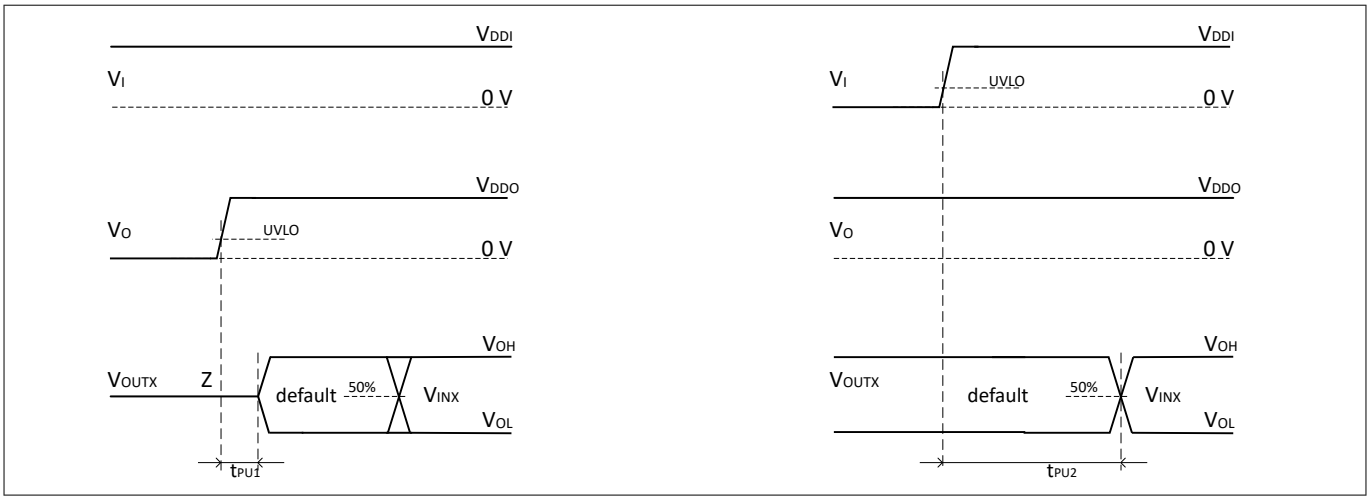

Figure 17 Power-up delay time

3.3 Data transmission input-to-output

Communication based on Coreless Transformer (CT) is used for signal transfer between input and output channels. If a constant DC level within the operating range is applied at the input, a proven high resolution pulse repetition scheme ensure functionality, enabling the output to follow the constant DC input. It also enables recovery from communication fails and safe system shutdown. In case of a power loss at the input channel, the pulse repetition scheme will be disabled and a watch-dog timer at the output triggers approximately after t_{DO} time period and drives the channel output to the default state. In case of multiple channels on the output side, the first watch-dog timer detecting the power loss at the input will drive all output channels on that side to default value. Once the power supply on the input channels is above the threshold value ($V_{DDX(UVLOon)}$), the communication is restored and the output will follow the input as shown in Figure 17.

3.4 Input/output voltage levels description

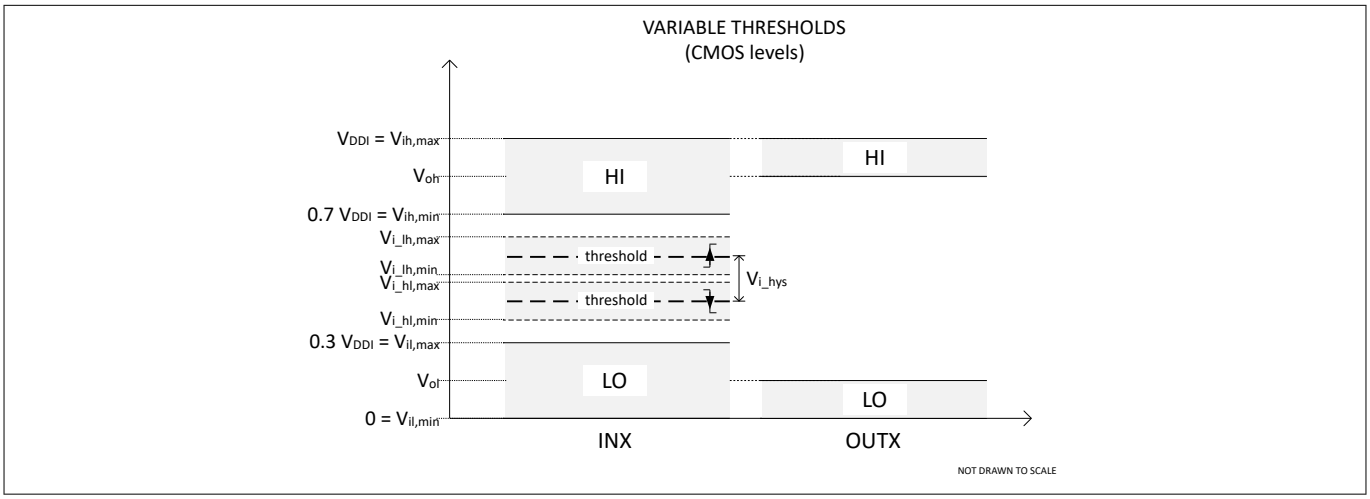

Figure 18 CMOS variable thresholds description

3.5 Supply characteristics

Maximum values are given at T_A = 125°C, C_{LOAD} = 15 pF and 50% duty cycle input square wave.

3+1 digital isolator (4DIR140xHA)

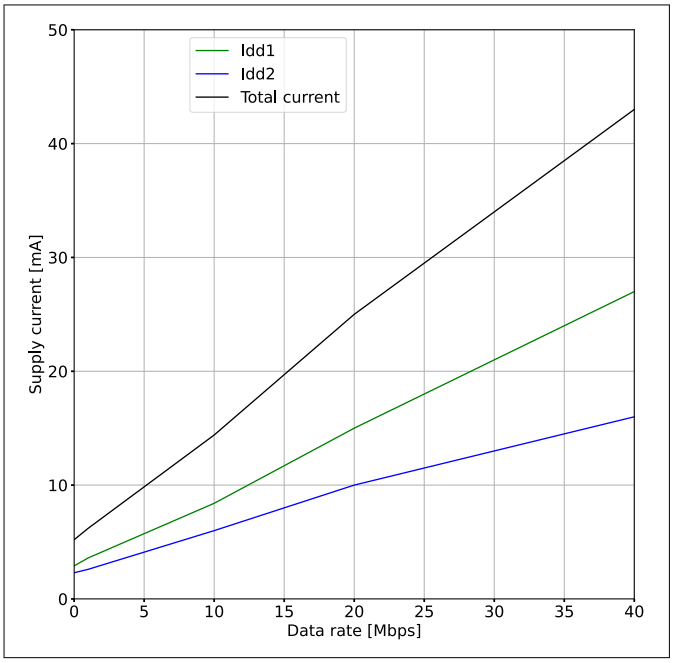

Figure 19 **Supply current vs. data rate (V_{DD1} = V_{DD2} = 6.5 V)**

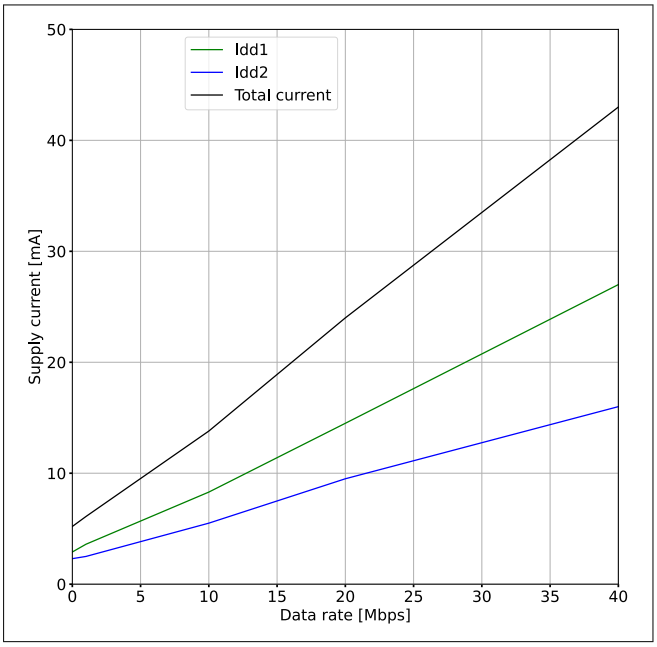

Figure 20 **Supply current vs. data rate (V_{DD1} = V_{DD2} = 5.0 V)**

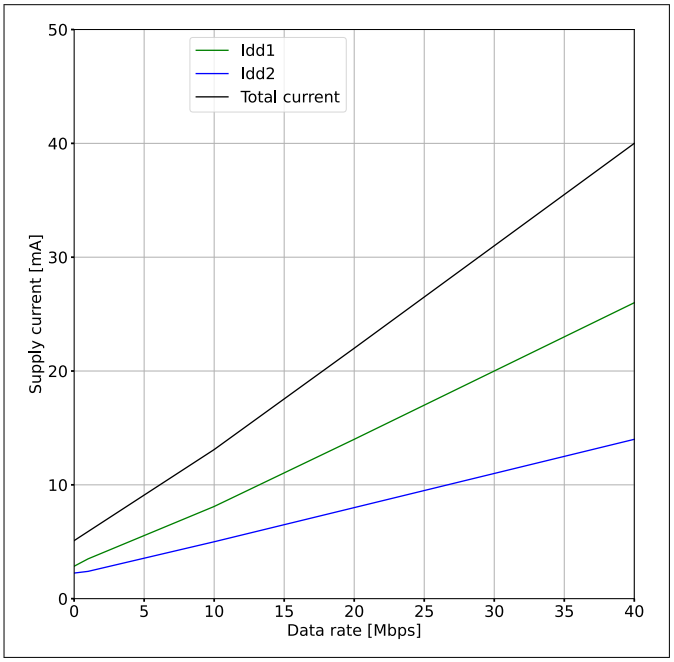

Figure 21 **Supply current vs. data rate (V_{DD1} = V_{DD2} = 3.3 V)**

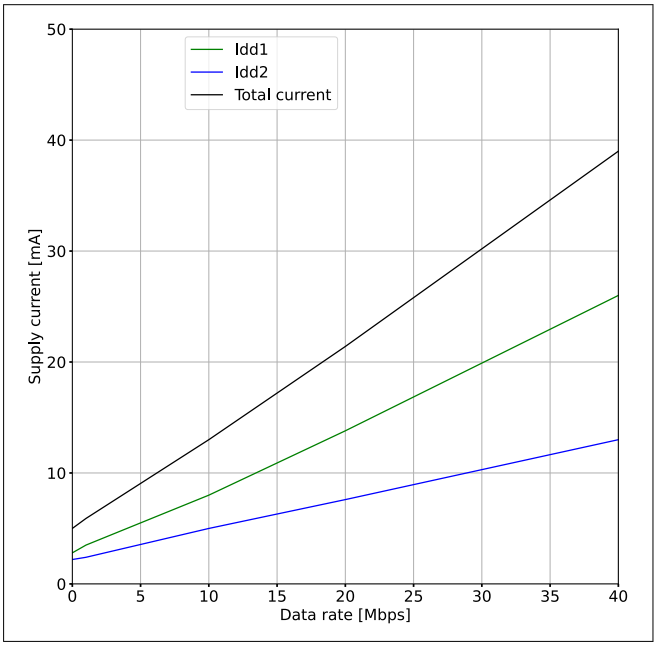

Figure 22 **Supply current vs. data rate (V_{DD1} = V_{DD2} = 2.7 V)**

3+1 EN1 neg. digital isolator (4DIR142xHA)

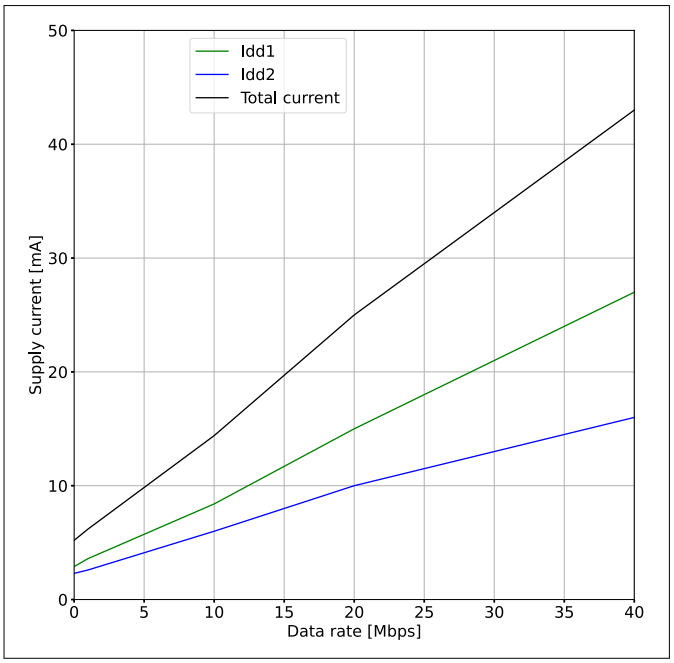

Figure 23 **Supply current vs. data rate (V_{DD1} = V_{DD2} = 6.5 V)**

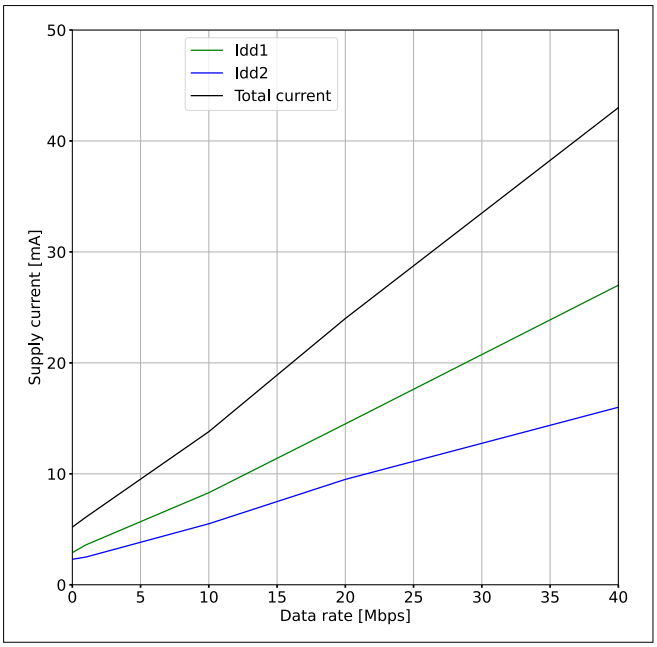

Figure 24 **Supply current vs. data rate (V_{DD1} = V_{DD2} = 5 V)**

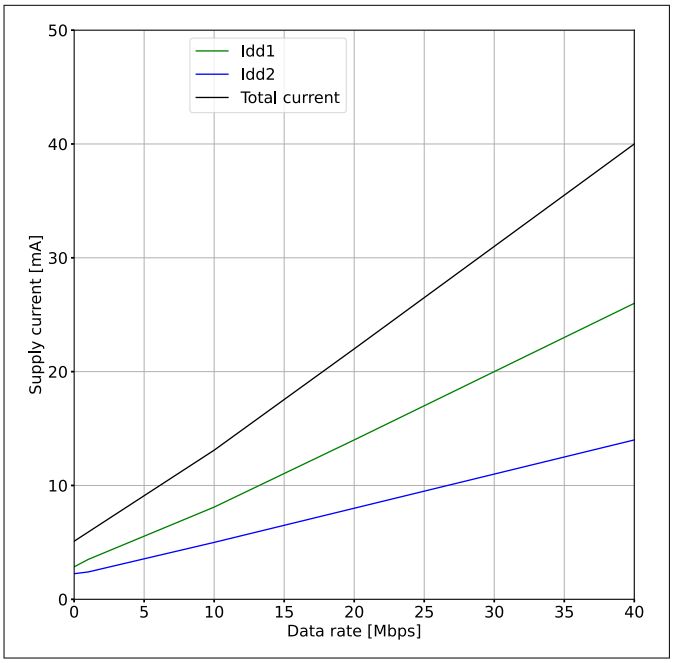

Figure 25 **Supply current vs. data rate (V_{DD1} = V_{DD2} = 3.3 V)**

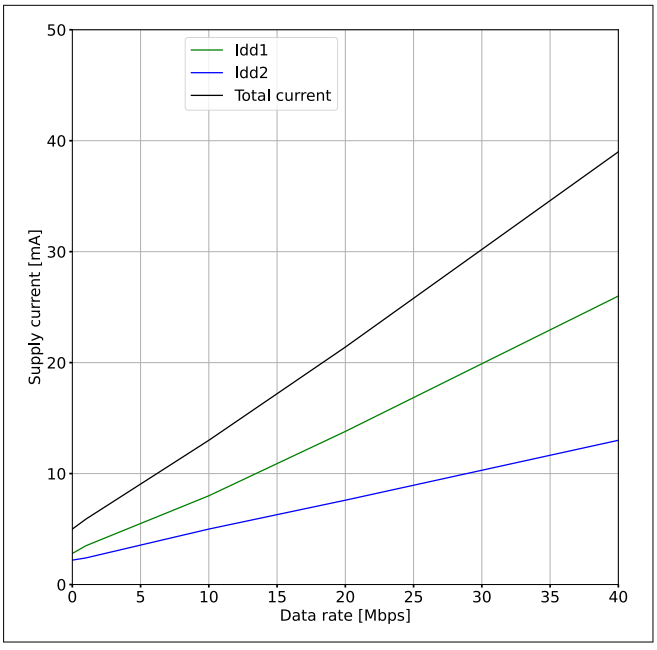

Figure 26 **Supply current vs. data rate (V_{DD1} = V_{DD2} = 2.7 V)**

2+2 digital isolator (4DIR240xHA)

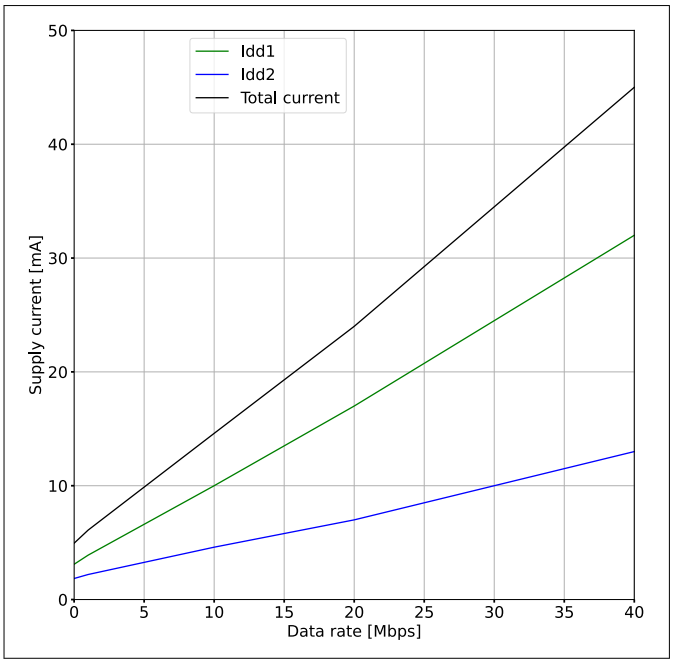

Figure 27 **Supply current vs. data rate (V_{DD1} = V_{DD2} = 6.5 V)**

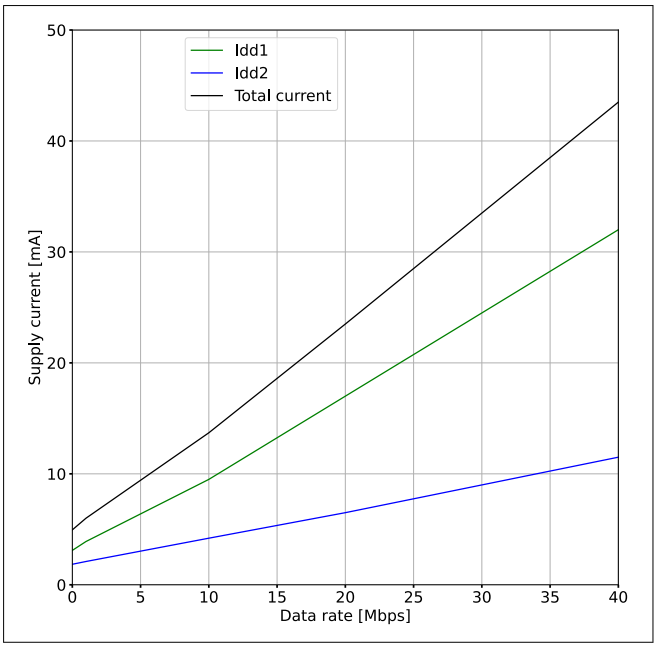

Figure 28 **Supply current vs. data rate (V_{DD1} = V_{DD2} = 5 V)**

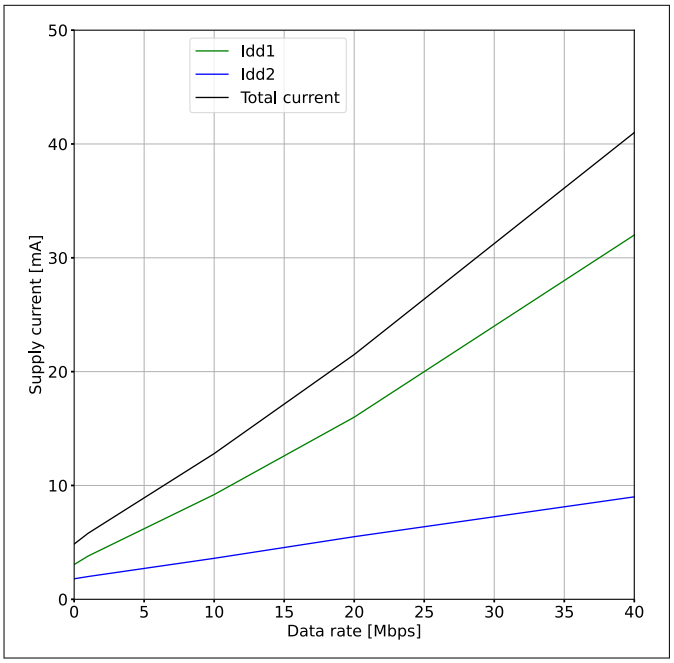

Figure 29 **Supply current vs. data rate (V_{DD1} = V_{DD2} = 3.3 V)**

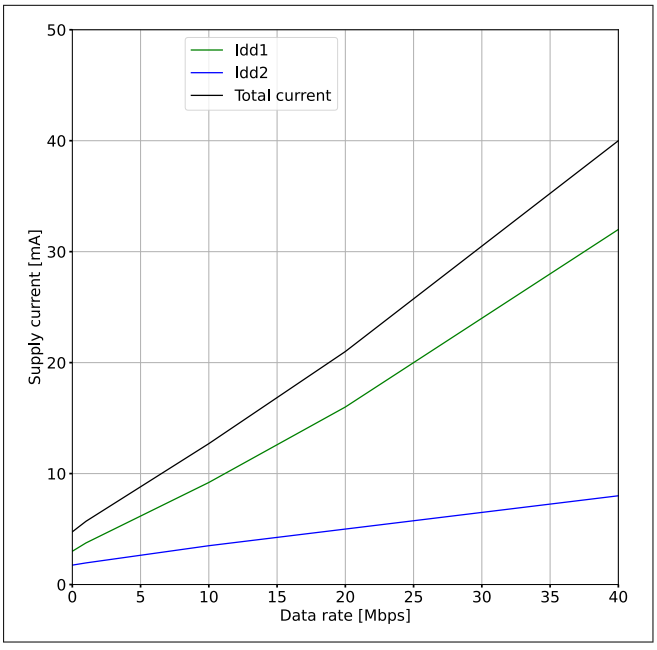

Figure 30 **Supply current vs. data rate (V_{DD1} = V_{DD2} = 2.7 V)**

4+0 digital isolator (4DIR040xHA)

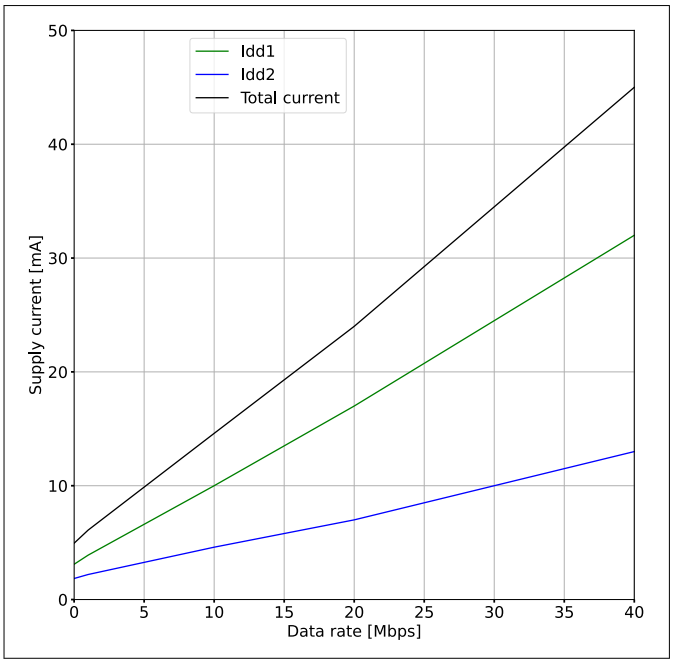

Figure 31 **Supply current vs. data rate (V_{DD1} = V_{DD2} = 6.5 V)**

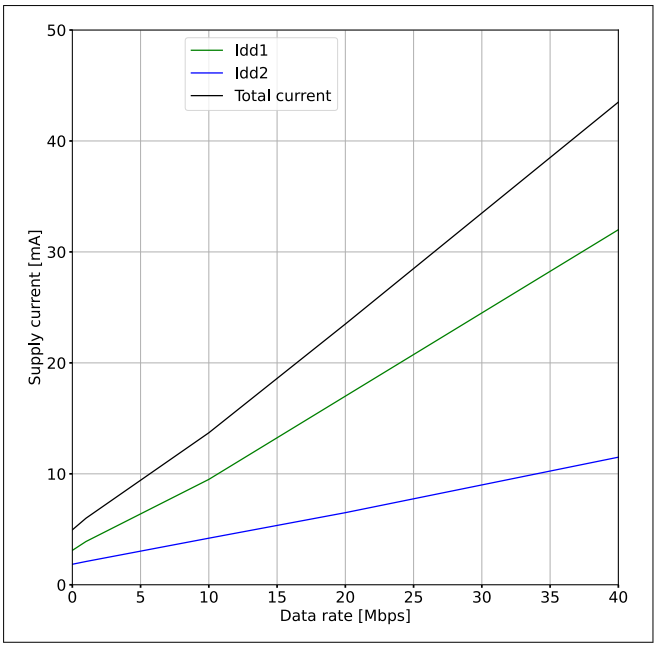

Figure 32 **Supply current vs. data rate (V_{DD1} = V_{DD2} = 5 V)**

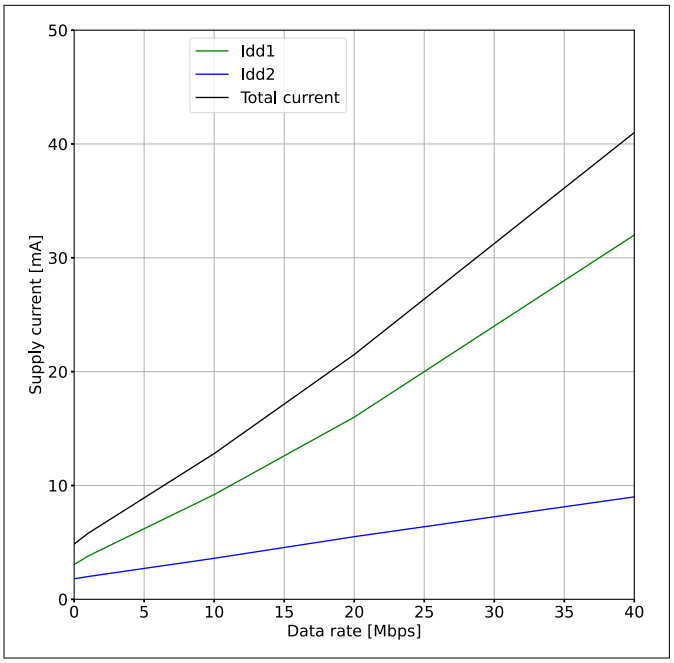

Figure 33 **Supply current vs. data rate (V_{DD1} = V_{DD2} = 3.3 V)**

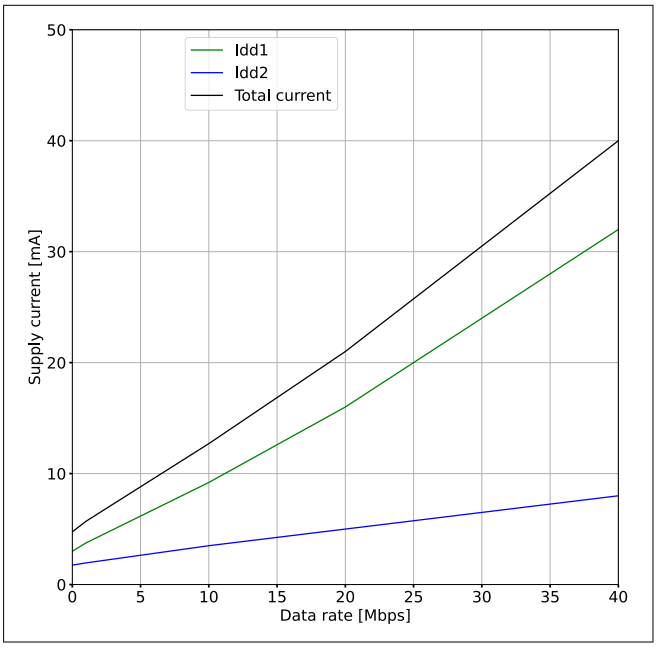

Figure 34 **Supply current vs. data rate (V_{DD1} = V_{DD2} = 2.7 V)**

4 Thermal and electrical characteristics

4.1 Absolute maximum ratings

Table 7 Absolute maximum ratings

Note: Stresses above the values listed below may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding these values may cause irreversible damage to the integrated circuit. These values are not tested during production test.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Supply voltage	V_{DD1}, V_{DD2}	-0.5		7.5	V	
Voltage at pins INx	V_{INX}			V_{DDI} + 0.5	V	1)
Voltage at pins OUTx	V_{OUTX}			V_{DDO} + 0.5	V	1)
Average output current per pin	I_{OUT}	-10		+10	mA	
Junction temperature	T_J	-40		150	°C	
Storage temperature	T_{STG}	-65		150	°C	
Soldering temperature	T_{SOL}			260	°C	reflow soldering according to JEDEC-J-STD-020
Electrostatic discharge HBM	V_{ESD_HBM}	-2		2	kV	Human Body Model (HBM) according to AEC-Q100-002
Electrostatic discharge CDM	V_{ESD_CDM}	-1.75		1.75	kV	Charged Device Model (CDM) according to AEC-Q100-011 Rev. D
Latch-up capability	I_{LU}			150	mA	Latch-up immunity characterization according to JEDEC78E Class II, pin voltages according to abs. max. ratings

1) V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of a given channel, respectively

4.2 Additional ESD ratings

Table 8 Additional ESD ratings

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Contact discharge per IEC 61000-4-2	$\lvert V_{ESD\_IEC} \rvert$		22		kV	Isolation barrier withstand test[1) 2)]

1) IEC ESD strike is applied across the barrier with all pins on each side tied together creating a two-terminal device.
2) Testing is carried out in air or oil to determine the intrinsic contact discharge capability of the device.

4.3 Operating range

Table 9 Operating range

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Data rate	DR	0		40	Mbps	
Supply voltage	V_{DD1}, V_{DD2}	2.7		6.5	V	
High-level input voltage	V_{IH}	0.7 V_{DI}		V_{DDI}	V	1)
Low-level input voltage	V_{IL}	0		0.3 V_{DI}	V	1)
Ambient temperature	T_A	-40		125	°C	

1) V_{DDI} = Input-side supply voltage. For input channels on side 1 it is V_{DD1} and for input channels on side 2 it is V_{DD2}

4.4 Common Mode Transient Immunity (CMTI)

Table 10 Common Mode Transient Immunity (CMTI)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Static Common Mode Transient Immunity (CMTI)	$\|CM_H\|$	100			kV/µs	V_{CM} = 1200 V; V_{INX} tied to V_{DDI} 1) 2) 3)
Static Common Mode Transient Immunity (CMTI)	$\|CM_L\|$	100			kV/µs	V_{CM} = 1200 V; V_{INX} tied to GNDX 2) 3)

1) V_{DDI} refers to the supply voltages on the input side of a given channel
2) Minimum slew rate of a common mode voltage at which the output signal is disturbed
3) Parameters not tested in production

4.5 Thermal characteristics

Typical thermal characteristics at T_A = 25°C

Table 11 Thermal characteristics for JEDEC and Reference PCB

Parameter	Symbol	JEDEC	Reference PCB	Unit	Note or condition
Thermal resistance junction-to-ambient	R_{thJA}	60 [1]	59 [2]	K/W	JEDEC 2s2p (JED51-7), P_{dis} = 378 mW
Thermal resistance junction-to-case (top)	R_{thJC}	27	27	K/W	[3]
Thermal resistance junction-to-board	R_{thJB}	20	30	K/W	[4]
Characterization parameter junction-to-top	Ψ_{thJT}	3.4	3	K/W	[5]
Characterization parameter junction-to-board	Ψ_{thJB}	20	20	K/W	[5]

1) Obtained by simulating a JEDEC - standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a

2) Obtained by simulating a JEDEC-standard, high-K board, as specified in JESD51-7 and in reference PCB specifications below, in an environment described in JESD51-2a

3) Obtained by simulating a cold plate test on the package top. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88

4) Obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8

5) Estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining R_{th}, using a procedure described in JESD51-2a (sections 6 and 7)

Table 12 Reference PCB specifications

Parameter	Value	λ_{therm} [W/(m-K)]
Dimension [mm^3]	76.2 x 114.3 x 1.5 (JEDEC)	
Material	FR4	0.3
Metalization	JEDEC 2s2p (JESD 51-7)	388
Cooling area	Ground inner layer	
Thermal vias	∅ = 0.5mm; plating 25µm; 4 x 2 pcs. connected to ground inner layer	
Package attach [50 µm]	Solder	55
Ground inner layer [mm^3]	74.2 x 74.2 x 0.03 (JEDEC), planes are 8.2 mm spaced	

Table 13 Reference PCB layout

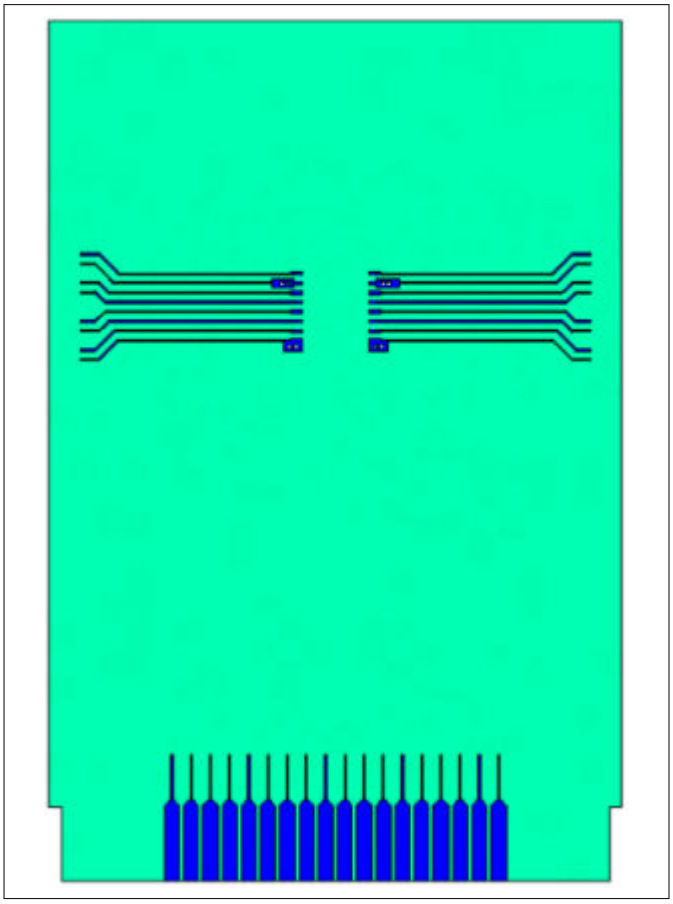

Figure 35 Top footprint

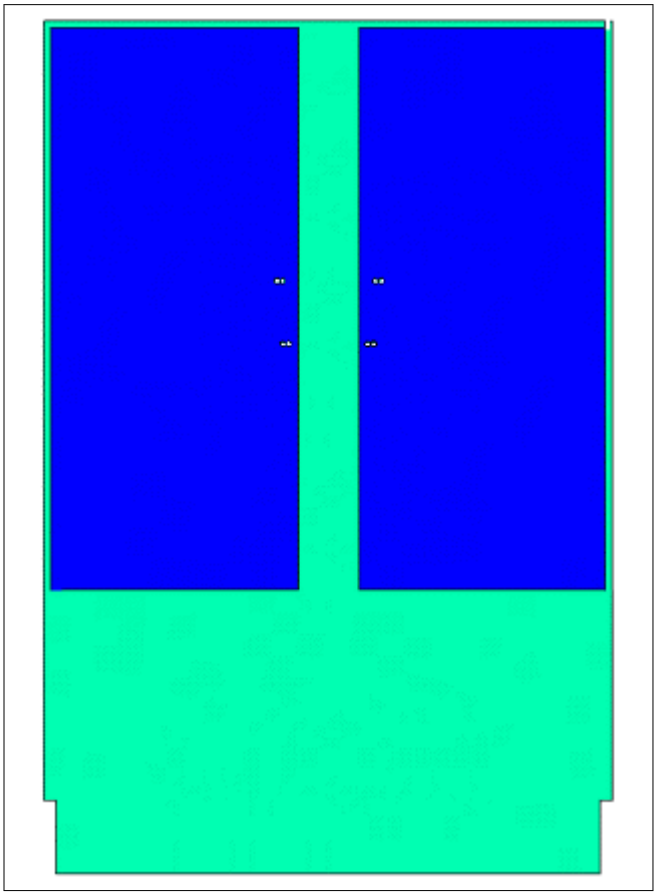

Figure 36 Inner layers (connect to ground)

4.6 Power supply - UVLO

Table 14 Power supply - UVLO

Typical values are given at T_A = 25 °C over operating range unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Supply UVLO turn-on threshold	$V_{DDX(UVLOon)}$	2.42	2.55	2.68	V	
Supply UVLO turn-off threshold	$V_{DDX(UVLOoff)}$	2.35	2.45	2.55	V	
Supply UVLO hysteresis	$V_{DDX(UVLOhys)}$	0.07	0.10		V	

4.7 Electrical characteristics

The electrical characteristics involve the spread of values given within the specified operating conditions.

4.7.1 Electrical characteristics - 6.5 V supply

Typical values are given at T_A = 25 °C with V_{DD1} = V_{DD2} = 6.5 V. Minimum/maximum specifications apply over the entire recommended operation range of V_{DD1} = V_{DD2} = 6.5 V, and -40°C ≤ T_A ≤ 125°C, unless otherwise noted. Switching characteristics are tested with C_{LOAD} = 15 pF and 50% duty-cycle input square wave, over operating range unless otherwise specified. Supply current values are specified considering that all channels are switching at the same data rate. Parameters are not tested in production unless otherwise specified.

4.7.1.1 Logic inputs

Table 15 Logic inputs

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
High-level input current	I_{IH}			10	µA	V_{INX} = V_{DDI} 1) 2)
Low-level input current	I_{IL}	-10			µA	V_{INX} = 0 V 2)
Input voltage threshold for transition LH	V_{I_LH}			0.7 V_{DDI}	V	
Input voltage threshold for transition HL	V_{I_HL}	0.3 V_{DDI}			V	
Input voltage threshold hysteresis	V_{I_HYS}	0.1 V_{DDI}			V	
Input pull-down resistor	R_{IN}		825		kΩ	V_{INX} = V_{DDI} 1)

1) V_{DDI} = Input-side supply voltage. For input channels on side 1 it is V_{DD1} and for input channels on side 2 it is V_{DD2}
2) Parameter tested in production

4.7.1.2 Logic outputs

Table 16 Logic outputs

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
High-level output voltage	V_{OH}	V_{DDO} - 0.4			V	I_{OH} = 4 mA 1)
Low-level output voltage	V_{OL}			0.4	V	I_{OL} = -4 mA

1) V_{DDO} - Output-side supply voltage. For output buffers on side 1 it is V_{DD1} and for output buffers on side 2 it is V_{DD2}

4.7.1.3 Power supply - 4DIR040xHA (4+0)

Table 17 Power supply - 4DIR040xHA (4+0)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Supply current - DC input	I_{DD1}			3.1	mA	$V_{INx} = V_{DDI}$ [1)]
Supply current - DC input	I_{DD2}			1.85	mA	$V_{INx} = V_{DDI}$ [1)]
Supply current - DC input	I_{DD1}			3.1	mA	V_{INx} = 0 V
Supply current - DC input	I_{DD2}			1.85	mA	V_{INx} = 0 V
Supply current - AC input	I_{DD1_1Mb}			3.9	mA	*DR* = 1 Mbps
Supply current - AC input	I_{DD2_1Mb}			2.2	mA	*DR* = 1 Mbps
Supply current - AC input	I_{DD1_10Mb}			10	mA	*DR* = 10 Mbps
Supply current - AC input	I_{DD2_10Mb}			4.6	mA	*DR* = 10 Mbps
Supply current - AC input	I_{DD1_20Mb}			17	mA	*DR* = 20 Mbps
Supply current - AC input	I_{DD2_20Mb}			7	mA	*DR* = 20 Mbps
Supply current - AC input	I_{DD1_40Mb}			32	mA	*DR* = 40 Mbps
Supply current - AC input	I_{DD2_40Mb}			13	mA	*DR* = 40 Mbps

1) V_{DDI} = Input-side supply voltage. For input channels on side 1 it is V_{DD1}, and for input channels on side 2 it is V_{DD2}.

4.7.1.4 Power supply - 4DIR140xHA (3+1)

Table 18 Power supply - 4DIR140xHA (3+1)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Supply current - DC input	I_{DD1}			2.9	mA	$V_{INx} = V_{DDI}$ [1)]
Supply current - DC input	I_{DD2}			2.3	mA	$V_{INx} = V_{DDI}$ [1)]
Supply current - DC input	I_{DD1}			2.9	mA	V_{INx} = 0 V
Supply current - DC input	I_{DD2}			2.3	mA	V_{INx} = 0 V
Supply current - AC input	I_{DD1_1Mb}			3.6	mA	*DR* = 1 Mbps
Supply current - AC input	I_{DD2_1Mb}			2.6	mA	*DR* = 1 Mbps
Supply current - AC input	I_{DD1_10Mb}			8.4	mA	*DR* = 10 Mbps
Supply current - AC input	I_{DD2_10Mb}			6	mA	*DR* = 10 Mbps
Supply current - AC input	I_{DD1_20Mb}			15	mA	*DR* = 20 Mbps
Supply current - AC input	I_{DD2_20Mb}			10	mA	*DR* = 20 Mbps
Supply current - AC input	I_{DD1_40Mb}			27	mA	*DR* = 40 Mbps
Supply current - AC input	I_{DD2_40Mb}			16	mA	*DR* = 40 Mbps

1) V_{DDI} = Input-side supply voltage. For input channels on side 1 it is V_{DD1} and for input channels on side 2 it is V_{DD2}

4.7.1.5 Power supply - 4DIR240xHA (2+2)

Table 19 Power supply - 4DIR240xHA (2+2)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Supply current - DC input	I_{DD1}			2.7	mA	$V_{INx} = V_{DDI}$ [1)]
Supply current - DC input	I_{DD2}			2.7	mA	$V_{INx} = V_{DDI}$ [1)]
Supply current - DC input	I_{DD1}			2.7	mA	V_{INx} = 0 V
Supply current - DC input	I_{DD2}			2.7	mA	V_{INx} = 0 V
Supply current - AC input	I_{DD1_1Mb}			3.4	mA	*DR* = 1 Mbps
Supply current - AC input	I_{DD2_1Mb}			3.4	mA	*DR* = 1 Mbps
Supply current - AC input	I_{DD1_10Mb}			7.5	mA	*DR* = 10 Mbps
Supply current - AC input	I_{DD2_10Mb}			7.0	mA	*DR* = 10 Mbps
Supply current - AC input	I_{DD1_20Mb}			13	mA	*DR* = 20 Mbps
Supply current - AC input	I_{DD2_20Mb}			12	mA	*DR* = 20 Mbps
Supply current - AC input	I_{DD1_40Mb}			23	mA	*DR* = 40 Mbps
Supply current - AC input	I_{DD2_40Mb}			21	mA	*DR* = 40 Mbps

1) V_{DDI} - Input-side supply voltage. For input channels on side 1 it is V_{DD1} and for input channels on side 2 it is V_{DD2}

4.7.1.6 Power supply - 4DIR142xHA (3+1 EN1 neg.)

Table 20 Power supply - 4DIR142xHA (3+1 EN1 neg.)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Supply current - DC input	I_{DD1}			2.9	mA	$V_{INx} = V_{DDI}$ [1]
Supply current - DC input	I_{DD2}			2.3	mA	$V_{INx} = V_{DDI}$ [1]
Supply current - DC input	I_{DD1}			2.9	mA	V_{INx} = 0 V
Supply current - DC input	I_{DD2}			2.3	mA	V_{INx} = 0 V
Supply current - AC input	I_{DD1_1Mb}			3.6	mA	*DR* = 1 Mbps
Supply current - AC input	I_{DD2_1Mb}			2.6	mA	*DR* = 1 Mbps
Supply current - AC input	I_{DD1_10Mb}			8.4	mA	*DR* = 10 Mbps
Supply current - AC input	I_{DD2_10Mb}			6	mA	*DR* = 10 Mbps
Supply current - AC input	I_{DD1_20Mb}			15	mA	*DR* = 20 Mbps
Supply current - AC input	I_{DD2_20Mb}			10	mA	*DR* = 20 Mbps
Supply current - AC input	I_{DD1_40Mb}			27	mA	*DR* = 40 Mbps
Supply current - AC input	I_{DD2_40Mb}			16	mA	*DR* = 40 Mbps

1) V_{DDI} = Input-side supply voltage. For input channels on side 1 it is V_{DD1} and for input channels on side 2 it is V_{DD2}

4.7.1.7 Dynamic characteristics

Table 21 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
INx to OUTx turn-on propagation delay	t_{PDon}	21	26	33	ns	From 50% level of rising input to 50% level of corresponding rising output [1]
INx to OUTx turn-off propagation delay	t_{PDoff}	21	26	33	ns	From 50% level of rising input to 50% level of corresponding rising output [1]
Part-to-part propagation delays mismatch	$\Delta t_{PD,p\text{-}p}$			6	ns	[1] [2]
Co-directional channel-to-channel propagation delay mismatch	$\Delta t_{PD,Ch\text{-}Ch}$			3.5	ns	Within same sample, over operating temperature range, same direction channels, switching in the same direction [1]
Opposing directional channel-to-channel propagation delay mismatch	$\Delta t_{PD,Ch\text{-}Ch}$			3.5	ns	Within same sample, over operating temperature range, opposing directional channels, switching with the same signal level [1]
Pulse width distortion	*PWD*			3	ns	$\lvert t_{PDoff} - t_{PDon} \rvert$ [1] [3]
Input pulse width that changes output state	$t_{pw,min}$	8	12.5	16	ns	Measured with full range of input signal $V_{IN} = V_{DDI}$ [4]
Output signal rise time	t_{rise}			4	ns	10% to 90% rising output, C_{LOAD} = 15 pF
Output signal fall time	t_{fall}			4	ns	90% to 10% falling output, C_{LOAD} = 15 pF
Output disable propagation delay (high output to high-impedance)	$t_{PD,HZ}$			10	ns	From 50% falling enable (except 4DIR142xHA) to V_{OH} - 0.5 V From 50% rising enable (for 4DIR142xHA) to V_{OH} - 0.5 V
Output disable propagation delay (low output to high impedance)	$t_{PD,LZ}$			10	ns	From 50% of falling enable (except 4DIR142xHA) to V_{OL} + 0.5 V From 50% of rising enable (for 4DIR142xHA) to V_{OL} + 0.5 V
Output enable propagation delay (high-impedance to high output)	$t_{PD,ZH}$			15	ns	From 50% rising enable (except 4DIR142xHA) to 50% of rising V_{OH} From 50% falling enable (for 4DIR142xHA) to 50% of rising V_{OH}

(table continues...)

Table 21 (continued) Dynamic characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Output enable propagation delay (high-impedance to low output)	$t_{PD,ZL}$			14	ns	From 50% rising enable (except 4DIR142xHA) to 50% of falling V_{OH} From 50% falling enable (for 4DIR142xHA) to 50% of falling V_{OH}
Default output delay time from input power loss	t_{DO}		0.4	2.6	µs	Measured from $V_{DDIUVLOoff}$ = 2.55 V. Power supply ramp rate = 1 V/µs
Time from UVLO to valid output data	t_{PU}			3	µs	Power supply ramp rate = 1 V/µs, DR > 6.6 Mbps

1) Parameter tested in production
2) The parameter gives the difference in propagation delay between different samples switching in the same direction under same conditions, including same ambient temperature
3) Also known as pulse skew. The parameter gives the maximum difference between on and off propagation delay shown from the same sample over the operating temperature range
4) V_{DDI} = Input-side supply voltage. For input channels on side 1 it is V_{DD1} and for input channels on side 2 it is V_{DD2}

4.7.2 Electrical characteristics - 5 V supply

Typical values are given at T_A = 25 °C, V_{DD1} = V_{DD2} = 5V. Minimum/maximum specifications apply over the entire recommended operation range of V_{DD1} = V_{DD2} = 5 V ± 10%, and -40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching characteristics are tested with C_{LOAD} = 15 pF and 50% duty cycle input square wave, over operating range unless otherwise specified. Supply current values are calculated considering all channels are switching at the same data rate. Parameters are tested in production unless otherwise specified. Only DC supply currents are tested in production and AC supply currents are not tested in production.

4.7.2.1 Logic inputs

Table 22 Logic inputs

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
High-level input current	I_{IH}			10	µA	V_{INX} = V_{DDI} [1] [2]
Low-level input current	I_{IL}	-10			µA	V_{INX} = 0 V [2]
Input voltage threshold for transition LH	V_{I_LH}			0.7V_{DI}	V	
Input voltage threshold for transition HL	V_{I_HL}	0.3V_{DI}			V	
Input voltage threshold hysteresis	V_{I_HYS}	0.1 V_{DI}			V	
Input pull-down resistor	R_{IN}		825		kΩ	V_{INX}=V_{DDI} [1]

1) V_{DDI} = Input-side supply voltage. For input channels on side 1 it is V_{DD1} and for input channels on side 2 it is V_{DD2}
2) Parameter not tested in production

4.7.2.2 Logic outputs

Table 23 Logic outputs

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
High-level output voltage	V_{OH}	V_{DDO} - 0.4			V	I_{OH} = 4 mA [1]
Low-level output voltage	V_{OL}			0.4	V	I_{OL} = -4 mA

1) V_{DDO} - Output-side supply voltage. For output buffers on side 1 it is V_{DD1} and for output buffers on side 2 it is V_{DD2}

4.7.2.3 Power supply - 4DIR040xHA (4+0)

Table 24 Power supply - 4DIR040xHA (4+0)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Supply current - DC input	I_{DD1}			3.1	mA	$V_{INx} = V_{DDI}$ [1)]
Supply current - DC input	I_{DD2}			1.85	mA	$V_{INx} = V_{DDI}$ [1)]
Supply current - DC input	I_{DD1}			3.1	mA	V_{INx} = 0 V
Supply current - DC input	I_{DD2}			1.85	mA	V_{INx} = 0 V
Supply current - AC input	I_{DD1_1Mb}			3.9	mA	*DR* = 1 Mbps
Supply current - AC input	I_{DD2_1Mb}			2.1	mA	*DR* = 1 Mbps
Supply current - AC input	I_{DD1_10Mb}			9.5	mA	*DR* = 10 Mbps
Supply current - AC input	I_{DD2_10Mb}			4.2	mA	*DR* = 10 Mbps
Supply current - AC input	I_{DD1_20Mb}			17	mA	*DR* = 20 Mbps
Supply current - AC input	I_{DD2_20Mb}			6.5	mA	*DR* = 20 Mbps
Supply current - AC input	I_{DD1_40Mb}			32	mA	*DR* = 40 Mbps
Supply current - AC input	I_{DD2_40Mb}			11.5	mA	*DR* = 40 Mbps

1) V_{DDI} = Input-side supply voltage. For input channels on side 1 it is V_{DD1} and for input channels on side 2 it is V_{DD2}

4.7.2.4 Power supply - 4DIR140xHA (3+1)

Table 25 Power supply - 4DIR140xHA (3+1)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Supply current - DC input	I_{DD1}			2.9	mA	$V_{INx} = V_{DDI}$ [1]
Supply current - DC input	I_{DD2}			2.3	mA	$V_{INx} = V_{DDI}$ [1]
Supply current - DC input	I_{DD1}			2.9	mA	V_{INx} = 0 V
Supply current - DC input	I_{DD2}			2.3	mA	V_{INx} = 0 V
Supply current - AC input	I_{DD1_1Mb}			3.6	mA	*DR* = 1 Mbps
Supply current - AC input	I_{DD2_1Mb}			2.5	mA	*DR* = 1 Mbps
Supply current - AC input	I_{DD1_10Mb}			8.3	mA	*DR* = 10 Mbps
Supply current - AC input	I_{DD2_10Mb}			5.5	mA	*DR* = 10 Mbps
Supply current - AC input	I_{DD1_20Mb}			14.5	mA	*DR* = 20 Mbps
Supply current - AC input	I_{DD2_20Mb}			9.5	mA	*DR* = 20 Mbps
Supply current - AC input	I_{DD1_40Mb}			27	mA	*DR* = 40 Mbps
Supply current - AC input	I_{DD2_40Mb}			16	mA	*DR* = 40 Mbps

1) V_{DDI} = Input-side supply voltage. For input channels on side 1 it is V_{DD1} and for input channels on side 2 it is V_{DD2}

4.7.2.5 Power supply - 4DIR240xHA (2+2)

Table 26 Power supply - 4DIR240xHA (2+2)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Supply current - DC input	I_{DD1}			2.65	mA	$V_{INx} = V_{DDI}$ [1)]
Supply current - DC input	I_{DD2}			2.65	mA	$V_{INx} = V_{DDI}$ [1)]
Supply current - DC input	I_{DD1}			2.65	mA	V_{INx} = 0 V
Supply current - DC input	I_{DD2}			2.65	mA	V_{INx} = 0 V
Supply current - AC input	I_{DD1_1Mb}			3.3	mA	*DR* = 1 Mbps
Supply current - AC input	I_{DD2_1Mb}			3.3	mA	*DR* = 1 Mbps
Supply current - AC input	I_{DD1_10Mb}			7.5	mA	*DR* = 10 Mbps
Supply current - AC input	I_{DD2_10Mb}			7	mA	*DR* = 10 Mbps
Supply current - AC input	I_{DD1_20Mb}			13	mA	*DR* = 20 Mbps
Supply current - AC input	I_{DD2_20Mb}			12	mA	*DR* = 20 Mbps
Supply current - AC input	I_{DD1_40Mb}			23	mA	*DR* = 40 Mbps
Supply current - AC input	I_{DD2_40Mb}			21	mA	*DR* = 40 Mbps

1) V_{DDI} = Input-side supply voltage. For input channels on side 1 it is V_{DD1} and for input channels on side 2 it is V_{DD2}

4.7.2.6 Power supply - 4DIR142xHA (3+1 EN1 neg.)

Table 27 Power supply - 4DIR142xHA (3+1 EN1 neg.)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Supply current - DC input	I_{DD1}			2.9	mA	$V_{INx} = V_{DDI}$ [1]
Supply current - DC input	I_{DD2}			2.3	mA	$V_{INx} = V_{DDI}$ [1]
Supply current - DC input	I_{DD1}			2.9	mA	V_{INx} = 0 V
Supply current - DC input	I_{DD2}			2.3	mA	V_{INx} = 0 V
Supply current - AC input	I_{DD1_1Mb}			3.6	mA	DR = 1 Mbps
Supply current - AC input	I_{DD2_1Mb}			2.5	mA	DR = 1 Mbps
Supply current - AC input	I_{DD1_10Mb}			8.3	mA	DR = 10 Mbps
Supply current - AC input	I_{DD2_10Mb}			5.5	mA	DR = 10 Mbps
Supply current - AC input	I_{DD1_20Mb}			14.5	mA	DR = 20 Mbps
Supply current - AC input	I_{DD2_20Mb}			9.5	mA	DR = 20 Mbps
Supply current - AC input	I_{DD1_40Mb}			27	mA	DR = 40 Mbps
Supply current - AC input	I_{DD2_40Mb}			16	mA	DR = 40 Mbps

1) V_{DDI} = Input-side supply voltage. For input channels on side 1 it is V_{DD1} and for input channels on side 2 it is V_{DD2}

4.7.2.7 Dynamic characteristics

Table 28 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
INx to OUTx turn-on propagation delay	t_{PDon}	21	26	32	ns	From 50% level of rising input to 50% level of corresponding rising output
INx to OUTx turn-off propagation delay	t_{PDoff}	21	26	32	ns	From 50% level of falling input to 50% level of corresponding falling output
Part-to-part propagation delays mismatch	$\Delta t_{PD,p\text{-}p}$			6	ns	1)
Co-directional channel-to-channel propagation delay mismatch	$\Delta t_{PD,Ch\text{-}Ch}$			3	ns	Within same sample, over operating temperature range, same direction channels, switching in the same direction
Opposing directional channel-to-channel propagation delay mismatch	$\Delta t_{PD,Ch\text{-}Ch}$			3	ns	Within same sample, over operating temperature range, opposing directional channels, switching with the same signal level
Pulse width distortion	*PWD*			3	ns	$\lvert t_{PDoff}\text{-}t_{PDon}\rvert$ 2)
Input pulse width that changes output state	$t_{pw,min}$	8.5	12.5	15	ns	Measured with full range of input signal $V_{IN} = V_{DDI}$ 3)
Output signal rise time	t_{rise}			3.5	ns	10% to 90% rising output, C_{LOAD} = 15 pF 4)
Output signal fall time	t_{fall}			3.5	ns	90% to 10% falling output, C_{LOAD} = 15 pF 4)
Output disable propagation delay (high output to high-impedance)	$t_{PD,HZ}$			11	ns	From 50% falling enable (except 4DIR142xHA) to V_{OH} - 0.5 V From 50% rising enable (for 4DIR142xHA) to V_{OH} - 0.5 V 4)
Output disable propagation delay (low output to high-impedance)	$t_{PD,LZ}$			10	ns	From 50% of falling enable (except 4DIR142xHA) to V_{OL} + 0.5 V From 50% of rising enable (for 4DIR142xHA) to V_{OL} + 0.5 V 4)
Output enable propagation delay (high-impedance to high output)	$t_{PD,ZH}$			14	ns	From 50% rising enable (except 4DIR142xHA) to 50% of rising V_{OH} From 50% falling enable (for 4DIR142xHA) to 50% of rising V_{OH} 4)

(table continues...)

Table 28 (continued) Dynamic characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Output enable propagation delay (high-impedance to low output)	$t_{PD,ZL}$			13	ns	From 50% of rising enable (except 4DIR142xHA) to 50% of falling V_{OH} From 50% of falling enable (for 4DIR142xHA) to 50% of falling V_{OH} 4)
Default output delay time from input power loss	t_{DO}		0.4	2.6	µs	Measured from $V_{DDIUVLOoff}$ = 2.55 V. Power supply ramp rate = 1 V/µs
Time from UVLO to valid output data	t_{PU}			3	µs	Power supply ramp rate = 1 V/µs, DR > 6.6 Mbps 4)

1) The parameter gives the difference in propagation delay between different samples switching in the same direction under same conditions, including same ambient temperature
2) Also known as pulse skew. The parameter gives the maximum difference between on and off propagation delay shown from the same sample over the operating temperature range
3) V_{DDI} = Input-side supply voltage. For input channels on side 1 it is V_{DD1} and for input channels on side 2 it is V_{DD2}
4) Parameter not tested in production

4.7.3 Electrical characteristics - 3.3 V supply

Typical values are given at T_A = 25 °C, V_{DD1} = V_{DD2} = 3.3V. Minimum/maximum specifications apply over the entire recommended operation range of V_{DD1} = V_{DD2} = 3.3 V ± 10%, and -40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching characteristics are tested with C_{LOAD} = 15 pF and 50% duty cycle input square wave, over operating range unless otherwise specified. Supply current values are calculated considering all channels are switching at the same data rate. Parameters are tested in production unless otherwise specified. Only DC supply currents are tested in production and AC supply currents are not tested in production.

4.7.3.1 Logic inputs

Table 29 Logic inputs

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
High-level input current	I_{IH}			10	µA	V_{INX} = V_{DDI} 1) 2)
Low-level input current	I_{IL}	-10			µA	V_{INX} = 0 V 2)
Input voltage threshold for transition LH	V_{I_LH}			0.7V_{DI}	V	
Input voltage threshold for transition HL	V_{I_HL}	0.3V_{DI}			V	
Input voltage threshold hysteresis	V_{I_HYS}	0.1 V_{DI}			V	
Input pull-down resistor	R_{IN}		825		kΩ	V_{INX}=V_{DDI} 1) 2)

1) V_{DDI} = Input-side supply voltage. For input channels on side 1 it is V_{DD1} and for input channels on side 2 it is V_{DD2}
2) Parameter not tested in production

4.7.3.2 Logic outputs

Table 30 Logic outputs

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
High-level output voltage	V_{OH}	V_{DDO} - 0.3			V	I_{OH} = 2 mA 1)
Low-level output voltage	V_{OL}			0.3	V	I_{OL} = -2 mA

1) V_{DDO} - Output-side supply voltage. For output buffers on side 1 it is V_{DD1} and for output buffers on side 2 it is V_{DD2}

4.7.3.3 Power supply - 4DIR040xHA (4+0)

Table 31 Power supply - 4DIR040xHA (4+0)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Supply current - DC input	I_{DD1}			3.05	mA	$V_{INx} = V_{DDI}$ [1)]
Supply current - DC input	I_{DD2}			1.8	mA	$V_{INx} = V_{DDI}$ [1)]
Supply current - DC input	I_{DD1}			3.05	mA	V_{INx} = 0 V
Supply current - DC input	I_{DD2}			1.8	mA	V_{INx} = 0 V
Supply current - AC input	I_{DD1_1Mb}			3.8	mA	*DR* = 1 Mbps
Supply current - AC input	I_{DD2_1Mb}			2	mA	*DR* = 1 Mbps
Supply current - AC input	I_{DD1_10Mb}			9.2	mA	*DR* = 10 Mbps
Supply current - AC input	I_{DD2_10Mb}			3.6	mA	*DR* = 10 Mbps
Supply current - AC input	I_{DD1_20Mb}			16	mA	*DR* = 20 Mbps
Supply current - AC input	I_{DD2_20Mb}			5.5	mA	*DR* = 20 Mbps
Supply current - AC input	I_{DD1_40Mb}			32	mA	*DR* = 40 Mbps
Supply current - AC input	I_{DD2_40Mb}			9	mA	*DR* = 40 Mbps

1) V_{DDI} - Input-side supply voltage. For input channels on side 1 it is V_{DD1} and for input channels on side 2 it is V_{DD2}

4.7.3.4 Power supply - 4DIR140xHA (3+1)

Table 32 Power supply - 4DIR140xHA (3+1)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Supply current - DC input	I_{DD1}			2.85	mA	$V_{INx} = V_{DDI}$ [1)]
Supply current - DC input	I_{DD2}			2.25	mA	$V_{INx} = V_{DDI}$ [1)]
Supply current - DC input	I_{DD1}			2.85	mA	V_{INx} = 0 V
Supply current - DC input	I_{DD2}			2.25	mA	V_{INx} = 0 V
Supply current - AC input	I_{DD1_1Mb}			3.5	mA	*DR* = 1 Mbps
Supply current - AC input	I_{DD2_1Mb}			2.4	mA	*DR* = 1 Mbps
Supply current - AC input	I_{DD1_10Mb}			8.1	mA	*DR* = 10 Mbps
Supply current - AC input	I_{DD2_10Mb}			5	mA	*DR* = 10 Mbps
Supply current - AC input	I_{DD1_20Mb}			14	mA	*DR* = 20 Mbps
Supply current - AC input	I_{DD2_20Mb}			8	mA	*DR* = 20 Mbps
Supply current - AC input	I_{DD1_40Mb}			26	mA	*DR* = 40 Mbps
Supply current - AC input	I_{DD2_40Mb}			14	mA	*DR* = 40 Mbps

1) V_{DDI} - Input-side supply voltage. For input channels on side 1 it is V_{DD1} and for input channels on side 2 it is V_{DD2}

4.7.3.5 Power supply - 4DIR240xHA (2+2)

Table 33 Power supply - 4DIR240xHA (2+2)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Supply current - DC input	I_{DD1}			2.6	mA	$V_{INx} = V_{DDI}$ [1)]
Supply current - DC input	I_{DD2}			2.6	mA	$V_{INx} = V_{DDI}$ [1)]
Supply current - DC input	I_{DD1}			2.6	mA	V_{INx} = 0 V
Supply current - DC input	I_{DD2}			2.6	mA	V_{INx} = 0 V
Supply current - AC input	I_{DD1_1Mb}			3.2	mA	*DR* = 1 Mbps
Supply current - AC input	I_{DD2_1Mb}			3.2	mA	*DR* = 1 Mbps
Supply current - AC input	I_{DD1_10Mb}			7	mA	*DR* = 10 Mbps
Supply current - AC input	I_{DD2_10Mb}			6.5	mA	*DR* = 10 Mbps
Supply current - AC input	I_{DD1_20Mb}			12	mA	*DR* = 20 Mbps
Supply current - AC input	I_{DD2_20Mb}			11	mA	*DR* = 20 Mbps
Supply current - AC input	I_{DD1_40Mb}			21	mA	*DR* = 40 Mbps
Supply current - AC input	I_{DD2_40Mb}			19	mA	*DR* = 40 Mbps

1) V_{DDI} - Input-side supply voltage. For input channels on side 1 it is V_{DD1} and for input channels on side 2 it is V_{DD2}

4.7.3.6 Power supply - 4DIR142xHA (3+1 EN1 neg.)

Table 34 Power supply - 4DIR142xHA (3+1 EN1 neg.)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Supply current - DC input	I_{DD1}			2.85	mA	$V_{INx} = V_{DDI}$ [1)]
Supply current - DC input	I_{DD2}			2.25	mA	$V_{INx} = V_{DDI}$ [1)]
Supply current - DC input	I_{DD1}			2.85	mA	V_{INx} = 0 V
Supply current - DC input	I_{DD2}			2.25	mA	V_{INx} = 0 V
Supply current - AC input	I_{DD1_1Mb}			3.5	mA	*DR* = 1 Mbps
Supply current - AC input	I_{DD2_1Mb}			2.4	mA	*DR* = 1 Mbps
Supply current - AC input	I_{DD1_10Mb}			8.1	mA	*DR* = 10 Mbps
Supply current - AC input	I_{DD2_10Mb}			5	mA	*DR* = 10 Mbps
Supply current - AC input	I_{DD1_20Mb}			14	mA	*DR* = 20 Mbps
Supply current - AC input	I_{DD2_20Mb}			8	mA	*DR* = 20 Mbps
Supply current - AC input	I_{DD1_40Mb}			26	mA	*DR* = 40 Mbps
Supply current - AC input	I_{DD2_40Mb}			14	mA	*DR* = 40 Mbps

1) V_{DDI} - Input-side supply voltage. For input channels on side 1 it is V_{DD1} and for input channels on side 2 it is V_{DD2}

4.7.3.7 Dynamic characteristics

Table 35 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
INx to OUTx turn-on propagation delay	t_{PDon}	21	26	32	ns	From 50% level of rising input to 50% level of rising output
INx to OUTx turn-off propagation delay	t_{PDoff}	21	26	32	ns	From 50% level of falling input to 50% level of falling output
Part-to-part propagation delays mismatch	$\Delta t_{PD,p\text{-}p}$			6	ns	[1]
Co-directional channel-to-channel propagation delay mismatch	$\Delta t_{PD,Ch\text{-}Ch}$			3	ns	Within same sample, over operating temperature range, same direction channels, switching in the same direction
Opposing directional channel-to-channel propagation delay mismatch	$\Delta t_{PD,Ch\text{-}Ch}$			3	ns	Within same sample, over operating temperature range, opposing directional channels, switching with the same signal level.
Pulse width distortion	*PWD*			3	ns	$\lvert t_{PDoff}\text{-}t_{PDon}\rvert$ [2]
Input pulse width that changes output state	$t_{pw,min}$	9	12.5	15	ns	Measured with full range of input signal $V_{IN} = V_{DDI}$ [3]
Output signal rise time	t_{rise}			3.5	ns	10% to 90% rising output, C_{LOAD} = 15 pF [4]
Output signal fall time	t_{fall}			3.5	ns	90% to 10% falling output, C_{LOAD} = 15 pF [4]
Output disable propagation delay (high output to high-impedance)	$t_{PD,HZ}$			13	ns	From 50% falling enable (except 4DIR142xHA) to V_{OH} - 0.5 V From 50% rising enable (for 4DIR142xHA) to V_{OH} - 0.5 V [4]
Output disable propagation delay (low output to high-impedance)	$t_{PD,LZ}$			12	ns	From 50% of falling enable (except 4DIR142xHA) to V_{OL} + 0.5 V From 50% of rising enable (for 4DIR142xHA) to V_{OL} + 0.5 V [4]
Output enable propagation delay (high-impedance to high output)	$t_{PD,ZH}$			14	ns	From 50% rising enable (except 4DIR142xHA) to 50% of rising V_{OH} From 50% falling enable (for 4DIR142xHA) to 50% of rising V_{OH} [4]

(table continues...)

Table 35 (continued) Dynamic characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Output enable propagation delay (high-impedance to low output)	$t_{PD,ZL}$			13	ns	From 50% of rising enable (except 4DIR142xHA) to 50% of falling V_{OH} From 50% of falling enable (for 4DIR142xHA) to 50% of falling V_{OH} 4)
Default output delay time from input power loss	t_{DO}		0.4	2.6	µs	Measured from $V_{DDIUVLOoff}$ = 2.55 V. Power supply ramp rate = 1 V/µs
Time from UVLO to valid output data	t_{PU}			3	µs	Power supply ramp rate = 1 V/µs, DR > 6.6 Mbps 4)

1) The parameter gives the difference in propagation delay between different samples switching in the same direction under same conditions, including same ambient temperature
2) Also known as pulse skew. The parameter gives the maximum difference between on and off propagation delay shown from the same sample over the operating temperature range
3) V_{DDI} - Input-side supply voltage. For input channels on side 1 it is V_{DD1} and for input channels on side 2 it is V_{DD2}
4) Parameter not tested in production

4.7.4 Electrical characteristics - 2.7 V supply

Typical values are given at T_A = 25 °C with V_{DD1} = V_{DD2} = 2.7 V. Minimum/maximum specifications apply over the entire recommended operation range of V_{DD1} = V_{DD2} = 2.7 V, and -40°C ≤ T_A ≤ 125°C, unless otherwise noted. Switching characteristics are tested with C_{LOAD} = 15 pF and 50% duty-cycle input square wave, over operating range unless otherwise specified. Supply current values are specified considering that all channels are switching at the same data rate. Parameters are not tested in production unless otherwise specified.

4.7.4.1 Logic inputs

Table 36 Logic inputs

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
High-level input current	I_{IH}			10	µA	V_{INX} = V_{DDI} [1]
Low-level input current	I_{IL}	-10			µA	V_{INX} = 0 V
Input voltage threshold for transition LH	V_{I_LH}			0.7 V_{DDI}	V	
Input voltage threshold for transition HL	V_{I_HL}	0.3 V_{DDI}			V	
Input voltage threshold hysteresis	V_{I_HYS}	0.1 V_{DDI}			V	
Input pull-down resistor	R_{IN}		825		kΩ	V_{INX}=V_{DDI} [1]

1) V_{DDI} = Input-side supply voltage. For input channels on side 1 it is V_{DD1} and for input channels on side 2 it is V_{DD2}

4.7.4.2 Logic outputs

Table 37 Logic outputs

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
High-level output voltage	V_{OH}	V_{DDO} - 0.3			V	I_{OH} = 1 mA [1]
Low-level output voltage	V_{OL}			0.3	V	I_{OL} = -1 mA

1) V_{DDO} - Output-side supply voltage. For output buffers on side 1 it is V_{DD1} and for output buffers on side 2 it is V_{DD2}

4.7.4.3 Power supply - 4DIR040xHA (4+0)

Table 38 Power supply - 4DIR040xHA (4+0)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Supply current - DC input	I_{DD1}			3	mA	$V_{INx} = V_{DDI}$ [1)]
Supply current - DC input	I_{DD2}			1.75	mA	$V_{INx} = V_{DDI}$ [1)]
Supply current - DC input	I_{DD1}			3	mA	V_{INx} = 0 V
Supply current - DC input	I_{DD2}			1.75	mA	V_{INx} = 0 V
Supply current - AC input	I_{DD1_1Mb}			3.75	mA	*DR* = 1 Mbps
Supply current - AC input	I_{DD2_1Mb}			1.95	mA	*DR* = 1 Mbps
Supply current - AC input	I_{DD1_10Mb}			9.2	mA	*DR* = 10 Mbps
Supply current - AC input	I_{DD2_10Mb}			3.5	mA	*DR* = 10 Mbps
Supply current - AC input	I_{DD1_20Mb}			16	mA	*DR* = 20 Mbps
Supply current - AC input	I_{DD2_20Mb}			5	mA	*DR* = 20 Mbps
Supply current - AC input	I_{DD1_40Mb}			32	mA	*DR* = 40 Mbps
Supply current - AC input	I_{DD2_40Mb}			8	mA	*DR* = 40 Mbps

1) V_{DDI} = Input-side supply voltage. For input channels on side 1 it is V_{DD1} and for input channels on side 2 it is V_{DD2}

4.7.4.4 Power supply - 4DIR140xHA (3+1)

Table 39 Power supply - 4DIR140xHA (3+1)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Supply current - DC input	I_{DD1}			2.8	mA	$V_{INx} = V_{DDI}$ [1)]
Supply current - DC input	I_{DD2}			2.2	mA	$V_{INx} = V_{DDI}$ [1)]
Supply current - DC input	I_{DD1}			2.8	mA	V_{INx} = 0 V
Supply current - DC input	I_{DD2}			2.2	mA	V_{INx} = 0 V
Supply current - AC input	I_{DD1_1Mb}			3.5	mA	*DR* = 1 Mbps
Supply current - AC input	I_{DD2_1Mb}			2.4	mA	*DR* = 1 Mbps
Supply current - AC input	I_{DD1_10Mb}			8	mA	*DR* = 10 Mbps
Supply current - AC input	I_{DD2_10Mb}			5	mA	*DR* = 10 Mbps
Supply current - AC input	I_{DD1_20Mb}			13.8	mA	*DR* = 20 Mbps
Supply current - AC input	I_{DD2_20Mb}			7.6	mA	*DR* = 20 Mbps
Supply current - AC input	I_{DD1_40Mb}			26	mA	*DR* = 40 Mbps
Supply current - AC input	I_{DD2_40Mb}			13	mA	*DR* = 40 Mbps

1) V_{DDI} = Input-side supply voltage. For input channels on side 1 it is V_{DD1} and for input channels on side 2 it is V_{DD2}

4.7.4.5 Power supply - 4DIR240xHA (2+2)

Table 40 Power supply - 4DIR240xHA (2+2)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Supply current - DC input	I_{DD1}			2.6	mA	$V_{INx} = V_{DDI}$ [1)]
Supply current - DC input	I_{DD2}			2.6	mA	$V_{INx} = V_{DDI}$ [1)]
Supply current - DC input	I_{DD1}			2.6	mA	V_{INx} = 0 V
Supply current - DC input	I_{DD2}			2.6	mA	V_{INx} = 0 V
Supply current - AC input	I_{DD1_1Mb}			3.2	mA	*DR* = 1 Mbps
Supply current - AC input	I_{DD2_1Mb}			3.2	mA	*DR* = 1 Mbps
Supply current - AC input	I_{DD1_10Mb}			7	mA	*DR* = 10 Mbps
Supply current - AC input	I_{DD2_10Mb}			6.5	mA	*DR* = 10 Mbps
Supply current - AC input	I_{DD1_20Mb}			12	mA	*DR* = 20 Mbps
Supply current - AC input	I_{DD2_20Mb}			11	mA	*DR* = 20 Mbps
Supply current - AC input	I_{DD1_40Mb}			21	mA	*DR* = 40 Mbps
Supply current - AC input	I_{DD2_40Mb}			19	mA	*DR* = 40 Mbps

1) V_{DDI} = Input-side supply voltage. For input channels on side 1 it is V_{DD1} and for input channels on side 2 it is V_{DD2}

4.7.4.6 Power supply - 4DIR142xHA (3+1 EN1 neg.)

Table 41 Power supply - 4DIR142xHA (3+1 EN1 neg.)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Supply current - DC input	I_{DD1}			2.8	mA	$V_{INx} = V_{DDI}$ [1]
Supply current - DC input	I_{DD2}			2.2	mA	$V_{INx} = V_{DDI}$ [1]
Supply current - DC input	I_{DD1}			2.8	mA	V_{INx} = 0 V
Supply current - DC input	I_{DD2}			2.2	mA	V_{INx} = 0 V
Supply current - AC input	I_{DD1_1Mb}			3.5	mA	*DR* = 1 Mbps
Supply current - AC input	I_{DD2_1Mb}			2.4	mA	*DR* = 1 Mbps
Supply current - AC input	I_{DD1_10Mb}			8	mA	*DR* = 10 Mbps
Supply current - AC input	I_{DD2_10Mb}			5	mA	*DR* = 10 Mbps
Supply current - AC input	I_{DD1_20Mb}			13.8	mA	*DR* = 20 Mbps
Supply current - AC input	I_{DD2_20Mb}			7.6	mA	*DR* = 20 Mbps
Supply current - AC input	I_{DD1_40Mb}			26	mA	*DR* = 40 Mbps
Supply current - AC input	I_{DD2_40Mb}			13	mA	*DR* = 40 Mbps

1) V_{DDI} = Input-side supply voltage. For input channels on side 1 it is V_{DD1} and for input channels on side 2 it is V_{DD2}

4.7.4.7 Dynamic characteristics

Table 42 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
INx to OUTx turn-on propagation delay	t_{PDon}	20	26	33	ns	From 50% level of rising input to 50% level of corresponding rising output [1]
INx to OUTx turn-off propagation delay	t_{PDoff}	20	26	33	ns	From 50% level of falling input to 50% level of corresponding falling output [1]
Part-to-part propagation delays mismatch	$\Delta t_{PD,p\text{-}p}$			6	ns	[1] [2]
Co-directional channel-to-channel propagation delay mismatch	$\Delta t_{PD,Ch\text{-}Ch}$			3	ns	Within same sample, over operating temperature range, same direction channels, switching in the same direction [1]
Opposing directional channel-to-channel propagation delay mismatch	$\Delta t_{PD,Ch\text{-}Ch}$			3	ns	Within same sample, over operating temperature range, opposing directional channels, switching with the same signal level [1]
Pulse width distortion	*PWD*			3.5	ns	$\lvert t_{PDoff}\text{-}t_{PDon}\rvert$ [1] [3]
Input pulse width that changes output state	$t_{pw,min}$	8.5	12.5	16	ns	Measured with full range of input signal $V_{IN} = V_{DDI}$ [1] [4]
Output signal rise time	t_{rise}			3	ns	10% to 90% rising output, C_{LOAD} = 15 pF
Output signal fall time	t_{fall}			3	ns	90% to 10% falling output, C_{LOAD} = 15 pF
Output disable propagation delay (high output to high-impedance)	$t_{PD,HZ}$			13	ns	From 50% falling enable (except 4DIR142xHA) to V_{OH} - 0.5 V From 50% rising enable (for 4DIR142xHA) to V_{OH} - 0.5 V
Output disable propagation delay (low output to high-impedance)	$t_{PD,LZ}$			13	ns	From 50% of falling enable (except 4DIR142xHA) to V_{OL} + 0.5 V From 50% of rising enable (for 4DIR142xHA) to V_{OL} + 0.5 V
Output enable propagation delay (high-impedance to high output)	$t_{PD,ZH}$			14	ns	From 50% rising enable (except 4DIR142xHA) to 50% of rising V_{OH} From 50% falling enable (for 4DIR142xHA) to 50% of rising V_{OH}

(table continues...)

Table 42 (continued) Dynamic characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Output enable propagation delay (high-impedance to low output)	$t_{PD,ZL}$			13	ns	From 50% of rising enable (except 4DIR142xHA) to 50% of falling V_{OH} From 50% of falling enable (for 4DIR142xHA) to 50% of falling V_{OH}
Default output delay time from input power loss	t_{DO}		0.4	2.6	µs	Measured from $V_{DDIUVLOoff}$ = 2.55 V. Power supply ramp rate = 1 V/µs [1]
Time from UVLO to valid output data	t_{PU}			3	µs	Power supply ramp rate = 1 V/µs, DR > 6.6 Mbps

1) Parameter tested in production
2) The parameter gives the difference in propagation delay between different samples switching in the same direction under same conditions, including same ambient temperature
3) Also known as pulse skew. The parameter gives the maximum difference between on and off propagation delay shown from the same sample over the operating temperature range
4) V_{DDI} = Input-side supply voltage. For input channels on side 1 it is V_{DD1} and for input channels on side 2 it is V_{DD2}

4.8 Insulation and safety-related specifications

This coupler is suitable for rated insulation only within the safety limiting values. Compliance with the safety limiting values shall be ensured by means of suitable protective circuits.

4.8.1 Insulation characteristics

Parameter	Symbol	Value	Unit	Note or condition
External clearance	*CLR*	>8	mm	Shortest distance in air from any input pin to any output pin according to IEC 60664-1[1)]
External creepage	*CRP*	>8	mm	Shortest distance over package surface from any input pin to any output pin according to IEC 60664-1[1)]
Comparative tracking index	*CTI*	≥600	V	According to IEC 60112
Material group		I		According to IEC 60112
Pollution degree		2		According to IEC 60664-1
Overvoltage category		I - IV		Rated mains voltage ≤ 150 V_{RMS} According to IEC 60664-1
Overvoltage category		I - IV		Rated mains voltage ≤ 300 V_{RMS} According to IEC 60664-1
Overvoltage category		I - III		Rated mains voltage ≤ 600 V_{RMS} According to IEC 60664-1
Overvoltage category		I-II		Rated mains voltage ≤ 1000 V_{RMS} According to IEC 60664-1
Climatic category		40/125 /21		
Input-to-output isolation according to UL1577 Ed. 5				
Input-to-output isolation voltage	V_{ISO}	5700	V_{rms}	$V_{TEST} = V_{ISO}$ for t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{ISO}$ for t = 1 s (100% productive tests)
Input-to-output isolation according to DIN VDE V 0884-17, IEC 60747-17[2)]				
Maximum rated transient isolation voltage	V_{IOTM}	8000	V_{pk}	$V_{TEST} = V_{IOTM}$ for t_{ini} = 60 s (type test and sample test) $V_{TEST} = 1.2 \times V_{IOTM}$ for t_{ini} = 1 s (routine test)
Maximum Impulse voltage	V_{IMP}	8000	V_{pk}	According to IEC 60664-1, IEC 60747-17
Maximum rated repetitive peak isolation voltage	V_{IORM}	1767	V_{pk}	According to Time Dependent Dielectric Breakdown (TDDB) test

Parameter	Symbol	Value	Unit	Note or condition
Apparent charge	q_{PD}	<5	pC	Method (b1) (routine test and type test pre-conditioning) $V_{PD(ini)} = 1.2 \times V_{IOTM}$ for $t_{ini} = 1$ s $V_{PD(m)} = 1.875 \times V_{IORM}$ for $t_m = 1$ s [3)] Method (a) (type test, subgroup 1 final measurements) $V_{PD(ini)} = V_{IOTM}$ for $t_{ini} = 60$ s $V_{PD(m)} = 1.6 \times V_{IORM}$ for $t_m = 10$ s Method (a) (type test, subgroup 2, 3 final measurements) $V_{PD(ini)} = V_{IOTM}$ for $t_{ini} = 60$ s $V_{PD(m)} = 1.2 \times V_{IORM}$ for $t_m = 10$ s
Maximum surge isolation voltage	V_{IOSM}	10400	V_{pk}	V_{IOSM}= 10.4 $kV_{pk} \geq 1.3 \times V_{IMP}$ for reinforced isolation according to IEC 60747-17 (type test)[4)]
Isolation resistance [6)]	R_{IO}	$>10^{12}$	Ω	V_{IO} = 500 V_{dc} for t = 60 s, T_A = 25°C [5)]
		$>10^{11}$	Ω	V_{IO} = 500 V_{dc} for t = 60 s, T_A = 125°C [5)]
	R_{IO_S}	$>10^{9}$	Ω	V_{IO} = 500 V_{dc} for t = 60 s, $T_A = T_S$ = 150°C [5)]
Isolation capacitance [6)]	C_{IO}	<2	pF	f = 1 MHz[5)]

1) Creepage and clearance requirements depend on the application and related end-equipment isolation standard. Care should be taken to keep the required creepage and clearance value on printed circuit board level.

2) Safety certification planned. The IEC 60747-17 and its German equivalent VDE 0884-17 is the successor of the component standard VDE 0884-11, which will expire in 2023.

3) The partial discharge voltage $V_{PD(m)}$ applied during productive tests is greater (4411 V_{pk} > 1.875 x V_{IORM}) to include the F_4 factor (1.1) that takes into account the maximum deviation of the mains supply voltage from its nominal value as specified by end-equipment standards IEC 60664-1, IEC 62368-1 ($V_{PD(m)} = F_1 \times F_2 \times F_3 \times F_4 \times V_{IORM} = 1.875 \times F_4 \times V_{IORM}$). The F_3 factor (1.25) is also considered for reinforced isolation as specified in IEC 60664-1.

4) The surge test is performed in insulation oil to determine the intrinsic surge immunity of the insulation barrier.

5) The parameters apply to the product converted in a two terminals device with all terminals on side 1 connected together and all terminals on side 2 connected together.

6) Parameter not tested in production.

4.8.2 Safety-limiting values

This coupler is suitable for rated insulation only within the safety limiting values. Compliance with the safety limiting values shall be ensured by means of suitable protective circuits.

Parameter	Symbol	Value	Unit	Note or condition
Maximum ambient safety temperature	T_S	150	°C	
Safety power dissipation	P_S	2.08	W	R_{thJA} = 60 K/W, T_A = 25 °C, T_J = 150 °C
Safety supply current	$I_{S,TOT}$	416	mA	R_{thJA} = 60 K/W, T_A = 25 °C, T_J = 150 °C, V_{DDX} = 5.0 V

4.8.2.1 Thermal derating curve

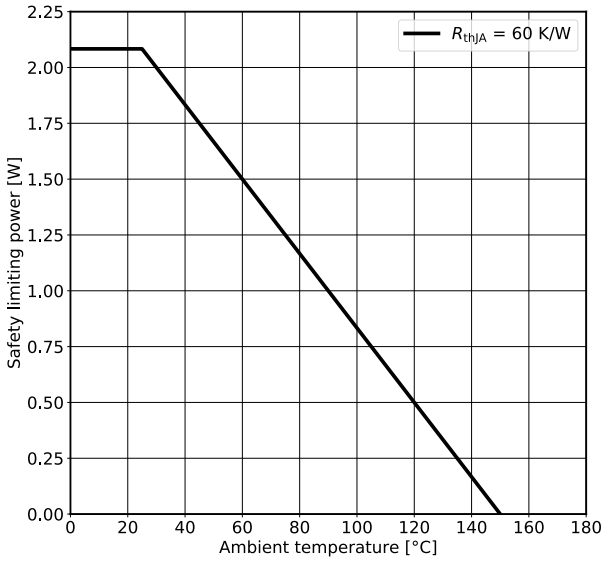

Figure 37 Thermal derating curve

5 Package dimensions

The package dimensions of quad-channel digital isolator are provided.

Package PG-DSO-16 wide-body 300 mil

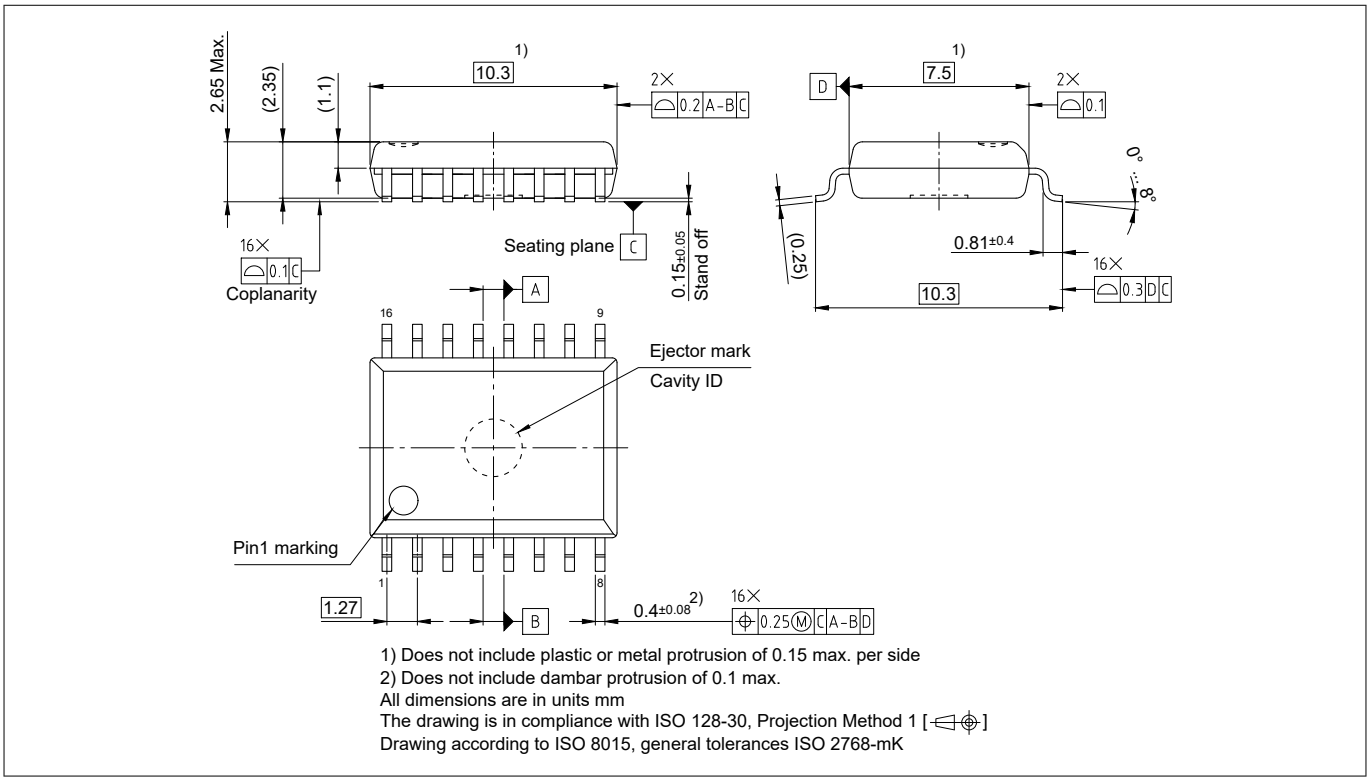

Figure 38 PG-DSO-16 wide-body 300 mil outline

5 Package dimensions

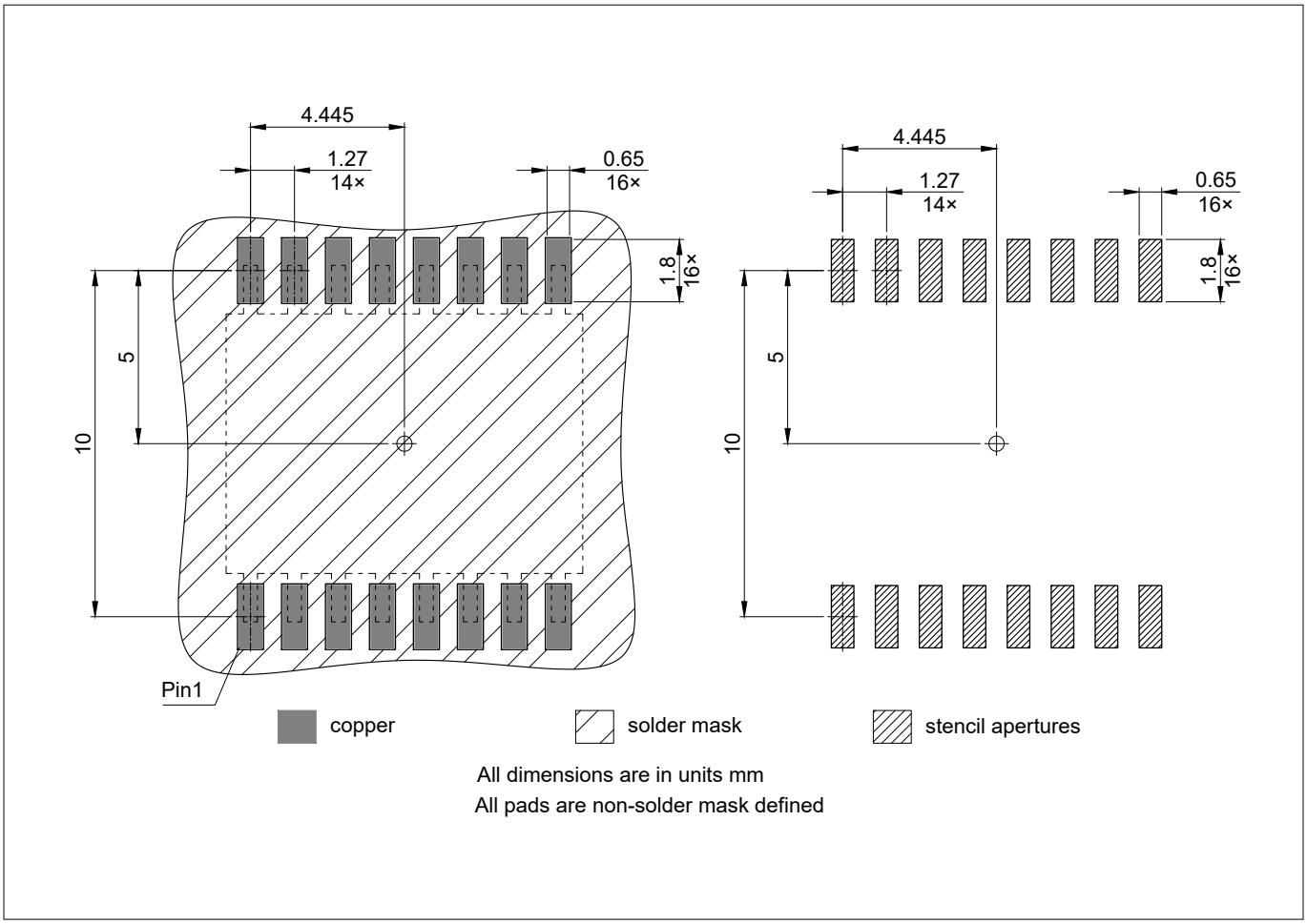

Figure 39 PG-DSO-16 wide-body 300 mil footprint

5 Package dimensions

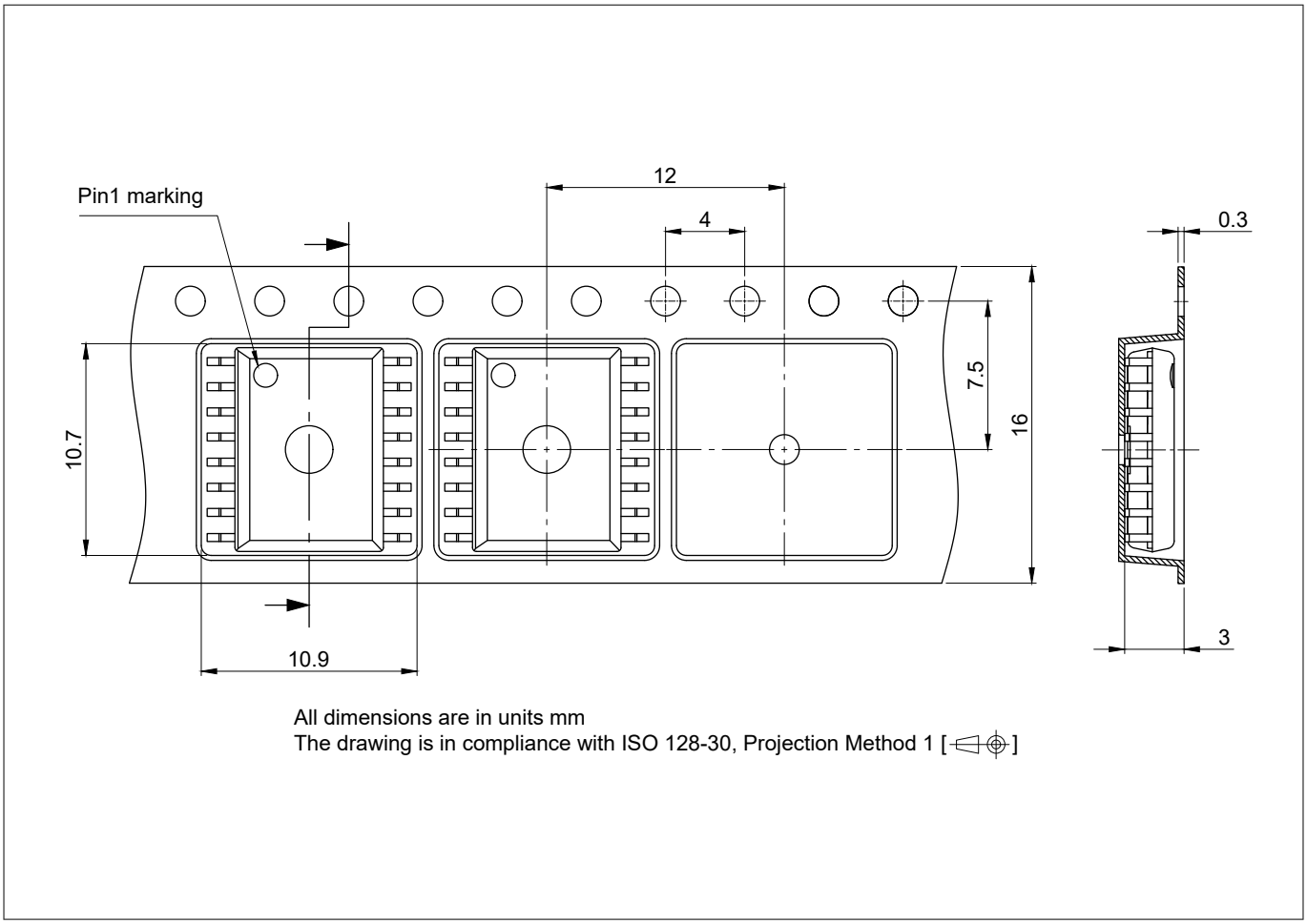

Figure 40 PG-DSO-16 wide-body 300 mil packing

Green product (RoHS-compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations, the device is available as a green product. Green products are RoHS-compliant (i.e they have Pb-free finish on leads and are suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages: https://www.infineon.com/packages

6 Ordering guide

Orderable part number (OPN)	Part number	Channel configuration	Default output state	Output enable	Package marking
4DIR0400HAXUMA1	4DIR0400HA	4 forward 0 reverse (4+0)	Low	Active-high	4R0400AA
4DIR0401HAXUMA1	4DIR0401HA		High		4R0401AA
4DIR1400HAXUMA1	4DIR1400HA	3 forward 1 reverse (3+1)	Low		4R1400AA
4DIR1401HAXUMA1	4DIR1401HA		High		4R1401AA
4DIR2400HAXUMA1	4DIR2400HA	2 forward 2 reverse (2+2)	Low		4R2400AA
4DIR2401HAXUMA1	4DIR2401HA		High		4R2401AA
4DIR1420HAXUMA1	4DIR1420HA	3 forward 1 reverse (3+1)	Low	Active-low[1)]	4R1420AA
4DIR1421HAXUMA1	4DIR1421HA		High		4R1421AA

1) Ideal for shared SPI bus

7 Revision history

Revision number	Major changes since previous revision
V1.7, 2024-07-25	Updated Certification status
V1.6, 2024-04-17	Changed V_{IOSM} from 11000 V_{PK} to 10400 V_{PK}
V1.5, 2024-03-19	Changed V_{IOSM} from 10000 V_{pk} to 11000 V_{pk} and changed V_{IORM} from 1131 V_{pk} to 1767 V_{pk}
V1.3, 2023-12-05	Added 4 forward and 0 reverse (4+0) variant (4DIR040xHA) to the portfolio
V1.2, 2023-11-13	Figure 1 updated
V1.0, 2023-07-26	Datasheet initial release

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Do you have a question about any aspect of this document?

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