

CD74HC137, CD74HCT137, CD54HC237, CD74HC237, CD74HCT237

High-Speed CMOS Logic, 3- to 8-Line Decoder/Demultiplexer with Address Latches

Features

- **Select One of Eight Data Outputs**
 - Active Low for CD74HC137 and CD74HCT137
 - Active High for 'HC237 and CD74HCT237
- **I/O Port or Memory Selector**
- **Two Enable Inputs to Simplify Cascading**
- **Typical Propagation Delay of 13ns at $V_{CC} = 5V$, 15pF, $T_A = 25^\circ C$ (CD74HC237)**
- **Fanout (Over Temperature Range)**
 - Standard Outputs 10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- **Wide Operating Temperature Range . . . $-55^\circ C$ to $125^\circ C$**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
 - 2V to 6V Operation
 - High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$, of V_{CC} at $V_{CC} = 5V$
- **HCT Types**
 - 4.5V to 5.5V Operation
 - Direct LSTTL Input Logic Compatibility, $V_{IL} = 0.8V$ (Max), $V_{IH} = 2V$ (Min)
 - CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL} , V_{OH}

Description

The CD74HC137, CD74HCT137, 'HC237, and CD74HCT237 are high speed silicon gate CMOS decoders well suited to memory address decoding or data routing applications. Both circuits feature low power consumption usually associated with CMOS circuitry, yet have speeds comparable to low power Schottky TTL logic.

Both circuits have three binary select inputs (A_0 , A_1 and A_2) that can be latched by an active High Latch Enable (LE) signal to isolate the outputs from select-input changes. A "Low" LE makes the output transparent to the input and the circuit functions as a one-of-eight decoder. Two Output Enable inputs (\overline{OE}_1 and OE_0) are provided to simplify cascading and to facilitate demultiplexing. The demultiplexing function is accomplished by using the A_0 , A_1 , A_2 inputs to select the desired output and using one of the other Output Enable inputs as the data input while holding the other Output Enable input in its active state. In the CD74HC137 and CD74HCT137 the selected output is a "Low"; in the 'HC237 and CD74HCT237 the selected output is a "High".

Ordering Information

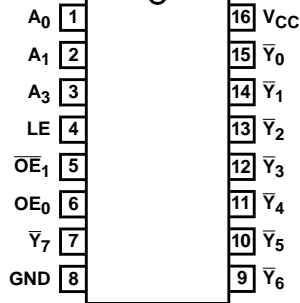
| PART NUMBER | TEMP. RANGE ($^\circ C$) | PACKAGE |
|---------------|-------------------------------|--------------|
| CD54HC237F3A | -55 to 125 | 16 Ld CERDIP |
| CD74HC137E | -55 to 125 | 16 Ld PDIP |
| CD74HC137PW | -55 to 125 | 16 Ld TSSOP |
| CD74HC137PWR | -55 to 125 | 16 Ld TSSOP |
| CD74HC137PWT | -55 to 125 | 16 Ld TSSOP |
| CD74HC237E | -55 to 125 | 16 Ld PDIP |
| CD74HC237M | -55 to 125 | 16 Ld SOIC |
| CD74HC237MT | -55 to 125 | 16 Ld SOIC |
| CD74HC237M96 | -55 to 125 | 16 Ld SOIC |
| CD74HC237NSR | -55 to 125 | 16 Ld SOP |
| CD74HC237PW | -55 to 125 | 16 Ld TSSOP |
| CD74HC237PWR | -55 to 125 | 16 Ld TSSOP |
| CD74HC237PWT | -55 to 125 | 16 Ld TSSOP |
| CD74HCT137E | -55 to 125 | 16 Ld PDIP |
| CD74HCT137MT | -55 to 125 | 16 Ld SOIC |
| CD74HCT137M96 | -55 to 125 | 16 Ld SOIC |
| CD74HCT237E | -55 to 125 | 16 Ld PDIP |

NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.

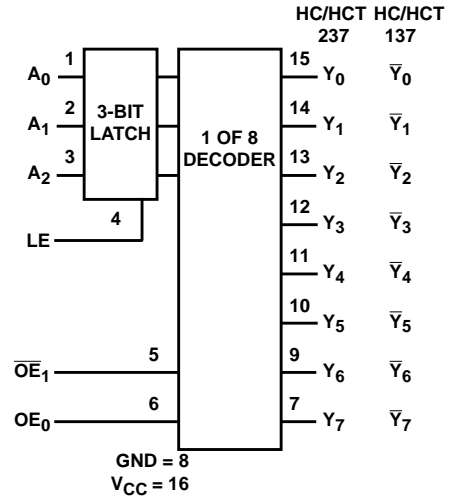
CD74HC137, CD74HCT137, CD54HC237, CD74HC237, CD74HCT237

Pinout

CD54HC237 (CERDIP)
 CD74HC137 (PDIP, TSSOP)
 CD74HCT137 (PDIP, SOIC)
 CD74HC237 (PDIP, SOIC, SOP, TSSOP)
 CD74HCT237 (PDIP)
 TOP VIEW



Functional Diagram



'HC137, 'HCT137 TRUTH TABLE

| INPUTS | | | | | | OUTPUTS | | | | | | | |
|--------|-----------------|-----------------|----------------|----------------|----------------|--|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| LE | OE ₀ | OE ₁ | A ₂ | A ₁ | A ₀ | Y ₀ | Y ₁ | Y ₂ | Y ₃ | Y ₄ | Y ₅ | Y ₆ | Y ₇ |
| X | X | H | X | X | X | H | H | H | H | H | H | H | H |
| X | L | X | X | X | X | H | H | H | H | H | H | H | H |
| L | H | L | L | L | L | L | H | H | H | H | H | H | H |
| L | H | L | L | L | H | H | L | H | H | H | H | H | H |
| L | H | L | L | H | L | H | H | L | H | H | H | H | H |
| L | H | L | L | H | H | H | H | H | L | H | H | H | H |
| L | H | L | H | L | L | H | H | H | H | L | H | H | H |
| L | H | L | H | L | H | H | H | H | H | H | L | H | H |
| L | H | L | H | H | L | H | H | H | H | H | H | L | H |
| L | H | L | H | H | H | H | H | H | H | H | H | H | L |
| H | H | L | X | X | X | Depends upon the address previously applied while LE was at a logic low. | | | | | | | |

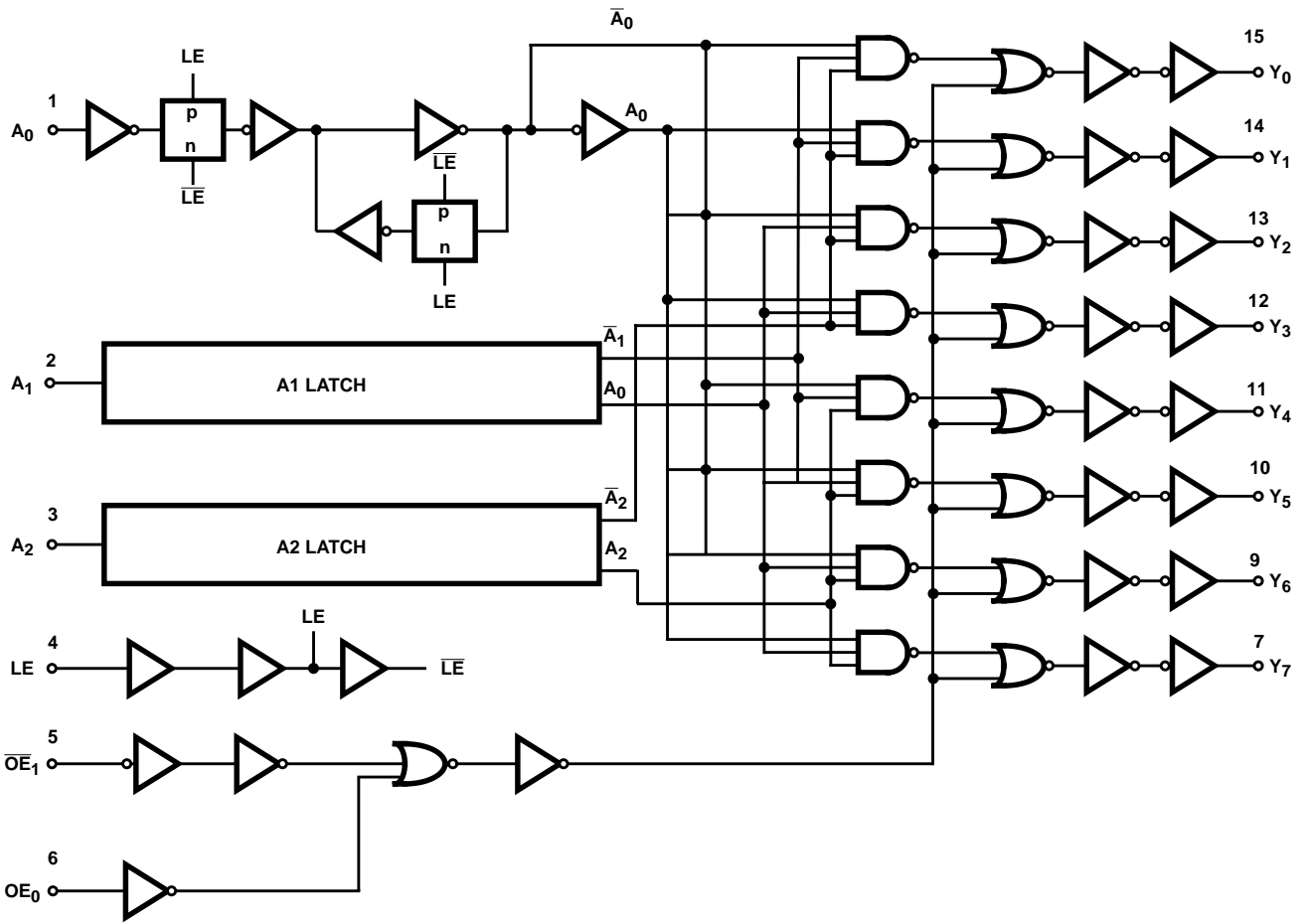
H = High Voltage Level, L = Low Voltage Level, X = Don't Care

'HC237, 'HCT237 TRUTH TABLE

| INPUTS | | | | | | OUTPUTS | | | | | | | |
|--------|-----------------|-----------------|----------------|----------------|----------------|--|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| LE | OE ₀ | OE ₁ | A ₂ | A ₁ | A ₀ | Y ₀ | Y ₁ | Y ₂ | Y ₃ | Y ₄ | Y ₅ | Y ₆ | Y ₇ |
| X | X | H | X | X | X | L | L | L | L | L | L | L | L |
| X | L | X | X | X | X | L | L | L | L | L | L | L | L |
| L | H | L | L | L | L | H | L | L | L | L | L | L | L |
| L | H | L | L | L | H | L | H | L | L | L | L | L | L |
| L | H | L | L | H | L | L | L | L | H | L | L | L | L |
| L | H | L | L | H | H | L | L | L | L | L | L | L | L |
| L | H | L | H | L | L | L | L | L | L | H | L | L | L |
| L | H | L | H | L | H | L | L | L | L | L | H | L | L |
| L | H | L | H | H | L | L | L | L | L | L | L | H | L |
| L | H | L | H | H | H | L | L | L | L | L | L | L | H |
| H | H | L | X | X | X | Depends upon the address previously applied while LE was at a logic low. | | | | | | | |

H = High Voltage Level, L = Low Voltage Level, X = Don't Care

Functional Block Diagram



CD74HC137, CD74HCT137, CD54HC237, CD74HC237, CD74HCT237

Absolute Maximum Ratings

| | |
|--|-------------|
| DC Supply Voltage, V_{CC} | -0.5V to 7V |
| DC Input Diode Current, I_{IK} | |
| For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ | $\pm 20mA$ |
| DC Output Diode Current, I_{OK} | |
| For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ | $\pm 20mA$ |
| DC Output Source or Sink Current per Output Pin, I_O | |
| For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ | $\pm 25mA$ |
| DC V_{CC} or Ground Current, I_{CC} | $\pm 50mA$ |

Thermal Information

| | |
|--|----------------|
| Package Thermal Impedance, θ_{JA} (see Note 1): | |
| E (PDIP) Package | 67°C/W |
| M (SOIC) Package | 73°C/W |
| NS (SOP) Package | 64°C/W |
| PW (TSSOP) Package | 108°C/W |
| Maximum Junction Temperature | 150°C |
| Maximum Storage Temperature Range | -65°C to 150°C |
| Maximum Lead Temperature (Soldering 10s) | 300°C |
| (SOIC - Lead Tips Only) | |

Operating Conditions

| | |
|--|----------------|
| Temperature Range (T_A) | -55°C to 125°C |
| Supply Voltage Range, V_{CC} | |
| HC Types | .2V to 6V |
| HCT Types | 4.5V to 5.5V |
| DC Input or Output Voltage, V_I, V_O | 0V to V_{CC} |
| Input Rise and Fall Time | |
| 2V | 1000ns (Max) |
| 4.5V | 500ns (Max) |
| 6V | 400ns (Max) |

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS | | V_{CC} (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|----------|----------------------|------------|-----------------|------|-----|-----------|---------------|---------|----------------|---------|---------|
| | | V_I (V) | I_O (mA) | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| HC TYPES | | | | | | | | | | | | |
| High Level Input Voltage | V_{IH} | - | - | 2 | 1.5 | - | - | 1.5 | - | 1.5 | - | V |
| | | | | 4.5 | 3.15 | - | - | 3.15 | - | 3.15 | - | V |
| | | | | 6 | 4.2 | - | - | 4.2 | - | 4.2 | - | V |
| Low Level Input Voltage | V_{IL} | - | - | 2 | - | - | 0.5 | - | 0.5 | - | 0.5 | V |
| | | | | 4.5 | - | - | 1.35 | - | 1.35 | - | 1.35 | V |
| | | | | 6 | - | - | 1.8 | - | 1.8 | - | 1.8 | V |
| High Level Output Voltage CMOS Loads | V_{OH} | V_{IH} or V_{IL} | -0.02 | 2 | 1.9 | - | - | 1.9 | - | 1.9 | - | V |
| | | | -0.02 | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| | | | -0.02 | 6 | 5.9 | - | - | 5.9 | - | 5.9 | - | V |
| High Level Output Voltage TTL Loads | V_{OH} | V_{IH} or V_{IL} | - | - | - | - | - | - | - | - | - | V |
| | | | -4 | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V |
| | | | -5.2 | 6 | 5.48 | - | - | 5.34 | - | 5.2 | - | V |
| Low Level Output Voltage CMOS Loads | V_{OL} | V_{IH} or V_{IL} | 0.02 | 2 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.02 | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.02 | 6 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| Low Level Output Voltage TTL Loads | V_{OL} | V_{IH} or V_{IL} | - | - | - | - | - | - | - | - | - | V |
| | | | 4 | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| | | | 5.2 | 6 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current | I_I | V_{CC} or GND | - | 6 | - | - | ± 0.1 | - | ± 1 | - | ± 1 | μA |

CD74HC137, CD74HCT137, CD54HC237, CD74HC237, CD74HCT237

DC Electrical Specifications (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | | V _{CC} (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|--|---------------------------|------------------------------------|---------------------|---------------------|------|-----|------|---------------|------|----------------|-----|-------|
| | | V _I (V) | I _O (mA) | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| Quiescent Device Current | I _{CC} | V _{CC} or GND | 0 | 6 | - | - | 8 | - | 80 | - | 160 | μA |
| HCT TYPES | | | | | | | | | | | | |
| High Level Input Voltage | V _{IH} | - | - | 4.5 to 5.5 | 2 | - | - | 2 | - | 2 | - | V |
| Low Level Input Voltage | V _{IL} | - | - | 4.5 to 5.5 | - | - | 0.8 | - | 0.8 | - | 0.8 | V |
| High Level Output Voltage CMOS Loads | V _{OH} | V _{IH} or V _{IL} | -0.02 | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| High Level Output Voltage TTL Loads | | | -4 | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V |
| Low Level Output Voltage CMOS Loads | V _{OL} | V _{IH} or V _{IL} | 0.02 | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| Low Level Output Voltage TTL Loads | | | 4 | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current | I _I | V _{CC} and GND | 0 | 5.5 | - | - | ±0.1 | - | ±1 | - | ±1 | μA |
| Quiescent Device Current | I _{CC} | V _{CC} or GND | 0 | 5.5 | - | - | 8 | - | 80 | - | 160 | μA |
| Additional Quiescent Device Current Per Input Pin: 1 Unit Load | ΔI _{CC} (Note 2) | V _{CC} -2.1 | - | 4.5 to 5.5 | - | 100 | 360 | - | 450 | - | 490 | μA |

NOTE:

- For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

| INPUT | UNIT LOADS |
|-------|------------|
| All | 1.5 |

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Table, e.g., 360μA max at 25°C.

Prerequisite For Switching Specifications

| PARAMETER | SYMBOL | V _{CC} (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---------------------------------|-----------------|---------------------|------|-----|-----|---------------|-----|----------------|-----|-------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| HC TYPES | | | | | | | | | | |
| A _n to LE Setup Time | t _{SU} | 2 | 50 | - | - | 65 | - | 75 | - | ns |
| | | 4.5 | 10 | - | - | 13 | - | 15 | - | ns |
| | | 6 | 9 | - | - | 11 | - | 13 | - | ns |
| A _n to LE Hold Time | t _H | 2 | 30 | - | - | 40 | - | 45 | - | ns |
| | | 4.5 | 6 | - | - | 8 | - | 9 | - | ns |
| | | 6 | 5 | - | - | 7 | - | 8 | - | ns |

CD74HC137, CD74HCT137, CD54HC237, CD74HC237, CD74HCT237

Prerequisite For Switching Specifications (Continued)

| PARAMETER | SYMBOL | V _{CC} (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---------------------|-----------------|---------------------|------|-----|-----|---------------|-----|----------------|-----|-------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| LE Pulse Width | t _W | 2 | 50 | - | - | 65 | - | 75 | - | ns |
| | | 4.5 | 10 | - | - | 13 | - | 15 | - | ns |
| | | 6 | 9 | - | - | 1 | - | 13 | - | ns |
| HCT TYPES | | | | | | | | | | |
| An to LE Setup Time | t _{SU} | 4.5 | 10 | - | - | 13 | - | 15 | - | ns |
| An to LE Hold Time | t _H | 4.5 | 7 | - | - | 9 | - | 11 | - | ns |
| CD74HCT137 | | | | | | | | | | |
| CD74HCT237 | t _H | 4.5 | 5 | - | - | 5 | - | 5 | - | ns |
| LE Pulse Width | t _W | 4.5 | 10 | - | - | 13 | - | 15 | - | ns |

Switching Specifications Input t_r, t_f = 6ns

| PARAMETER | SYMBOL | TEST CONDITIONS | V _{CC} (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|-------------------------------------|-----------------------|---------------------|------|-----|-----|---------------|-----|----------------|-----|-------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| HC TYPES | | | | | | | | | | | |
| Propagation Delay CD74HC137, CD74HCT137 An to any \bar{Y} | t _{PLH} , t _{PHL} | C _L = 50pF | 2 | - | - | 180 | - | 225 | - | 270 | ns |
| | | | 4.5 | - | - | 36 | - | 45 | - | 54 | ns |
| | | | 6 | - | - | 31 | - | 38 | - | 46 | ns |
| Propagation Delay 'HC237, CD74HCT237 An to any Y | t _{PLH} , t _{PHL} | C _L = 50pF | 2 | - | - | 160 | - | 200 | - | 240 | ns |
| | | | 4.5 | - | - | 32 | - | 40 | - | 48 | ns |
| | | | 6 | - | - | 27 | - | 34 | - | 41 | ns |
| Address to Output CD74HC137 | t _{PLH} , t _{PHL} | C _L = 15pF | 5 | 5 | 15 | - | - | - | - | ns | |
| 'HC237 | t _{PLH} , t _{PHL} | C _L = 15pF | 5 | - | 13 | - | - | - | - | ns | |
| OE ₀ to any \bar{Y} or Y | t _{PLH} , t _{PHL} | C _L = 50pF | 2 | - | - | 145 | - | 180 | - | 220 | ns |
| | | | 4.5 | - | - | 29 | - | 36 | - | 44 | ns |
| | | | 6 | - | - | 25 | - | 31 | - | 38 | ns |
| OE ₁ to any \bar{Y} or Y | t _{TLH} , t _{THL} | C _L = 50pF | 2 | - | - | 145 | - | 180 | - | 220 | ns |
| | | | 4.5 | - | - | 29 | - | 36 | - | 44 | ns |
| | | | 6 | - | - | 25 | - | 31 | - | 38 | ns |
| LE to any \bar{Y} or Y | t _{TLH} , t _{THL} | C _L = 50pF | 2 | - | - | 190 | - | 240 | - | 285 | ns |
| | | | 4.5 | - | - | 38 | - | 48 | - | 57 | ns |
| | | | 6 | - | - | 32 | - | 41 | - | 48 | ns |
| Power Dissipation Capacitance, (Notes 3, 4) CD74HC137 | C _{PD} | C _L = 15pF | 5 | - | 19 | - | - | - | - | pF | |
| | C _{PD} | C _L = 15pF | 5 | - | 23 | - | - | - | - | pF | |
| Output Transition Time | t _{TLH} , t _{THL} | C _L = 50pF | 2 | - | - | 75 | - | 95 | - | 110 | ns |
| | | | 4.5 | - | - | 15 | - | 19 | - | 22 | ns |
| | | | 6 | - | - | 13 | - | 16 | - | 19 | ns |
| Input Capacitance | C _I | - | - | - | 10 | - | 10 | - | 10 | pF | |

CD74HC137, CD74HCT137, CD54HC237, CD74HC237, CD74HCT237

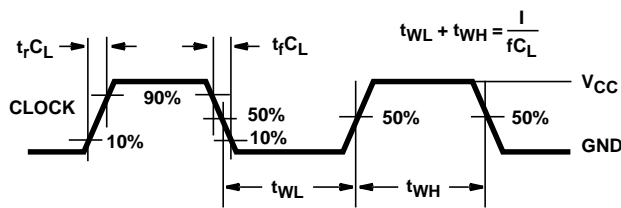
Switching Specifications Input $t_r, t_f = 6\text{ns}$ (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | V_{CC} (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|--|--------------------|---------------------|--------------|------|-----|-----|---------------|-----|----------------|-----|-------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| HCT TYPES | | | | | | | | | | | |
| Propagation Delay An to any \bar{Y} or Y Address to Output | t_{PLH}, t_{PHL} | $C_L = 50\text{pF}$ | 4.5 | - | - | 38 | - | 48 | - | 57 | ns |
| | t_{PLH}, t_{PHL} | $C_L = 15\text{pF}$ | 5 | - | 16 | - | - | - | - | - | ns |
| OE_0 to any Y (HC137) | t_{PLH}, t_{PHL} | $C_L = 50\text{pF}$ | 4.5 | - | - | 35 | - | 44 | - | 53 | ns |
| OE_0 to any \bar{Y} (HC237) | t_{PLH}, t_{PHL} | $C_L = 50\text{pF}$ | 4.5 | - | - | 33 | - | 41 | - | 60 | ns |
| \overline{OE}_1 to any \bar{Y} (HC137) | t_{TLH}, t_{THL} | $C_L = 50\text{pF}$ | 4.5 | - | - | 37 | - | 46 | - | 56 | ns |
| \overline{OE}_1 to any \bar{Y} (HC237) | t_{TLH}, t_{THL} | $C_L = 50\text{pF}$ | 4.5 | - | - | 35 | - | 44 | - | 53 | ns |
| LE to any Y (HC137) | t_{TLH}, t_{THL} | $C_L = 50\text{pF}$ | 4.5 | - | - | 44 | - | 55 | - | 66 | ns |
| LE to any \bar{Y} (HC237) | t_{TLH}, t_{THL} | $C_L = 50\text{pF}$ | 4.5 | - | - | 42 | - | 53 | - | 63 | ns |
| Power Dissipation Capacitance, (Notes 3, 4) | | | | | | | | | | | |
| CD74HC137 | C_{PD} | $C_L = 15\text{pF}$ | 5 | - | 19 | - | - | - | - | - | pF |
| 'HC237 | C_{PD} | $C_L = 15\text{pF}$ | 5 | - | 23 | - | - | - | - | - | pF |
| Output Transition Time | t_{TLH}, t_{THL} | $C_L = 50\text{pF}$ | 4.5 | | | 15 | | 19 | | 22 | ns |
| Input Capacitance | C_i | - | - | - | - | 10 | - | 10 | - | 10 | pF |

NOTES:

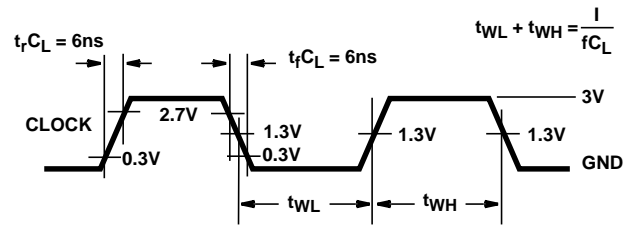
- C_{PD} is used to determine the dynamic power consumption, per gate.
- $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where: f_i = Input Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

Test Circuits and Waveforms



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX} , input duty cycle = 50%.

FIGURE 1. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX} , input duty cycle = 50%.

FIGURE 2. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH

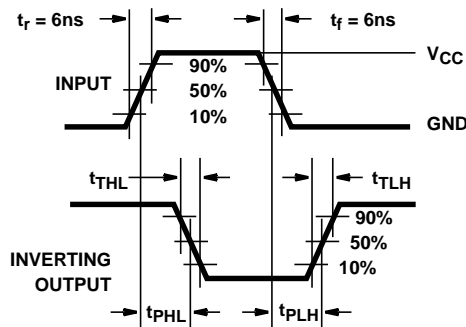


FIGURE 3. HC AND HCU TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

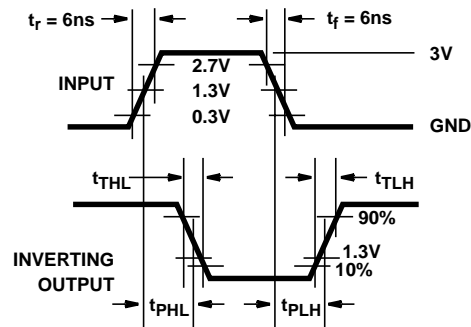


FIGURE 4. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

Test Circuits and Waveforms (Continued)

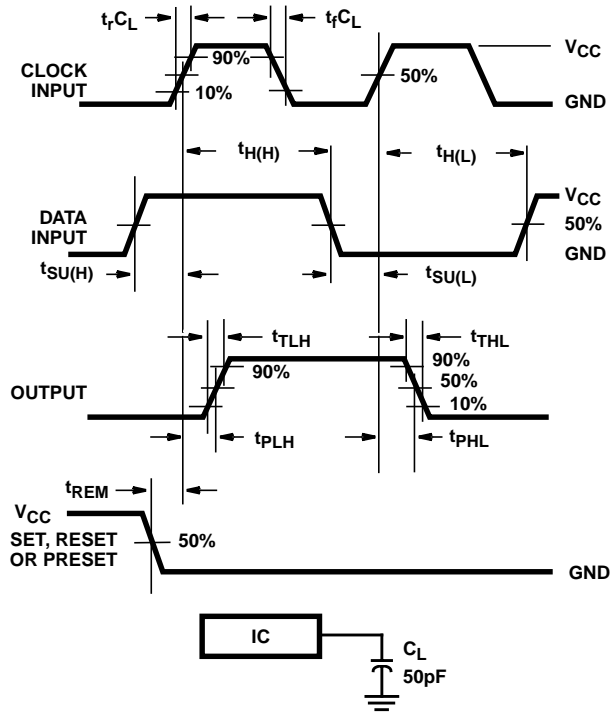


FIGURE 5. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

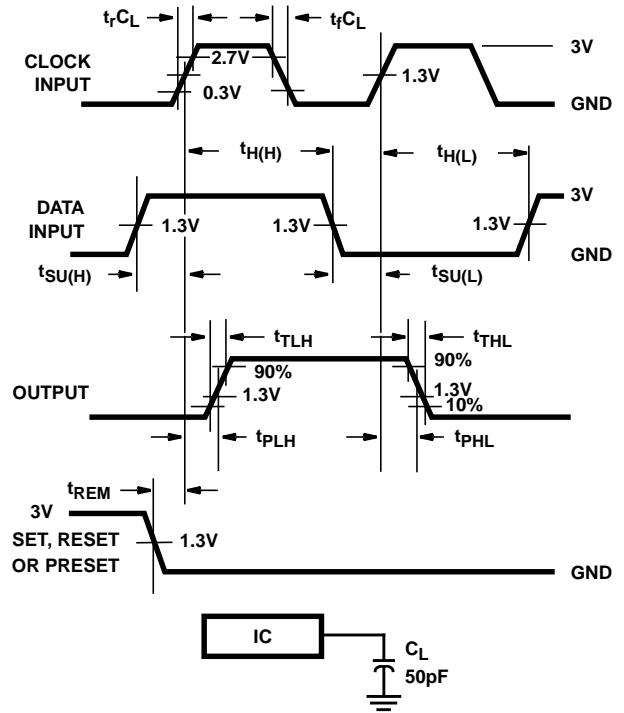


FIGURE 6. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|------------------|--------------------------------------|----------------------|--------------|--------------------------------|-------------------------|
| 5962-8860601EA | ACTIVE | CDIP | J | 16 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8860601EA CD54HC237F3A | Samples |
| CD54HC237F | ACTIVE | CDIP | J | 16 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | CD54HC237F | Samples |
| CD54HC237F3A | ACTIVE | CDIP | J | 16 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8860601EA CD54HC237F3A | Samples |
| CD74HC137E | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -55 to 125 | CD74HC137E | Samples |
| CD74HC137PW | LIFEBUY | TSSOP | PW | 16 | 90 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HJ137 | |
| CD74HC137PWR | ACTIVE | TSSOP | PW | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HJ137 | Samples |
| CD74HC237E | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -55 to 125 | CD74HC237E | Samples |
| CD74HC237EE4 | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -55 to 125 | CD74HC237E | Samples |
| CD74HC237M96 | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU SN | Level-1-260C-UNLIM | -55 to 125 | HC237M | Samples |
| CD74HC237NSR | ACTIVE | SO | NS | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC237M | Samples |
| CD74HC237PWR | ACTIVE | TSSOP | PW | 16 | 2000 | RoHS & Green | NIPDAU SN | Level-1-260C-UNLIM | -55 to 125 | HJ237 | Samples |
| CD74HCT137E | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -55 to 125 | CD74HCT137E | Samples |
| CD74HCT137M96 | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCT137M | Samples |
| CD74HCT137MT | LIFEBUY | SOIC | D | 16 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCT137M | |
| CD74HCT237E | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -55 to 125 | CD74HCT237E | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF CD54HC237, CD74HC237 :

● Catalog : [CD74HC237](#)

● Military : [CD54HC237](#)

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product

● Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD74HC137PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| CD74HC237M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| CD74HC237M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.6 | 9.3 | 2.1 | 8.0 | 16.0 | Q1 |
| CD74HC237NSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| CD74HC237PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| CD74HC237PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.85 | 5.45 | 1.6 | 8.0 | 12.0 | Q1 |
| CD74HC237PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| CD74HCT137M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD74HC137PWR | TSSOP | PW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| CD74HC237M96 | SOIC | D | 16 | 2500 | 356.0 | 356.0 | 35.0 |
| CD74HC237M96 | SOIC | D | 16 | 2500 | 366.0 | 364.0 | 50.0 |
| CD74HC237NSR | SO | NS | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| CD74HC237PWR | TSSOP | PW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| CD74HC237PWR | TSSOP | PW | 16 | 2000 | 366.0 | 364.0 | 50.0 |
| CD74HC237PWR | TSSOP | PW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| CD74HCT137M96 | SOIC | D | 16 | 2500 | 340.5 | 336.1 | 32.0 |

TUBE


*All dimensions are nominal



| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|--------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| CD74HC137E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HC137E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HC137PW | PW | TSSOP | 16 | 90 | 530 | 10.2 | 3600 | 3.5 |
| CD74HC237E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HC237E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HC237EE4 | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HC237EE4 | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HCT137E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HCT137E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HCT237E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HCT237E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

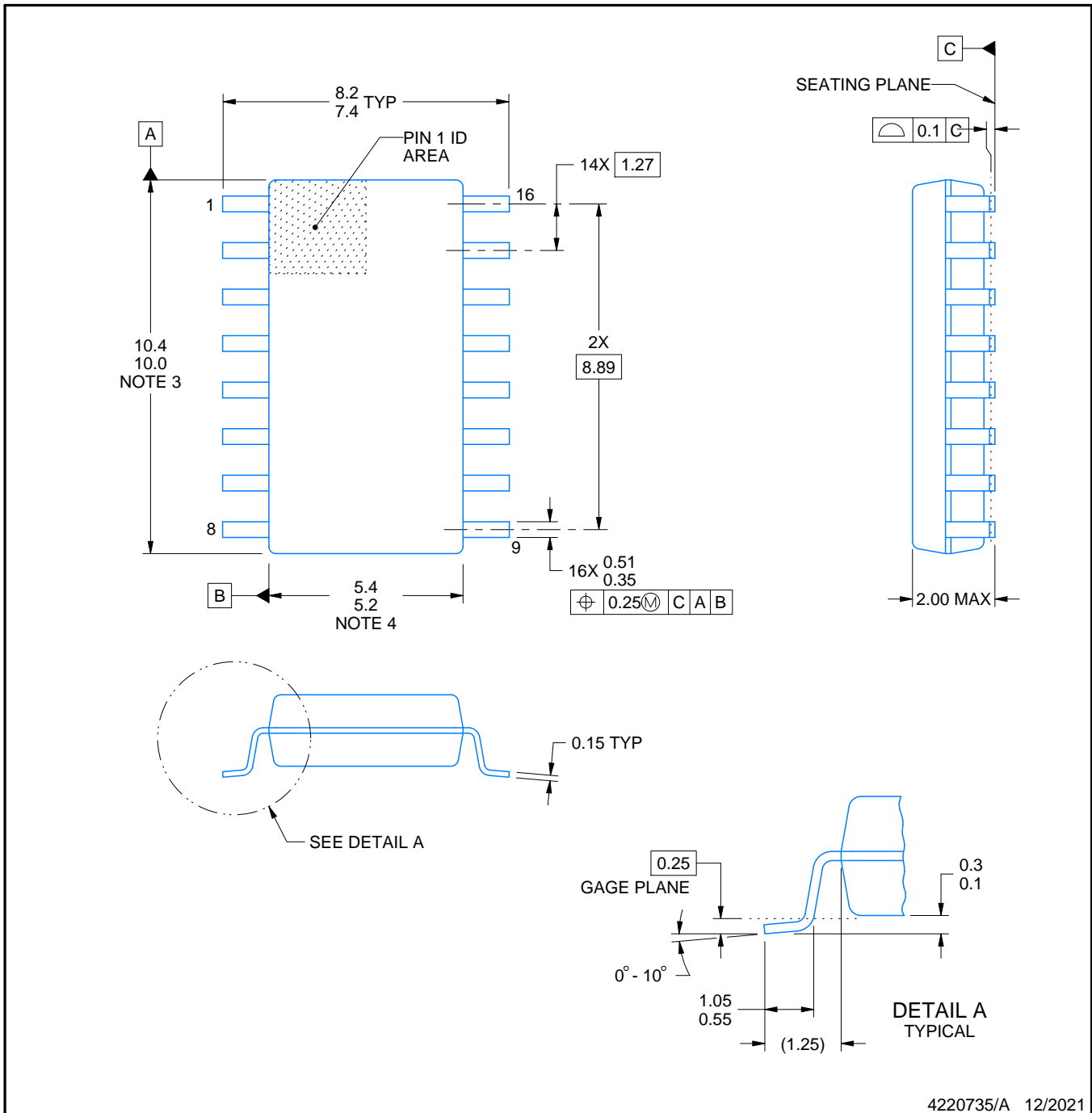


PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES:

- All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

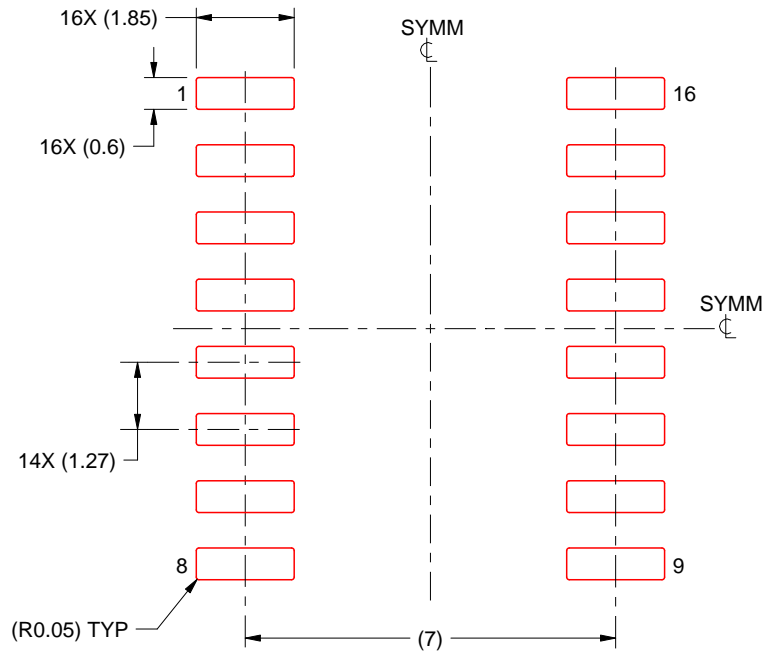
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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