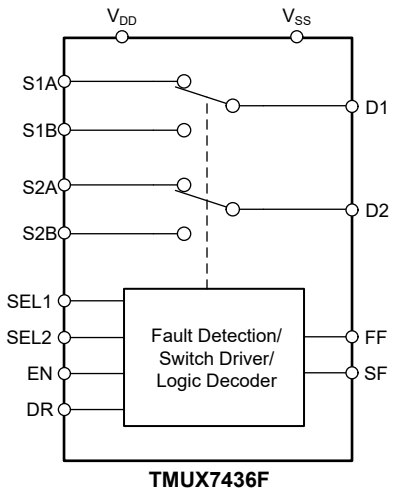
TMUX7436F ±60 V Fault-Protected, Dual 2:1 Multiplexer With Latch-Up Immunity and 1.8 V Logic

1 Features

- Wide supply voltage range:
  - Single supply: 8 V to 44 V
  - Dual supply: ±5 V to ±22 V
- Integrated fault protection:
  - Overvoltage protection, source to supplies or source to drain: ±85 V
  - Overvoltage protection: ±60 V
  - Powered-off protection: ±60 V
  - Interrupt flags to indicate fault status
  - Output open circuited during fault
- Latch-up immunity by device construction
- 6 kV human body model (HBM) ESD rating
- Low On-Resistance: 8.6 Ω typical
- Flat On-Resistance: 10 mΩ typical
- 1.8-V Logic capable
- Failsafe logic: up to 44 V independent of supply
- Industry-standard TSSOP and smaller WQFN packages

2 Applications

- Factory automation and control
- Programmable logic controllers (PLC)
- Analog input modules
- Semiconductor test equipment
- Battery test equipment
- Servo drive control module
- Data acquisition systems (DAQ)



Functional Block Diagram

3 Description

The TMUX7436F is a complementary metal-oxide semiconductor (CMOS) analog multiplexer with latch-up immunity in a dual channel, 2:1 configuration. The device works well with dual supplies (±5 V to ±22 V), a single supply (8 V to 44 V), or asymmetric supplies (such as V_{DD} = 12 V, V_{SS} = –5 V). The overvoltage protection is available in powered and powered-off conditions, making the TMUX7436F device suitable for applications where power supply sequencing cannot be precisely controlled.

The device blocks fault voltages up to +60 V or −60 V relative to ground in powered and powered-off conditions. When no power supplies are present, the switch channels remain in the OFF state regardless of switch input conditions, and any control signal present on the logic pins is ignored. If the signal path input voltage on any Sx pin exceeds the supply voltage (V_{DD} or V_{SS}) by a threshold voltage (V_T), then the channel turns OFF and the Sx pin becomes high impedance. The drain pin (Dx) is either pulled to the fault supply voltage that was exceeded or left floating depending on the DR control logic. The TMUX7436F device provides two active-low interrupt flags (FF and SF) to provide details of the fault and help system diagnostics. The FF flag indicates if any of the source inputs are experiencing a fault condition, while the SF flag is used to decode which specific inputs are experiencing a fault condition.

Package Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TMUX7436F	PW (TSSOP, 16)	5.00 mm × 4.40 mm
	RRP (WQFN, 16)(2)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) Preview package

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4 Revision History

Changes from Revision * (October 2022) to Revision A (November 2022)	Page
• Changed the status of the data sheet from: *Advanced Information* to: *Production Data*	1

5 Pin Configuration and Functions

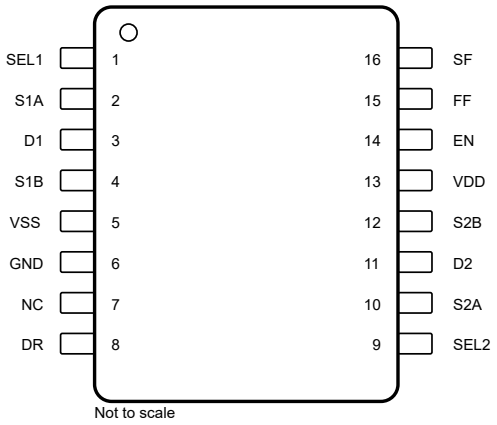


Figure 5-1. PW Package, 16-Pin TSSOP (Top View)

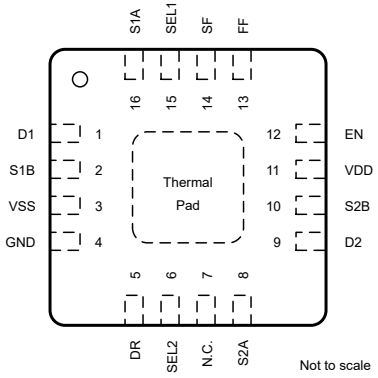


Figure 5-2. RRP (Preview) Package, 16-Pin WQFN (Top View)

Table 5-1. Pin Functions

PIN			TYPE[1]	DESCRIPTION
NAME	TSSOP	WQFN[2]		
D1	3	1	I/O	Drain pin 1. Can be an input or output. The drain pin is not overvoltage protected.
D2	11	9	I/O	Drain pin 2. Can be an input or output. The drain pin is not overvoltage protected.
DR	8	5	I	Drain Response (DR) input. Tying the DR pin to GND enables the drain to be pulled to V_{DD} or V_{SS} through a 40 kΩ resistor during an overvoltage fault event. The drain pin becomes open circuit when the DR pin is a logic high or left floating.
EN	14	12	I	Active high logic enable (EN) pin, has internal 4 MΩ pull-down resistor. The device is disabled and all switches become high impedance when the pin is low. As provided in Table 8-1, when the pin is high, the SELx logic inputs determine individual switch states.
FF	15	13	O	General fault flag. This pin is an open drain output and is asserted low when overvoltage condition is detected on any of the source (Sxy) input pins. Connect this pin to an external supply (1.8 V to 5.5 V) through a 1 kΩ pull-up resistor.
GND	6	4	P	Ground (0 V) reference
N.C.	7	7	—	No internal connection. This pin can be shorted to GND or left floating.
S1A	2	16	I/O	Overvoltage protected source pin 1A. Can be an input or output.
S1B	4	2	I/O	Overvoltage protected source pin 1B. Can be an input or output.
S2A	10	8	I/O	Overvoltage protected source pin 2A. Can be an input or output.
S2B	12	10	I/O	Overvoltage protected source pin 2B. Can be an input or output.
SEL1	1	15	I	Logic control input 1.
SEL2	9	6	I	Logic control input 2.
SF	16	14	O	Specific fault flag. This pin is an open drain output and is asserted low when an overvoltage condition is detected on a specific (Sxy) input pin, depending on the state of the SELx pins, as provided in Table 8-1. Connect this pin to an external supply (1.8 V to 5.5 V) through a 1 kΩ pull-up resistor.
V_{DD}	13	11	P	Positive power supply. This pin is the most positive power-supply potential. Connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{DD} and GND for reliable operation.
V_{SS}	5	3	P	Negative power supply. This pin is the most negative power-supply potential. This pin can be connected to ground in single-supply applications. Connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{SS} and GND for reliable operation.
Thermal Pad			—	The thermal pad is not connected internally. It is recommended to tie the pad to GND or VSS for best performance.

(1) I = input, O = output, I/O = input and output, P = power.
(2) Preview package.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD} to V_{SS}	Supply voltage		48	V
V_{DD} to GND		–0.3	48	V
V_{SS} to GND		–48	0.3	V
V_S to GND	Source input pin (Sx) voltage to GND	–65	65	V
V_S to V_{DD}	Source input pin (Sx) voltage to V_{DD}	–90		V
V_S to V_{SS}	Source input pin (Sx) voltage to V_{SS}		90	V
V_D	Drain pin (Dx) voltage	V_{SS}–0.7	V_{DD}+0.7	V
V_{LOGIC}	Logic control input pin voltage (EN, SELx, DR)(2)	GND –0.7	48	V
V_{xF}	Logic output pin voltage (FF, SF)(2)	GND –0.7	6	V
I_{LOGIC}	Logic control input pin current (EN, SELx, DR)(2)	–30	30	mA
I_{xF}	Logic output pin current (FF, SF)(2)	–10	10	mA
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (Sx or Dx)	I_{DC} ± 10 %(3)	I_{DC} ± 10 %(3)	mA
T_{stg}	Storage temperature	–65	150	°C
T_A	Ambient temperature	–55	150	°C
T_J	Junction temperature		150	°C
P_{tot} (4)	Total power dissipation (TSSOP)		650	mW

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Stresses have to be kept at or below both voltage and current ratings at all time.
(3) Refer to Recommended Operating Conditions for I_{DC} ratings.
(4) For TSSOP package: P_{tot} derates linearly above T_A = 70°C by 10.1 mW/°C.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±4000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Thermal Information

THERMAL METRIC(1)		TMUX7436F		UNIT
		PW (TSSOP)	RRP (WQFN)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	100.4	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	31.3	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	46.4	TBD	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.7	TBD	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	45.8	TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	TBD	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$V_{DD} – V_{SS}$ (1)	Power supply voltage differential		8		44	V
V_{DD}	Positive power supply voltage		5		44	
V_S	Source pin (Sx) voltage (non-fault condition)		V_{SS}		V_{DD}	V
V_S to GND	Source pin (Sx) voltage to GND (fault condition)		–60		60	
V_S to V_{DD} (2)	Source pin (Sx) voltage to V_{DD} or V_D (fault condition)		–85			
V_S to V_{SS} (2)	Source pin (Sx) voltage to V_{SS} or V_D (fault condition)				85	
V_D	Drain pin (Dx) voltage		V_{SS}		V_{DD}	
V_{LOGIC}	Logic control input pin voltage (EN, SELx, DR)		GND		44	V
V_{xF} (3)	Logic output pin voltage (FF, SF)		GND		5.5	
T_A	Ambient temperature		–40		125	°C
I_{DC}	Continuous current through switch operating 1 channel, TSSOP package	T_A = 25°C			115	mA
		T_A = 85°C			115	mA
		T_A = 125°C			85	mA
I_{DC}	Continuous current through switch operating max number of channels at the same time, TSSOP package	T_A = 25°C			115	mA
		T_A = 85°C			115	mA
		T_A = 125°C			60	mA

(1) V_{DD} and V_{SS} can be any value as long as 8 V ≤ (V_{DD} – V_{SS}) ≤ 44 V, and the minimum V_{DD} is met.
(2) Source pin voltage (Sx) under a fault condition may not exceed 85 V from supply pins (V_{DD} and V_{SS}.) or drain pins (D, Dx).
(3) Logic output pin (FF) is an open drain output and should be pulled up to a voltage within the maximum ratings.

6.5 Electrical Characteristics: Global

at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG SWITCH							
V_T	Threshold voltage for fault detector		25°C		0.7		V
LOGIC INPUT/ OUTPUT							
V_{IH}	High-level input voltage	EN, SELx, DR pins	–40°C to +125°C	1.3		44	V
V_{IL}	Low-level input voltage	EN, SELx, DR pins	–40°C to +125°C	0		0.8	V
$V_{OL(FLAG)}$	Low-level output voltage	FF and SF pins, I_O = 5 mA	–40°C to +125°C			0.35	V
POWER SUPPLY							
V_{UVLO}	Undervoltage lockout (UVLO) threshold voltage (V_{DD} – V_{SS})	Rising edge, single supply	–40°C to +125°C	5.1	5.8	6.6	V
		Falling edge, single supply	–40°C to +125°C	5	5.7	6.4	V
V_{HYS}	V_{DD} Undervoltage lockout (UVLO) hysteresis	Single supply	–40°C to +125°C		0.2		V
$R_{D(OVP)}$	Drain resistance to supply rail during overvoltage event on selected source pin	Drain resistance to supply rail during overvoltage event on selected source pin	25°C		40		kΩ

6.6 ±15 V Dual Supply: Electrical Characteristics

V_{DD} = +15 V ± 10%, V_{SS} = –15 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +15 V, V_{SS} = –15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = –10 V to +10 V I_D = –10 mA	25°C		8.6	11	Ω
			–40°C to +85°C			14	
			–40°C to +125°C			16.5	
ΔR_{ON}	On-resistance mismatch between channels	V_S = –10 V to +10 V I_D = –10 mA	25°C		0.06	0.45	Ω
			–40°C to +85°C			0.5	
			–40°C to +125°C			0.6	
R_{FLAT}	On-resistance flatness	V_S = –10 V to +10 V I_D = –10 mA	25°C		0.01	0.4	Ω
			–40°C to +85°C			0.4	
			–40°C to +125°C			0.4	
R_{ON_DRIFT}	On-resistance drift	V_S = 0 V, I_S = –10 mA	–40°C to +125°C		0.04		Ω/°C
$I_{S(OFF)}$	Input leakage current(1)	V_{DD} = 16.5 V, V_{SS} = –16.5 V Switch state is off V_S = +10 V / –10 V V_D = –10 V / + 10 V	25°C	–0.7	0.03	0.7	nA
			–40°C to +85°C	–2		2	
			–40°C to +125°C	–11		11	
$I_{D(OFF)}$	Output off leakage current(1)	V_{DD} = 16.5 V, V_{SS} = –16.5 V Switch state is off V_S = +10 V / –10 V V_D = –10 V / + 10 V	25°C	–1.4	0.06	1.4	nA
			–40°C to +85°C	–4		4	
			–40°C to +125°C	–24		24	
$I_{S(ON)}$ $I_{D(ON)}$	Output on leakage current(2)	V_{DD} = 16.5 V, V_{SS} = –16.5 V Switch state is on V_S = V_D = ±10 V	25°C	–1.4	0.08	1.4	nA
			–40°C to +85°C	–4		4	
			–40°C to +125°C	–27		27	
FAULT CONDITION							
$I_{S(FA)}$	Input leakage current durring overvoltage	V_S = ± 60 V, GND = 0 V, V_{DD} = 16.5 V, V_{SS} = –16.5 V	–40°C to +125°C		±100		µA
$I_{S(FA)\ Grounded}$	Input leakage current during overvoltage with grounded supply voltages	V_S = ± 60 V, GND = 0 V V_{DD} = V_{SS} = 0 V	–40°C to +125°C		±125		µA
$I_{S(FA)\ Floating}$	Input leakage current during overvoltage with floating supply voltages	V_S = ± 60 V, GND = 0 V, V_{DD} = V_{SS} = floating	–40°C to +125°C		±125		µA
$I_{D(FA)}$	Output leakage current during overvoltage	V_S = ± 60 V, GND = 0 V, V_{DD} = 16.5 V, V_{SS} = –16.5 V	25°C	–20	±0.1	20	nA
			–40°C to +85°C	–30		30	
			–40°C to +125°C	–60		60	
$I_{D(FA)\ Grounded}$	Output leakage current during overvoltage with grounded supply voltages	V_S = ± 60 V, GND = 0 V, V_{DD} = V_{SS} = 0 V	25°C	–30	±0.01	30	nA
			–40°C to +85°C	–50		50	
			–40°C to +125°C	–90		90	
$I_{D(FA)\ Floating}$	Output leakage current during overvoltage with floating supply voltages	V_S = ± 60 V, GND = 0 V, V_{DD} = V_{SS} = floating	25°C		±4		µA
			–40°C to +85°C		±6		
			–40°C to +125°C		±8		
I_{IH}	High-level input current	V_{EN} = V_{SELx} = V_{DR} = V_{DD}	25°C			±1.6	µA
			–40°C to +125°C			±2	
I_{IL}	Low-level input current	V_{EN} = V_{SELx} = V_{DR} = 0	25°C			±1	µA
			–40°C to +125°C			±1.1	

6.6 ±15 V Dual Supply: Electrical Characteristics (continued)

V_{DD} = +15 V ± 10%, V_{SS} = –15 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +15 V, V_{SS} = –15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
SWITCHING CHARACTERISTICS							
$t_{ON (EN)}$	Enable turn-on time	V_S = 10 V, R_L = 300 Ω, C_L= 12 pF	25°C		435	515	ns
			–40°C to +85°C			530	
			–40°C to +125°C			550	
$t_{OFF (EN)}$	Enable turn-off time	V_S = 10 V, R_L = 300 Ω, C_L= 12 pF	25°C		50	130	ns
			–40°C to +85°C			140	
			–40°C to +125°C			150	
t_{TRAN}	Transition time	V_S = 10 V, R_L = 300 Ω, C_L= 12 pF	25°C		417	540	ns
			–40°C to +85°C			555	
			–40°C to +125°C			570	
$t_{RESPONSE}$	Fault response time	R_L = 300 Ω, C_L= 12 pF	25°C		110	505	ns
			–40°C to +85°C			515	
			–40°C to +125°C			520	
$t_{RECOVERY}$	Fault recovery time	R_L = 300 Ω, C_L= 12 pF	25°C		1600	4500	ns
			–40°C to +85°C			4800	
			–40°C to +125°C			4800	
$t_{RESPONSE(FLAG)}$	Fault flag response time	R_L = 300 Ω, C_L= 12 pF, R_{PU} = 1 kΩ, C_{L_xF} = 12 pF	25°C		120		ns
$t_{RECOVERY(FLAG)}$	Fault flag recovery time	R_L = 300 Ω, C_L= 12 pF, R_{PU} = 1 kΩ, C_{L_xF} = 12 pF	25°C		1		µs
t_{BBM}	Break-before-make time delay	V_S = 10 V, R_L = 300 Ω, C_L= 12 pF	–40°C to +125°C	200	380		ns
Q_{INJ}	Charge injection	V_S = 0 V, C_L = 1 nF	25°C		–300		pC
O_{ISO}	Off-isolation	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 1 MHz	25°C		–60		dB
X_{TALK}	Intra-channel crosstalk	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 1 MHz	25°C		–62		dB
	Inter-channel crosstalk	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 1 MHz	25°C		–88		
BW	–3 dB bandwidth	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 0 V	25°C		220		MHz
I_{LOSS}	Insertion loss	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 1 MHz	25°C		–0.7		dB
THD+N	Total harmonic distortion plus noise	R_S = 50 Ω, R_L = 10 kΩ, V_S = 15 V_{PP}, V_{BIAS} = 0 V, f = 20 Hz to 20 kHz	25°C		0.0007		%
$C_{S(OFF)}$	Input off-capacitance	f = 1 MHz, V_S = 0 V	25°C		13		pF
$C_{D(OFF)}$	Output off-capacitance	f = 1 MHz, V_S = 0 V	25°C		25		pF
$C_{S(ON)}$ $C_{D(ON)}$	Input/Output on-capacitance	f = 1 MHz, V_S = 0 V	25°C		28		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 16.5 V, V_{SS} = –16.5 V, V_{SELx} = V_{DR} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.32	0.5	mA
			–40°C to +85°C			0.5	
			–40°C to +125°C			0.6	
I_{SS}	V_{SS} supply current	V_{DD} = 16.5 V, V_{SS} = –16.5 V, V_{SELx} = V_{DR} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.26	0.4	mA
			–40°C to +85°C			0.4	
			–40°C to +125°C			0.5	
I_{GND}	GND current	V_{DD} = 16.5 V, V_{SS} = –16.5 V, V_{SELx} = V_{DR} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.06		mA
$I_{DD(FA)}$	V_{DD} supply current under fault	V_S = ± 60 V, V_{DD} = 16.5 V, V_{SS} = –16.5 V, V_{SELx} = V_{DR} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.27	0.7	mA
			–40°C to +85°C			0.8	
			–40°C to +125°C			0.8	

6.6 ±15 V Dual Supply: Electrical Characteristics (continued)

V_{DD} = +15 V ± 10%, V_{SS} = –15 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +15 V, V_{SS} = –15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
$I_{SS(FA)}$	V_{SS} supply current under fault	V_S = ± 60 V, V_{DD} = 16.5 V, V_{SS} = –16.5 V, V_{SELx} = V_{DR} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.2	0.6	mA
			–40°C to +85°C			0.8	
			–40°C to +125°C			0.8	
$I_{GND(FA)}$	GND current under fault	V_S = ± 60 V, V_{DD} = 16.5 V, V_{SS} = –16.5 V, V_{SELx} = V_{DR} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.15		mA
$I_{DD(DISABLE)}$	V_{DD} supply current (disable mode)	V_{DD} = 16.5 V, V_{SS} = –16.5 V, V_{SELx} = V_{DR} = 0 V, 5 V, or V_{DD}, V_{EN} = 0 V	25°C		0.15	0.5	mA
			–40°C to +85°C			0.5	
			–40°C to +125°C			0.5	
$I_{SS(DISABLE)}$	V_{SS} supply current (disable mode)	V_{DD} = 16.5 V, V_{SS} = –16.5 V, V_{SELx} = V_{DR} = 0 V, 5 V, or V_{DD}, V_{EN} = 0 V	25°C		0.1	0.4	mA
			–40°C to +85°C			0.4	
			–40°C to +125°C			0.4	

(1) When V_S is positive,V_D is negative. And when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating. And when V_D is at a voltage potential, V_S is floating.

6.7 ±20 V Dual Supply: Electrical Characteristics

V_{DD} = +20 V ± 10%, V_{SS} = –20 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +20 V, V_{SS} = –20 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = –15 V to +15 V I_D = –10 mA	25°C		8.6	11	Ω
			–40°C to +85°C			14	
			–40°C to +125°C			17	
ΔR_{ON}	On-resistance mismatch between channels	V_S = –15 V to +15 V I_D = –10 mA	25°C		0.06	0.35	Ω
			–40°C to +85°C			0.5	
			–40°C to +125°C			0.5	
R_{FLAT}	On-resistance flatness	V_S = –15 V to +15 V I_D = –10 mA	25°C		0.015	0.4	Ω
			–40°C to +85°C			0.5	
			–40°C to +125°C			0.5	
R_{ON_DRIFT}	On-resistance drift	V_S = 0 V, I_S = –10 mA	–40°C to +125°C		0.04		Ω/°C
$I_{S(OFF)}$	Input leakage current(1)	V_{DD} = 22 V, V_{SS} = –22 V Switch state is off V_S = +15 V / –15 V V_D = –15 V / + 15 V	25°C	–0.7	0.03	0.7	nA
			–40°C to +85°C	–2		2	
			–40°C to +125°C	–11		11	
$I_{D(OFF)}$	Output off leakage current(1)	V_{DD} = 22 V, V_{SS} = –22 V Switch state is off V_S = +15 V / –15 V V_D = –15 V / + 15 V	25°C	–1.4	0.06	1.4	nA
			–40°C to +85°C	–4		4	
			–40°C to +125°C	–24		24	
$I_{S(ON)}$ $I_{D(ON)}$	Output on leakage current(2)	V_{DD} = 22 V, V_{SS} = –22 V Switch state is on V_S = V_D = ±15 V	25°C	–1.4	0.08	1.4	nA
			–40°C to +85°C	–4		4	
			–40°C to +125°C	–27		27	
FAULT CONDITION							
$I_{S(FA)}$	Input leakage current durring overvoltage	V_S = ± 60 V, GND = 0 V, V_{DD} = 22 V, V_{SS} = –22 V	–40°C to +125°C		±85		µA
$I_{S(FA)\ Grounded}$	Input leakage current during overvoltage with grounded supply voltages	V_S = ± 60 V, GND = 0 V, V_{DD} = V_{SS} = 0 V	–40°C to +125°C		±125		µA
$I_{S(FA)\ Floating}$	Input leakage current during overvoltage with floating supply voltages	V_S = ± 60 V, GND = 0 V, V_{DD} = V_{SS} = floating	–40°C to +125°C		±125		µA
$I_{D(FA)}$	Output leakage current during overvoltage	V_S = ± 60 V, GND = 0 V, V_{DD} = 22 V, V_{SS} = –22 V,	25°C	–50	±5	50	nA
			–40°C to +85°C	–70		70	
			–40°C to +125°C	–90		90	
$I_{D(FA)\ Grounded}$	Output leakage current during overvoltage with grounded supply voltages	V_S = ± 60 V, GND = 0 V, V_{DD} = V_{SS} = 0 V	25°C	–30	±10	30	nA
			–40°C to +85°C	–50		50	
			–40°C to +125°C	–90		90	
$I_{D(FA)\ Floating}$	Output leakage current during overvoltage with floating supply voltages	V_S = ± 60 V, GND = 0 V, V_{DD} = V_{SS} = floating	25°C		±4		µA
			–40°C to +85°C		±6		
			–40°C to +125°C		±8		
I_{IH}	High-level input current	V_{EN} = V_{SELx} = V_{DR} = V_{DD}	25°C			±1.8	µA
			–40°C to +125°C			±2.2	
I_{IL}	Low-level input current	V_{EN} = V_{SELx} = V_{DR} = 0	25°C			±1	µA
			–40°C to +125°C			±1.1	

6.7 ±20 V Dual Supply: Electrical Characteristics (continued)

V_{DD} = +20 V ± 10%, V_{SS} = –20 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +20 V, V_{SS} = –20 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
SWITCHING CHARACTERISTICS							
$t_{ON (EN)}$	Enable turn-on time	V_S = 10 V, R_L = 300 Ω, C_L= 12 pF	25°C		430	535	ns
			–40°C to +85°C			560	
			–40°C to +125°C			585	
$t_{OFF (EN)}$	Enable turn-off time	V_S = 10 V, R_L = 300 Ω, C_L= 12 pF	25°C		50	120	ns
			–40°C to +85°C			130	
			–40°C to +125°C			150	
t_{TRAN}	Transition time	V_S = 10 V, R_L = 300 Ω, C_L= 12 pF	25°C		433	555	ns
			–40°C to +85°C			571	
			–40°C to +125°C			580	
$t_{RESPONSE}$	Fault response time	R_L = 300 Ω, C_L= 12 pF	25°C		110	505	ns
			–40°C to +85°C			515	
			–40°C to +125°C			520	
$t_{RECOVERY}$	Fault recovery time	R_L = 300 Ω, C_L= 12 pF	25°C		1600	4500	ns
			–40°C to +85°C			4900	
			–40°C to +125°C			4900	
$t_{RESPONSE(FLAG)}$	Fault flag response time	R_L = 300 Ω, C_L= 12 pF, R_{PU} = 1 kΩ, C_{L_xF} = 12 pF	25°C		140		ns
$t_{RECOVERY(FLAG)}$	Fault flag recovery time	R_L = 300 Ω, C_L= 12 pF, R_{PU} = 1 kΩ, C_{L_xF} = 12 pF	25°C		1		µs
t_{BBM}	Break-before-make time delay	V_S = 10 V, R_L = 300 Ω, C_L= 12 pF	–40°C to +125°C	210	400		ns
Q_{INJ}	Charge injection	V_S = 0 V, C_L = 1 nF	25°C		–330		pC
O_{ISO}	Off-isolation	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 1 MHz	25°C		–60		dB
X_{TALK}	Intra-channel crosstalk	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 1 MHz	25°C		–64		dB
	Inter-channel crosstalk	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 1 MHz	25°C		–81		
BW	–3 dB bandwidth	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 0 V	25°C		230		MHz
I_{LOSS}	Insertion loss	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 1 MHz	25°C		–0.7		dB
THD+N	Total harmonic distortion plus noise	R_S = 50 Ω, R_L = 10 kΩ, V_S = 20 V_{PP}, V_{BIAS} = 0 V, f = 20 Hz to 20 kHz	25°C		0.0008		%
$C_{S(OFF)}$	Input off-capacitance	f = 1 MHz, V_S = 0 V	25°C		12		pF
$C_{D(OFF)}$	Output off-capacitance	f = 1 MHz, V_S = 0 V	25°C		24		pF
$C_{S(ON)}$ $C_{D(ON)}$	Input/Output on-capacitance	f = 1 MHz, V_S = 0 V	25°C		27		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 22 V, V_{SS} = –22 V, V_{SELx} = V_{DR} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.32	0.5	mA
			–40°C to +85°C			0.5	
			–40°C to +125°C			0.6	
I_{SS}	V_{SS} supply current	V_{DD} = 22 V, V_{SS} = –22 V, V_{SELx} = V_{DR} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.26	0.4	mA
			–40°C to +85°C			0.4	
			–40°C to +125°C			0.5	
I_{GND}	GND current	V_{DD} = 22 V, V_{SS} = –22 V, V_{SELx} = V_{DR} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.06		mA
$I_{DD(FA)}$	V_{DD} supply current under fault	V_S = ± 60 V, V_{DD} = 22 V, V_{SS} = –22 V, V_{SELx} = V_{DR} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.27	0.8	mA
			–40°C to +85°C			1	
			–40°C to +125°C			1	

6.7 ±20 V Dual Supply: Electrical Characteristics (continued)

V_{DD} = +20 V ± 10%, V_{SS} = –20 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +20 V, V_{SS} = –20 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
$I_{SS(FA)}$	V_{SS} supply current under fault	V_S = ± 60 V, V_{DD} = 22 V, V_{SS} = –22 V, V_{SELx} = V_{DR} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.2	0.7	mA
			–40°C to +85°C			1	
			–40°C to +125°C			1	
$I_{GND(FA)}$	GND current under fault	V_S = ± 60 V, V_{DD} = 22 V, V_{SS} = –22 V, V_{SELx} = V_{DR} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.15		mA
$I_{DD(DISABLE)}$	V_{DD} supply current (disable mode)	V_{DD} = 22 V, V_{SS} = –22 V, V_{SELx} = V_{DR} = 0 V, 5 V, or V_{DD}, V_{EN} = 0 V	25°C		0.15	0.5	mA
			–40°C to +85°C			0.5	
			–40°C to +125°C			0.5	
$I_{SS(DISABLE)}$	V_{SS} supply current (disable mode)	V_{DD} = 22 V, V_{SS} = –22 V, V_{SELx} = V_{DR} = 0 V, 5 V, or V_{DD}, V_{EN} = 0 V	25°C		0.1	0.4	mA
			–40°C to +85°C			0.4	
			–40°C to +125°C			0.4	

(1) When V_S is positive,V_D is negative. And when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating. And when V_D is at a voltage potential, V_S is floating.

6.8 12 V Single Supply: Electrical Characteristics

V_{DD} = +12 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +12 V, V_{SS} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to 7.8 V, I_S = –10 mA	25°C		8.6	11	Ω
			–40°C to +85°C			15	
			–40°C to +125°C			18	
ΔR_{ON}	On-resistance mismatch between channels	V_S = 0 V to 7.8 V, I_S = –10 mA	25°C		0.06	0.5	Ω
			–40°C to +85°C			0.6	
			–40°C to +125°C			0.7	
R_{FLAT}	On-resistance flatness	V_S = 0 V to 7.8 V, I_S = –10 mA	25°C		0.06	0.4	Ω
			–40°C to +85°C			0.5	
			–40°C to +125°C			0.5	
R_{ON_DRIFT}	On-resistance drift	V_S = 6 V, I_S = –10 mA	–40°C to +125°C		0.04		Ω/°C
$I_{S(OFF)}$	Input leakage current(1)	V_{DD} = 13.2 V, V_{SS} = 0 V Switch state is off V_S = 10 V / 1 V V_D = 1 V / 10 V	25°C	–0.7	0.03	0.7	nA
			–40°C to +85°C	–2		2	
			–40°C to +125°C	–11		11	
$I_{D(OFF)}$	Output off leakage current(1)	V_{DD} = 13.2 V, V_{SS} = 0 V Switch state is off V_S = 10 V / 1 V V_D = 1 V / 10 V	25°C	–1.4	0.06	1.4	nA
			–40°C to +85°C	–4		4	
			–40°C to +125°C	–24		24	
$I_{S(ON)}$ $I_{D(ON)}$	Output on leakage current(2)	V_{DD} = 13.2 V, V_{SS} = 0 V Switch state is on V_S = V_D = 10 V or 1 V	25°C	–1.4	0.08	1.4	nA
			–40°C to +85°C	–4		4	
			–40°C to +125°C	–26		26	
FAULT CONDITION							
$I_{S(FA)}$	Input leakage current durring overvoltage	V_S = ± 60 V, GND = 0 V, V_{DD} = 13.2 V, V_{SS} = 0 V	–40°C to +125°C		±130		µA
$I_{S(FA)\ Grounded}$	Input leakage current during overvoltage with grounded supply voltages	V_S = ± 60 V, GND = 0 V, V_{DD} = V_{SS} = 0 V	–40°C to +125°C		±125		µA
$I_{S(FA)\ Floating}$	Input leakage current during overvoltage with floating supply voltages	V_S = ± 60 V, GND = 0 V, V_{DD} = V_{SS} = floating	–40°C to +125°C		±125		µA
$I_{D(FA)}$	Output leakage current during overvoltage	V_S = ± 60 V, GND = 0 V, V_{DD} = 13.2 V, V_{SS} = 0 V	25°C	–20	±2	20	nA
			–40°C to +85°C	–30		30	
			–40°C to +125°C	–50		50	
$I_{D(FA)\ Grounded}$	Output leakage current during overvoltage with grounded supply voltages	V_S = ± 60 V, GND = 0 V, V_{DD} = V_{SS} = 0 V	25°C	–30	±10	30	nA
			–40°C to +85°C	–50		50	
			–40°C to +125°C	–90		90	
$I_{D(FA)\ Floating}$	Output leakage current during overvoltage with floating supply voltages	V_S = ± 60 V, GND = 0 V, V_{DD} = V_{SS} = floating	25°C		±4		µA
			–40°C to +85°C		±6		
			–40°C to +125°C		±8		
I_{IH}	High-level input current	V_{EN} = V_{SELx} = V_{DR} = V_{DD}	25°C			±1.6	µA
			–40°C to +125°C			±2	
I_{IL}	Low-level input current	V_{EN} = V_{SELx} = V_{DR} = 0	25°C			±1	µA
			–40°C to +125°C			±1.1	

6.8 12 V Single Supply: Electrical Characteristics (continued)

V_{DD} = +12 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +12 V, V_{SS} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
SWITCHING CHARACTERISTICS							
$t_{ON (EN)}$	Enable turn-on time	V_S = 8 V, R_L = 300 Ω, C_L= 12 pF	25°C		350	515	ns
			–40°C to +85°C			530	
			–40°C to +125°C			550	
$t_{OFF (EN)}$	Enable turn-off time	V_S = 8 V, R_L = 300 Ω, C_L= 12 pF	25°C		85	200	ns
			–40°C to +85°C			210	
			–40°C to +125°C			210	
t_{TRAN}	Transition time	V_S = 8 V, R_L = 300 Ω, C_L= 12 pF	25°C		360	520	ns
			–40°C to +85°C			540	
			–40°C to +125°C			560	
$t_{RESPONSE}$	Fault response time	R_L = 300 Ω, C_L= 12 pF	25°C		180	765	ns
			–40°C to +85°C			765	
			–40°C to +125°C			765	
$t_{RECOVERY}$	Fault recovery time	R_L = 300 Ω, C_L= 12 pF	25°C		950	2400	ns
			–40°C to +85°C			2900	
			–40°C to +125°C			2900	
$t_{RESPONSE(FLAG)}$	Fault flag response time	R_L = 300 Ω, C_L= 12 pF, R_{PU} = 1 kΩ, C_{L_xF} = 12 pF	25°C		160		ns
$t_{RECOVERY(FLAG)}$	Fault flag recovery time	R_L = 300 Ω, C_L= 12 pF, R_{PU} = 1 kΩ, C_{L_xF} = 12 pF	25°C		0.7		µs
t_{BBM}	Break-before-make time delay	V_S = 8 V, R_L = 300 Ω, C_L= 12 pF	25°C	155	250		ns
Q_{INJ}	Charge injection	V_S = 6 V, C_L = 1 nF	25°C		–203		pC
O_{ISO}	Off-isolation	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 1 MHz	25°C		–56		dB
X_{TALK}	Intra-channel crosstalk	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 6 V, f = 1 MHz	25°C		–58		dB
	Inter-channel crosstalk	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 6 V, f = 1 MHz	25°C		–81		
BW	–3 dB bandwidth	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 0 V	25°C		213		MHz
I_{LOSS}	Insertion loss	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 1 MHz	25°C		–0.7		dB
THD+N	Total harmonic distortion plus noise	R_S = 50 Ω, R_L = 10k Ω, V_S = 6 V_{PP}, V_{BIAS} = 6 V, f = 20 Hz to 20 kHz	25°C		0.0009		%
$C_{S(OFF)}$	Input off-capacitance	f = 1 MHz, V_S = 6 V	25°C		13		pF
$C_{D(OFF)}$	Output off-capacitance	f = 1 MHz, V_S = 6 V	25°C		28		pF
$C_{S(ON)}$ $C_{D(ON)}$	Input/Output on-capacitance	f = 1 MHz, V_S = 6 V	25°C		31		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 13.2 V, V_{SS} = 0 V, V_{SELx} = V_{DR} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.3	0.5	mA
			–40°C to +85°C			0.5	
			–40°C to +125°C			0.6	mA
I_{SS}	V_{SS} supply current	V_{DD} = 13.2 V, V_{SS} = 0 V, V_{SELx} = V_{DR} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.14	0.4	mA
			–40°C to +85°C			0.4	
			–40°C to +125°C			0.4	
I_{GND}	GND current	V_{DD} = 13.2 V, V_{SS} = 0 V, V_{SELx} = V_{DR} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.06		mA
$I_{DD(FA)}$	V_{DD} supply current under fault	V_S = ± 60 V, V_{DD} = 13.2 V, V_{SS} = 0 V, V_{SELx} = V_{DR} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.25	0.6	mA
			–40°C to +85°C			0.7	
			–40°C to +125°C			0.7	

6.8 12 V Single Supply: Electrical Characteristics (continued)

V_{DD} = +12 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +12 V, V_{SS} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
$I_{SS(FA)}$	V_{SS} supply current under fault	V_S = ± 60 V, V_{DD} = 13.2 V, V_{SS} = 0 V, V_{SELx} = V_{DR} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.15	0.5	mA
			–40°C to +85°C			0.5	
			–40°C to +125°C			0.5	
$I_{GND(FA)}$	GND current under fault	V_S = ± 60 V, V_{DD} = 13.2 V, V_{SS} = 0 V, V_{SELx} = V_{DR} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.15		mA
$I_{DD(DISABLE)}$	V_{DD} supply current (disable mode)	V_{DD} = 13.2 V, V_{SS} = 0 V, V_{SELx} = V_{DR} = 0 V, 5 V, or V_{DD}, V_{EN} = 0 V	25°C		0.15	0.5	mA
			–40°C to +85°C			0.5	
			–40°C to +125°C			0.5	
$I_{SS(DISABLE)}$	V_{SS} supply current (disable mode)	V_{DD} = 13.2 V, V_{SS} = 0 V, V_{SELx} = V_{DR} = 0 V, 5 V, or V_{DD}, V_{EN} = 0 V	25°C		0.1	0.4	mA
			–40°C to +85°C			0.4	
			–40°C to +125°C			0.4	

(1) When V_S is 10 V, V_D is 1 V. Or when V_S is 1 V, V_D is 10 V.
(2) When V_S is at a voltage potential, V_D is floating. Or when V_D is at a voltage potential, V_S is floating.

6.9 36 V Single Supply: Electrical Characteristics

V_{DD} = +36 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +36 V, V_{SS} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to 30 V, I_S = –10 mA	25°C		8.6	11	Ω
			–40°C to +85°C			14	
			–40°C to +125°C			17	
ΔR_{ON}	On-resistance mismatch between channels	V_S = 0 V to 30 V, I_S = –10 mA	25°C		0.06	0.5	Ω
			–40°C to +85°C			0.6	
			–40°C to +125°C			0.7	
R_{FLAT}	On-resistance flatness	V_S = 0 V to 30 V, I_S = –10 mA	25°C		0.07	0.4	Ω
			–40°C to +85°C			0.5	
			–40°C to +125°C			0.5	
R_{ON_DRIFT}	On-resistance drift	V_S = 18 V, I_S = –1 mA	–40°C to +125°C		0.04		Ω/°C
$I_{S(OFF)}$	Input leakage current[1]	V_{DD} = 39.6 V, V_{SS} = 0 V Switch state is off V_S = 30 V / 1 V V_D = 1 V / 30 V	25°C	–0.7	0.05	0.7	nA
			–40°C to +85°C	–2		2	
			–40°C to +125°C	–11		11	
$I_{D(OFF)}$	Output off leakage current[1]	V_{DD} = 39.6 V, V_{SS} = 0 V Switch state is off V_S = 30 V / 1 V V_D = 1 V / 30 V	25°C	–1.4	0.1	1.4	nA
			–40°C to +85°C	–4		4	
			–40°C to +125°C	–24		24	
$I_{S(ON)}$ $I_{D(ON)}$	Output on leakage current[2]	V_{DD} = 39.6 V, V_{SS} = 0 V Switch state is on V_S = V_D = 30 V or 1 V	25°C	–1.4	0.15	1.4	nA
			–40°C to +85°C	–4		4	
			–40°C to +125°C	–27		27	
FAULT CONDITION							
$I_{S(FA)}$	Input leakage current durring overvoltage	V_S = 60 / –40 V, V_{DD} = 39.6 V, V_{SS} = 0 V, GND = 0 V	–40°C to +125°C		±90		µA
$I_{S(FA)\ Grounded}$	Input leakage current during overvoltage with grounded supply voltages	V_S = ± 60 V, V_{DD} = V_{SS} = 0 V, GND = 0 V	–40°C to +125°C		±125		µA
$I_{S(FA)\ Floating}$	Input leakage current during overvoltage with floating supply voltages	V_S = ± 60 V, V_{DD} = V_{SS} = floating, GND = 0 V,	–40°C to +125°C		±125		µA
$I_{D(FA)}$	Output leakage current during overvoltage	V_S = 60 / –40 V, V_{DD} = 39.6 V, V_{SS} = 0, GND = 0V	25°C	–20	±2	20	nA
			–40°C to +85°C	–30		30	
			–40°C to +125°C	–60		60	
$I_{D(FA)\ Grounded}$	Output leakage current during overvoltage with grounded supply voltages	V_S = ± 60 V, GND = 0 V, V_{DD} = V_{SS} = 0 V	25°C	–30	±10	30	nA
			–40°C to +85°C	–50		50	
			–40°C to +125°C	–90		90	
$I_{D(FA)\ Floating}$	Output leakage current during overvoltage with floating supply voltages	V_S = ± 60 V, GND = 0 V, V_{DD} = V_{SS} = floating	25°C		±4		µA
			–40°C to +85°C		±6		
			–40°C to +125°C		±8		
I_{IH}	High-level input current	V_{EN} = V_{SELx} = V_{DR} = V_{DD}	25°C			±2.7	µA
			–40°C to +125°C			±3.1	
I_{IL}	Low-level input current	V_{EN} = V_{SELx} = V_{DR} = 0	25°C			±1	µA
			–40°C to +125°C			±1.1	

6.9 36 V Single Supply: Electrical Characteristics (continued)

V_{DD} = +36 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +36 V, V_{SS} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
SWITCHING CHARACTERISTICS							
$t_{ON (EN)}$	Enable turn-on time	V_S = 18 V, R_L = 300 Ω, C_L= 12 pF	25°C		370	520	ns
			–40°C to +85°C			550	
			–40°C to +125°C			560	
$t_{OFF (EN)}$	Enable turn-off time	V_S = 18 V, R_L = 300 Ω, C_L= 12 pF	25°C		100	210	ns
			–40°C to +85°C			230	
			–40°C to +125°C			230	
t_{TRAN}	Transition time	V_S = 18 V, R_L = 300 Ω, C_L= 12 pF	25°C		365	540	ns
			–40°C to +85°C			560	
			–40°C to +125°C			570	
$t_{RESPONSE}$	Fault response time	R_L = 300 Ω, C_L= 12 pF	25°C		120	340	ns
			–40°C to +85°C			360	
			–40°C to +125°C			385	
$t_{RECOVERY}$	Fault recovery time	R_L = 300 Ω, C_L= 12 pF	25°C		1250	2350	ns
			–40°C to +85°C			2850	
			–40°C to +125°C			2850	
$t_{RESPONSE(FLAG)}$	Fault flag response time	R_L = 300 Ω, C_L= 12 pF, R_{PU} = 1 kΩ, C_{L_xF} = 12 pF	25°C		100		ns
$t_{RECOVERY(FLAG)}$	Fault flag recovery time	R_L = 300 Ω, C_L= 12 pF, R_{PU} = 1 kΩ, C_{L_xF} = 12 pF	25°C		1		µs
t_{BBM}	Break-before-make time delay	V_S = 18 V, R_L = 300 Ω, C_L= 12 pF	25°C	160	270		ns
Q_{INJ}	Charge injection	V_S = 18 V, C_L = 1 nF	25°C		–300		pC
O_{ISO}	Off-isolation	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 6 V, f = 1 MHz	25°C		–56		dB
X_{TALK}	Intra-channel crosstalk	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 6 V, f = 1 MHz	25°C		–59		dB
	Inter-channel crosstalk	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 6 V, f = 1 MHz	25°C		–80		
BW	–3 dB bandwidth	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 6 V	25°C		215		MHz
I_{LOSS}	Insertion loss	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 6 V, f = 1 MHz	25°C		–0.7		dB
THD+N	Total harmonic distortion plus noise	R_S = 50 Ω, R_L = 10 kΩ, V_S = 18 V_{PP}, V_{BIAS} = 18 V, f = 20 Hz to 20 kHz	25°C		0.0008		%
$C_{S(OFF)}$	Input off-capacitance	f = 1 MHz, V_S = 18 V	25°C		14		pF
$C_{D(OFF)}$	Output off-capacitance	f = 1 MHz, V_S = 18 V	25°C		28		pF
$C_{S(ON)}$ $C_{D(ON)}$	Input/Output on-capacitance	f = 1 MHz, V_S = 18 V	25°C		31		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 39.6 V, V_{SS} = 0 V, V_{SELx} = V_{DR} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.3	0.5	mA
			–40°C to +85°C			0.5	
			–40°C to +125°C			0.6	
I_{SS}	V_{SS} supply current	V_{DD} = 39.6 V, V_{SS} = 0 V, V_{SELx} = V_{DR} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.14	0.4	mA
			–40°C to +85°C			0.4	
			–40°C to +125°C			0.4	
I_{GND}	GND current	V_{DD} = 39.6 V, V_{SS} = 0 V, V_{SELx} = V_{DR} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.06		mA
$I_{DD(FA)}$	V_{DD} supply current under fault	V_S = 60 / –40 V, V_{DD} = 39.6 V, V_{SS} = 0 V, V_{SELx} = V_{DR} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.25	1.2	mA
			–40°C to +85°C			1.6	
			–40°C to +125°C			1.6	

6.9 36 V Single Supply: Electrical Characteristics (continued)

V_{DD} = +36 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +36 V, V_{SS} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
$I_{SS(FA)}$	V_{SS} supply current under fault	V_S = 60 / –40 V, V_{DD} = 39.6 V, V_{SS} = 0 V, V_{SELx} = V_{DR} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.15	0.5	mA
			–40°C to +85°C			0.5	
			–40°C to +125°C			0.5	
$I_{GND(FA)}$	GND current under fault	V_S = 60 / –40 V, V_{DD} = 39.6 V, V_{SS} = 0 V, V_{SELx} = V_{DR} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.1		mA
$I_{DD(DISABLE)}$	V_{DD} supply current (disable mode)	V_{DD} = 39.6 V, V_{SS} = 0 V, V_{SELx} = V_{DR} = 0 V, 5 V, or V_{DD}, V_{EN} = 0 V	25°C		0.15	0.5	mA
			–40°C to +85°C			0.5	
			–40°C to +125°C			0.5	
$I_{SS(DISABLE)}$	V_{SS} supply current (disable mode)	V_{DD} = 39.6 V, V_{SS} = 0 V, V_{SELx} = V_{DR} = 0 V, 5 V, or V_{DD}, V_{EN} = 0 V	25°C		0.1	0.4	mA
			–40°C to +85°C			0.4	
			–40°C to +125°C			0.4	

(1) When V_S is 30 V, V_D is 1 V. Or when V_S is 1 V, V_D is 30 V.
(2) When V_S is at a voltage potential, V_D is floating. Or when V_D is at a voltage potential, V_S is floating.

6.10 Typical Characteristics

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)

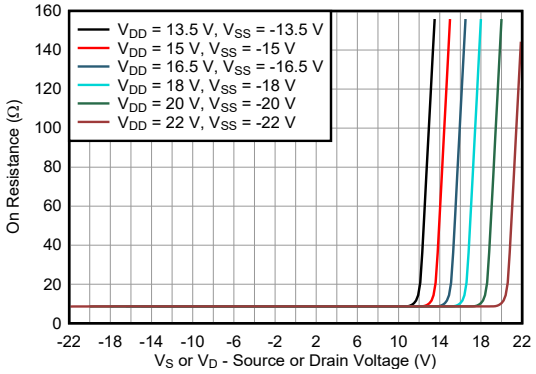


Figure 6-1. On-Resistance vs Source or Drain Voltage

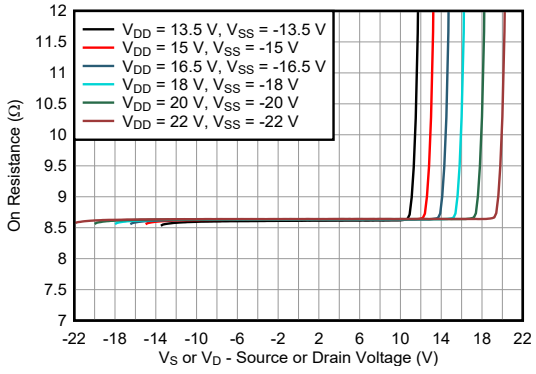


Figure 6-2. On-Resistance vs Source or Drain Voltage

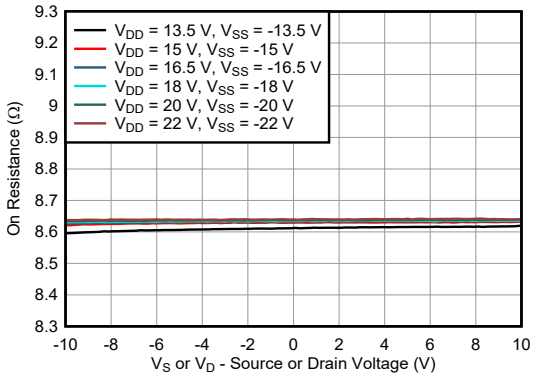


Figure 6-3. On-Resistance vs Source or Drain Voltage

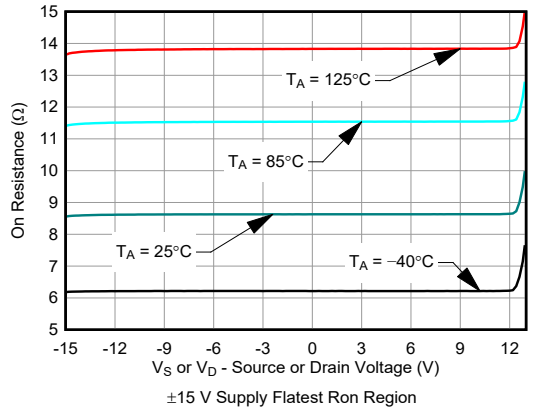


Figure 6-4. On-Resistance vs Source or Drain Voltage

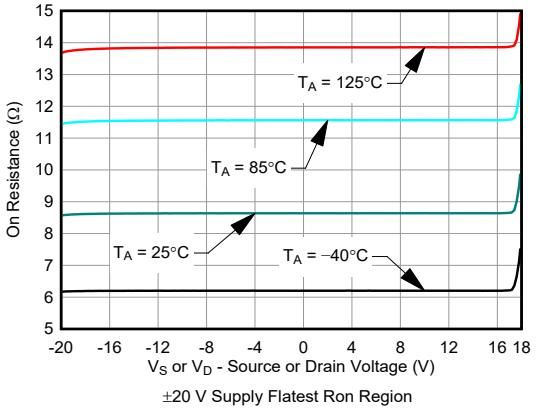


Figure 6-5. On-Resistance vs Source or Drain Voltage

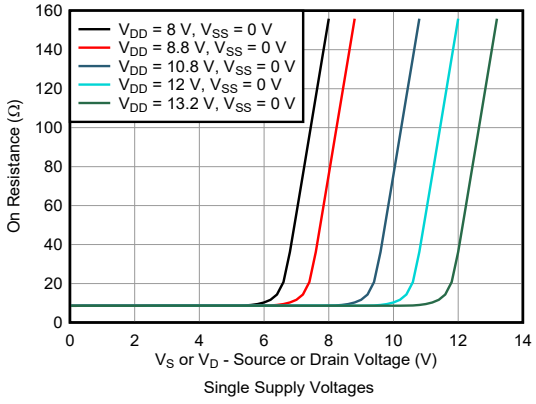


Figure 6-6. On-Resistance vs Source or Drain Voltage

6.10 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)

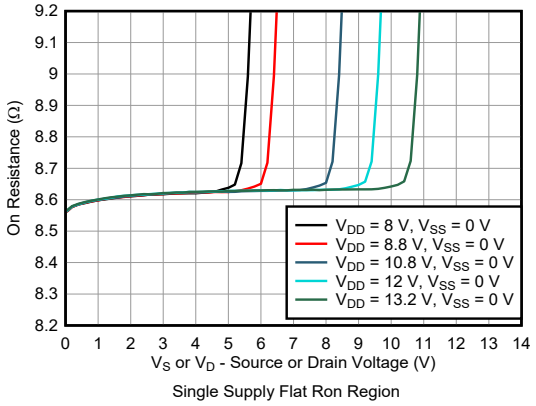


Figure 6-7. On-Resistance vs Source or Drain Voltage

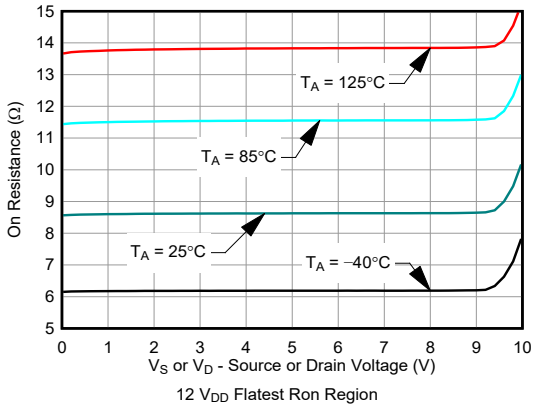


Figure 6-8. On-Resistance vs Source or Drain Voltage

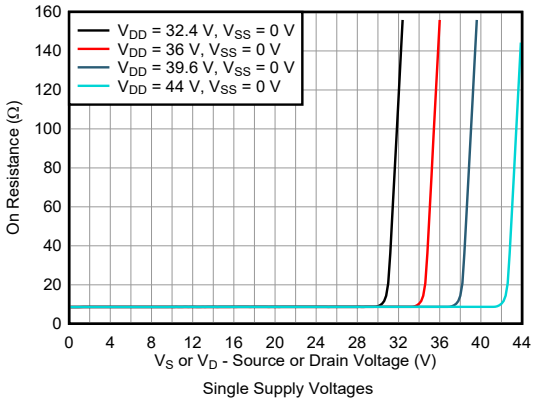


Figure 6-9. On-Resistance vs Source or Drain Voltage

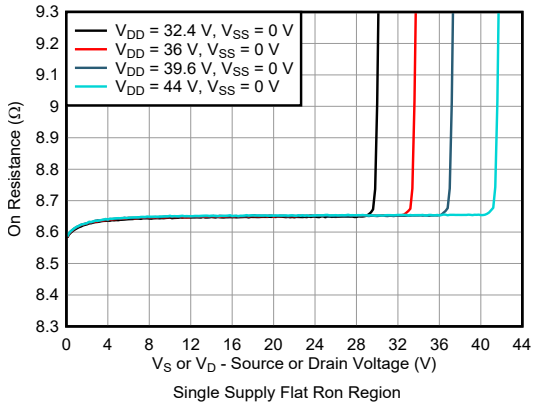


Figure 6-10. On-Resistance vs Source or Drain Voltage

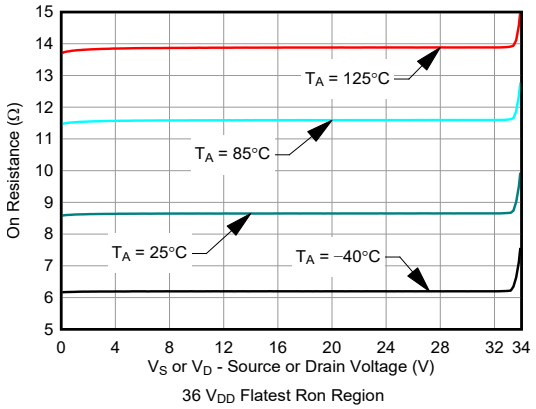


Figure 6-11. On-Resistance vs Source or Drain Voltage

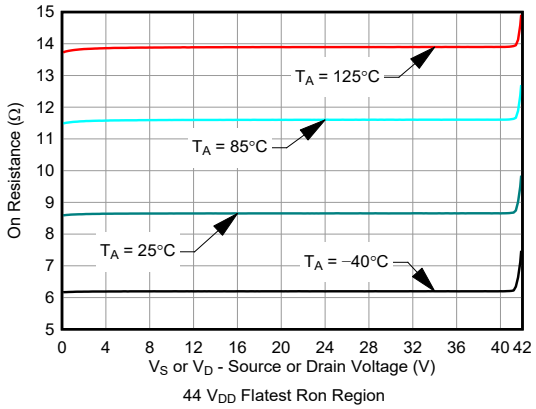


Figure 6-12. On-Resistance vs Source or Drain Voltage

6.10 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)

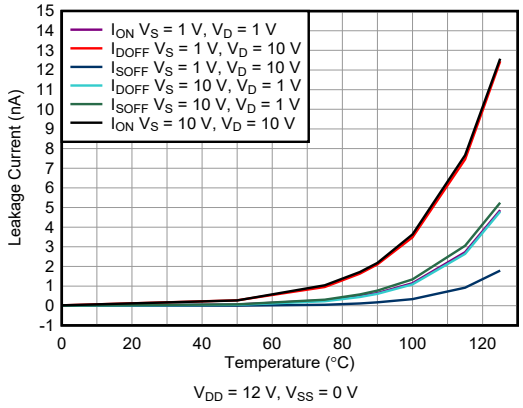


Figure 6-13. Leakage Current vs Temperature

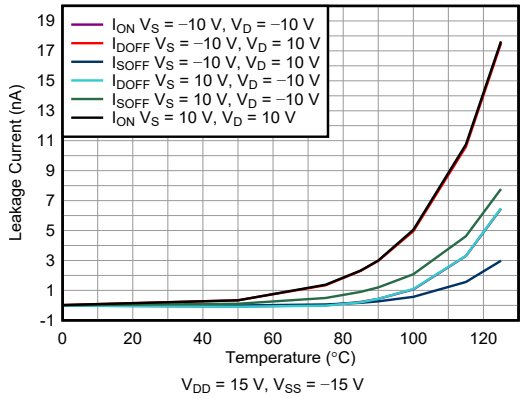


Figure 6-14. Leakage Current vs Temperature

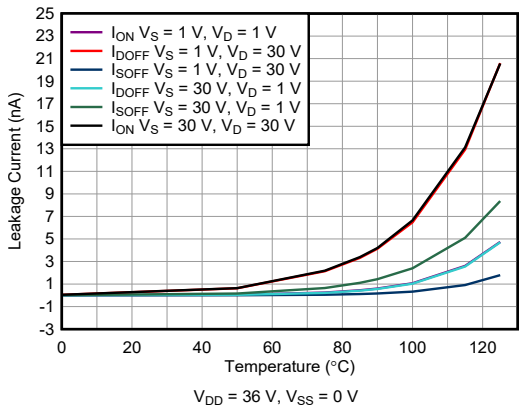


Figure 6-15. Leakage Current vs Temperature

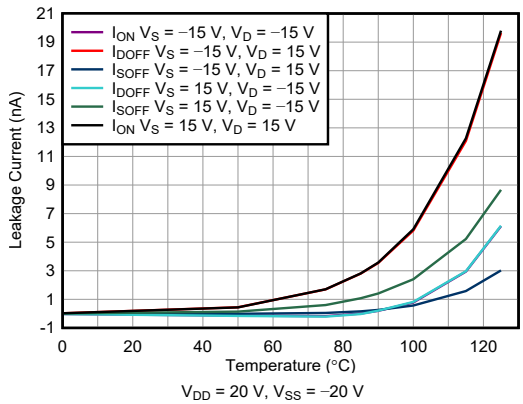


Figure 6-16. Leakage Current vs Temperature

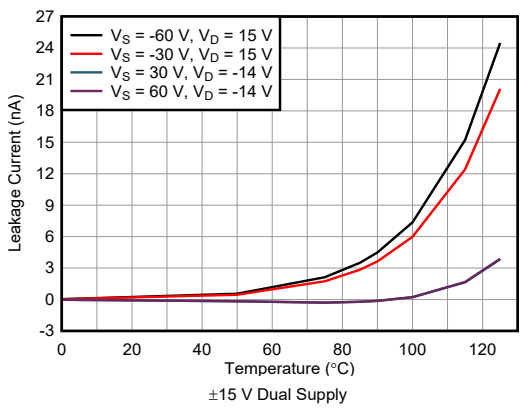


Figure 6-17. $I_{D(FA)}$ Overvoltage Leakage Current vs Temperature

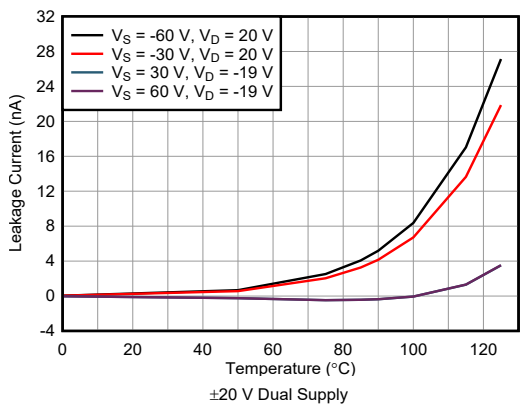


Figure 6-18. $I_{D(FA)}$ Overvoltage Leakage Current vs Temperature

6.10 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)

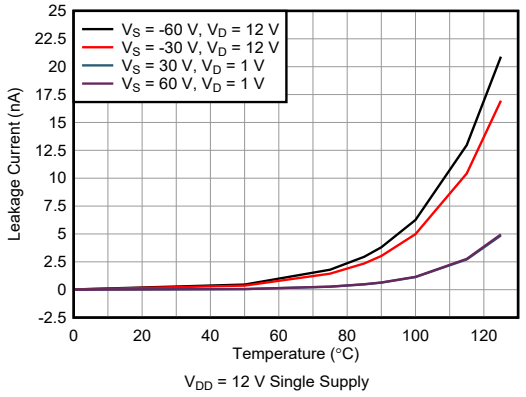


Figure 6-19. $I_{D(FA)}$ Overvoltage Leakage Current vs Temperature

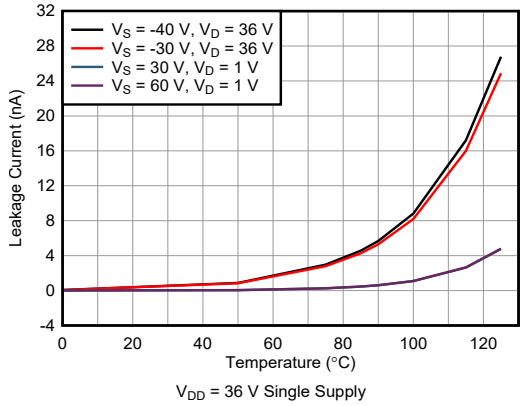


Figure 6-20. $I_{D(FA)}$ Overvoltage Leakage Current vs Temperature

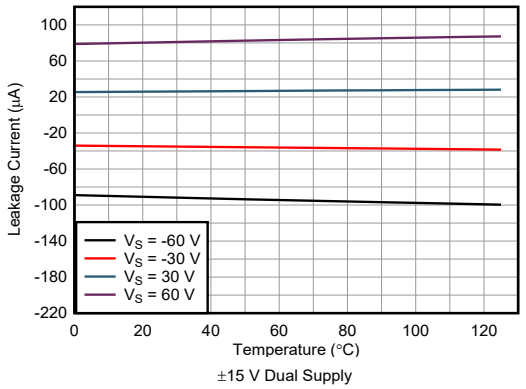


Figure 6-21. $I_{S(FA)}$ Overvoltage Leakage Current vs Temperature

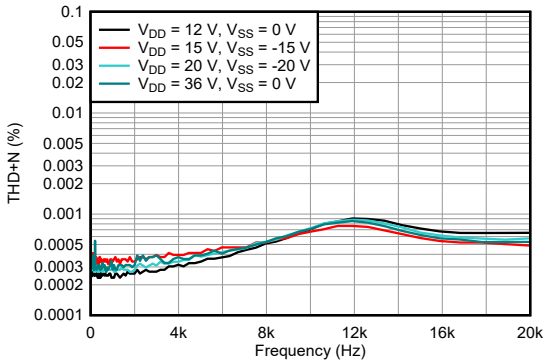


Figure 6-22. THD+N vs Frequency

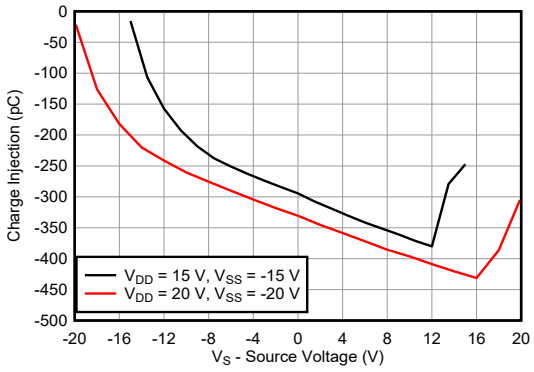


Figure 6-23. Charge Injection vs Source Voltage – Dual Supply

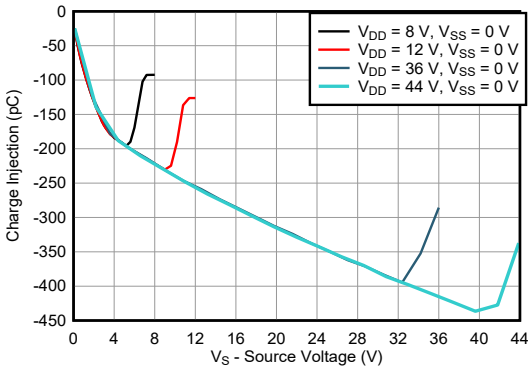


Figure 6-24. Charge Injection vs Source Voltage – Single Supply

6.10 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)

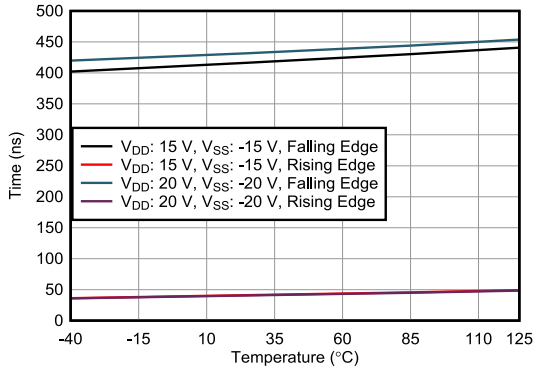


Figure 6-25. Transition Times vs Temperature

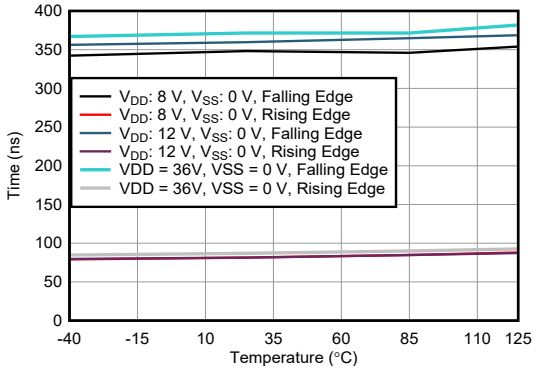


Figure 6-26. Transition Times vs Temperature

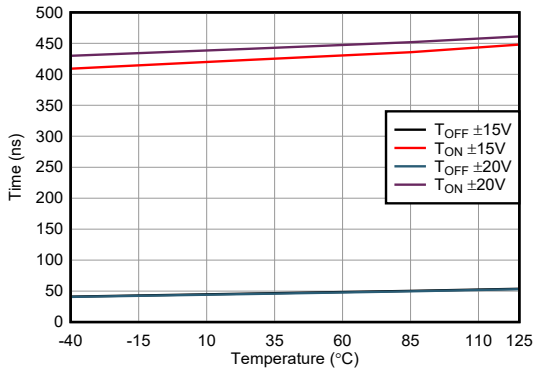


Figure 6-27. Turn-On and Turn-Off Times vs Temperature

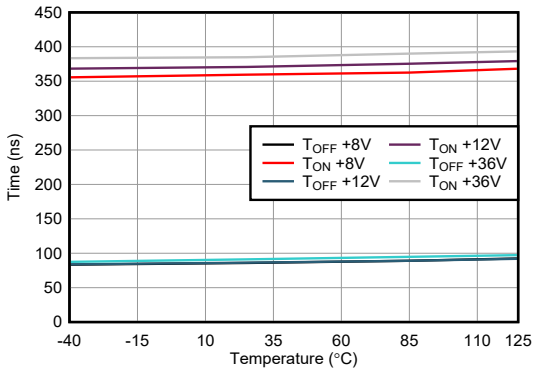


Figure 6-28. Turn-On and Turn-Off Times vs Temperature

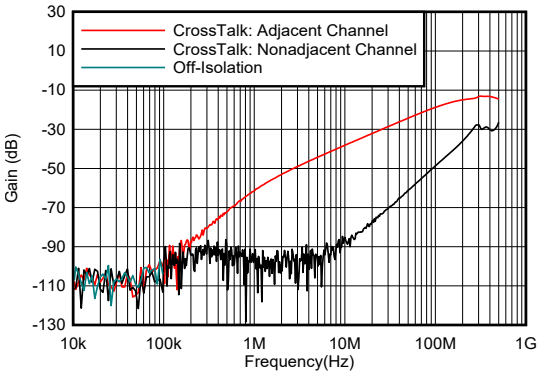


Figure 6-29. Crosstalk and Off Isolation vs Frequency

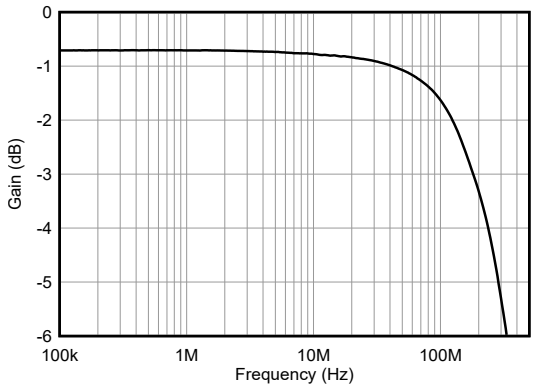


Figure 6-30. Insertion Loss vs Frequency

6.10 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)

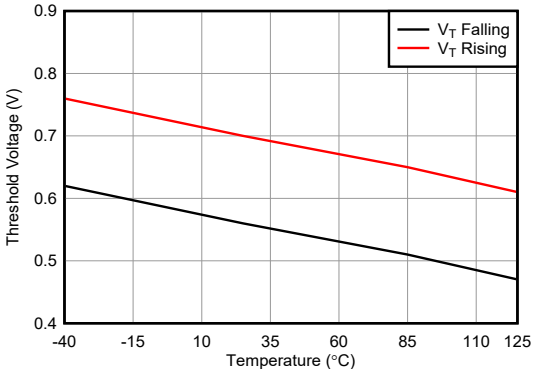


Figure 6-31. Threshold Voltage vs Temperature

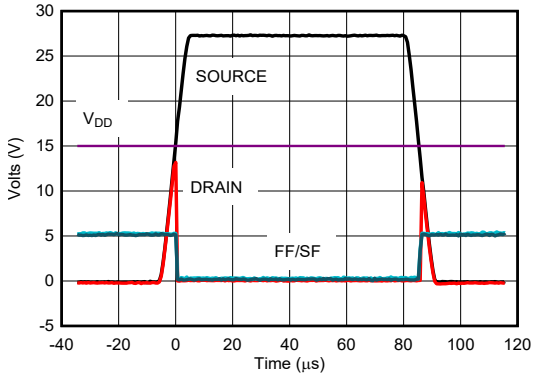


Figure 6-32. Fault Response and Recovery

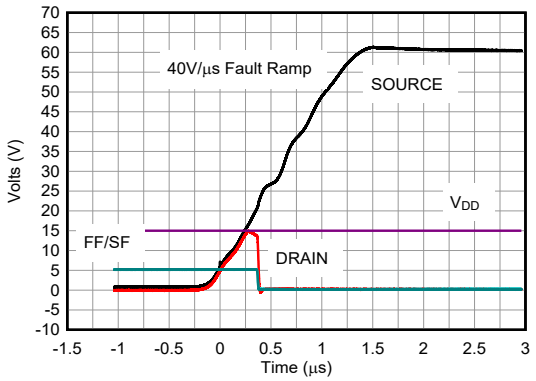


Figure 6-33. Drain Output Response – Positive Overvoltage

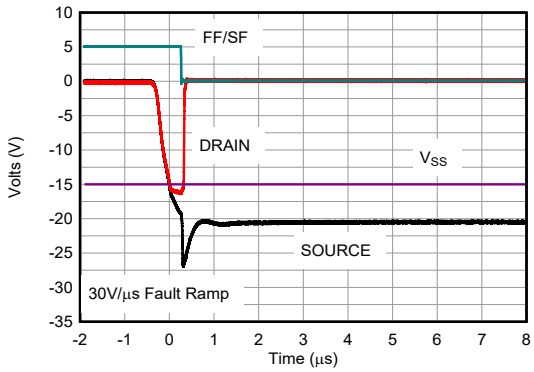


Figure 6-34. Drain Output Response – Negative Overvoltage

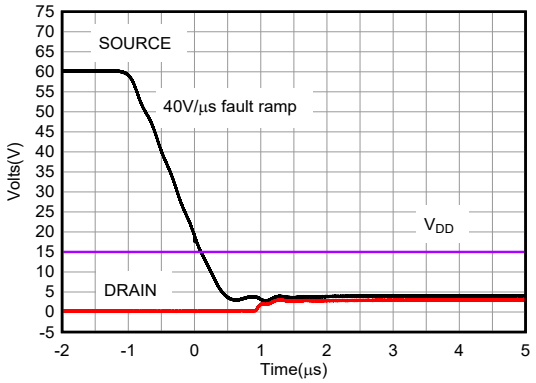


Figure 6-35. Drain Output Recovery – Positive Overvoltage

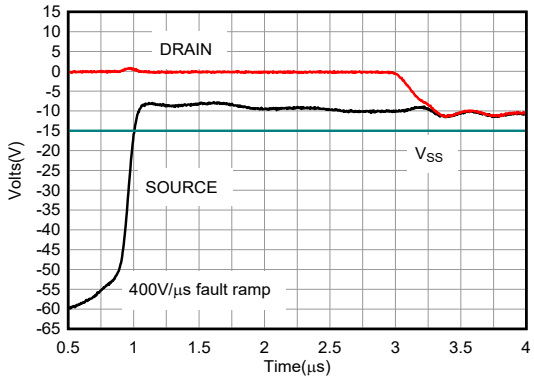


Figure 6-36. Drain Output Recovery – Negative Overvoltage

7 Parameter Measurement Information

7.1 On-Resistance

The on-resistance of the TMUX7436F is the ohmic resistance across the source (Sx) and drain (Dx) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. Figure 7-1 shows the measurement setup used to measure R_{ON}. ΔR_{ON} represents the difference between the R_{ON} of any two channels, while R_{ON_FLAT} denotes the flatness that is defined as the difference between the maximum and minimum value of on-resistance measured over the specified analog signal range.

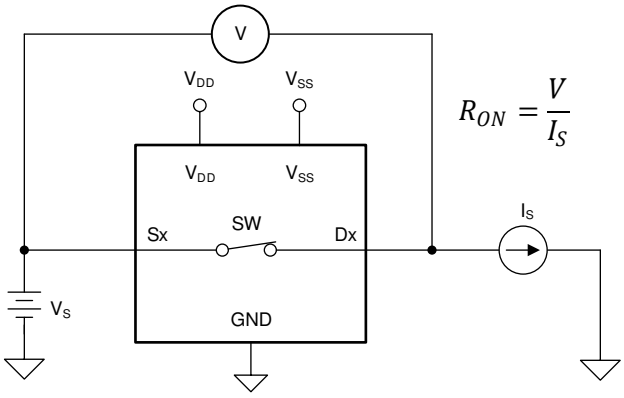


Figure 7-1. On-Resistance Measurement Setup

7.2 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

1. Source off-leakage current $I_{S(OFF)}$: the leakage current flowing into or out of the source pin when the switch is off.
2. Drain off-leakage current $I_{D(OFF)}$: the leakage current flowing into or out of the drain pin when the switch is off.

Figure 7-2 shows the setup used to measure both off-leakage currents.

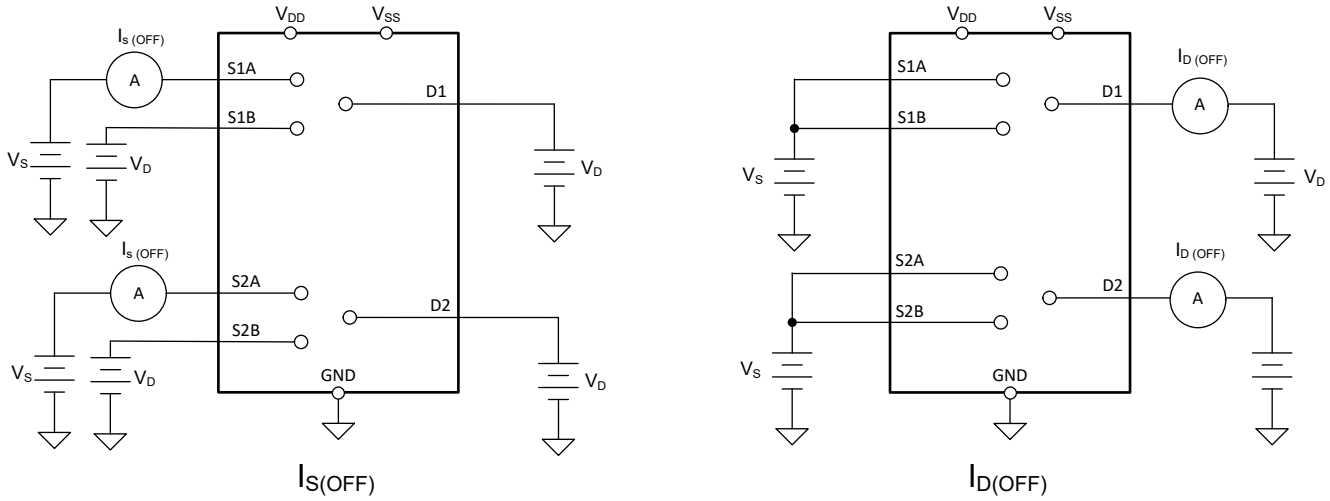


Figure 7-2. Off-Leakage Measurement Setup

7.3 On-Leakage Current

Source on-leakage current ($I_{S(ON)}$) and drain on-leakage current ($I_{D(ON)}$) denote the channel leakage currents when the switch is in the on state. $I_{S(ON)}$ is measured with the drain floating, while $I_{D(ON)}$ is measured with the source floating. Figure 7-3 shows the circuit used for measuring the on-leakage currents.

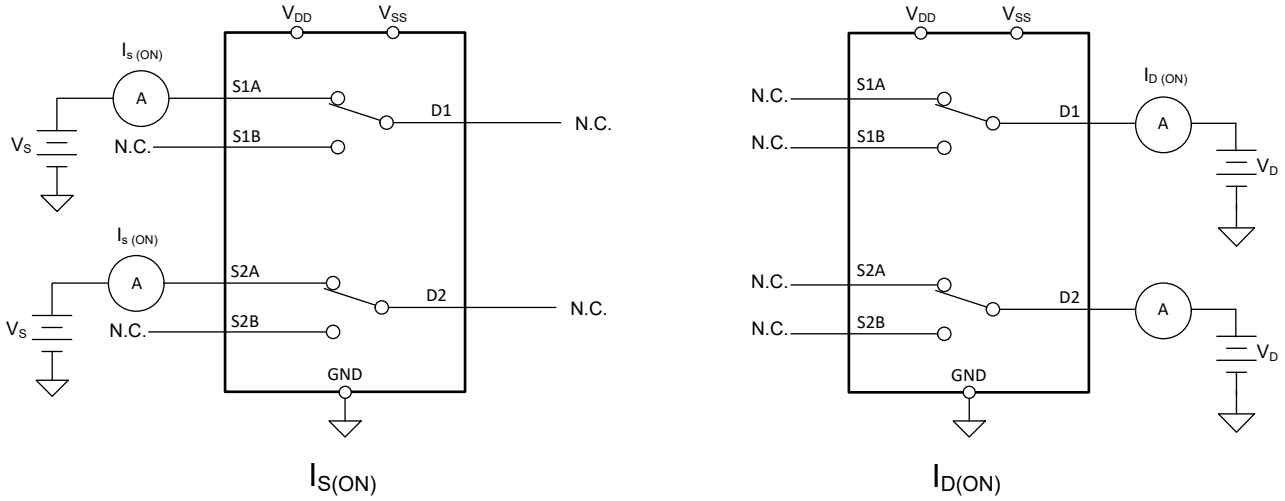


Figure 7-3. On-Leakage Measurement Setup

7.4 Input and Output Leakage Current Under Overvoltage Fault

If any of the source pin voltage goes above the supplies (V_{DD} or V_{SS}) by one threshold voltage (V_T), then the overvoltage protection feature of the TMUX7436F is triggered to turn off the switch under fault, keeping the fault channel in a high-impedance state. $I_{S(FA)}$ and $I_{D(FA)}$ denotes the input and output leakage current under overvoltage fault conditions, respectively. When the overvoltage fault occurs, the supply (or supplies) can either be in normal operating condition (Figure 7-4) or abnormal operating condition (Figure 7-5). During abnormal operating condition, the supply (or supplies) can either be unpowered (V_{DD}= V_{SS} = 0 V) or floating (V_{DD}= V_{SS} = no connection), and remains within the leakage performance specifications.

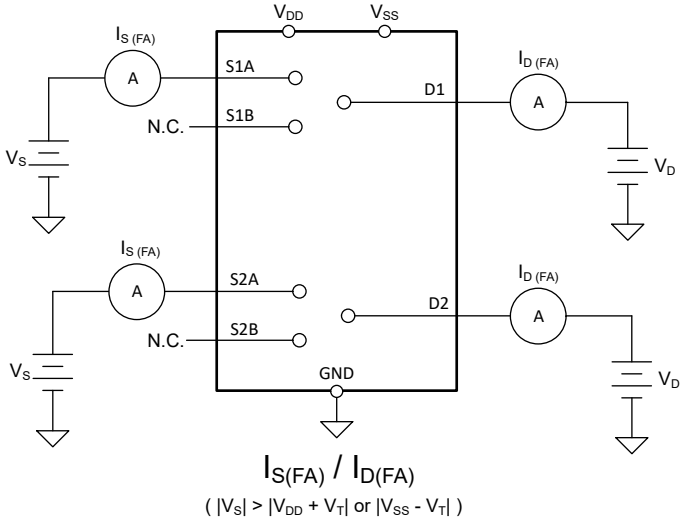


Figure 7-4. Measurement Setup for Input and Output Leakage Current under Overvoltage Fault With Normal Supplies

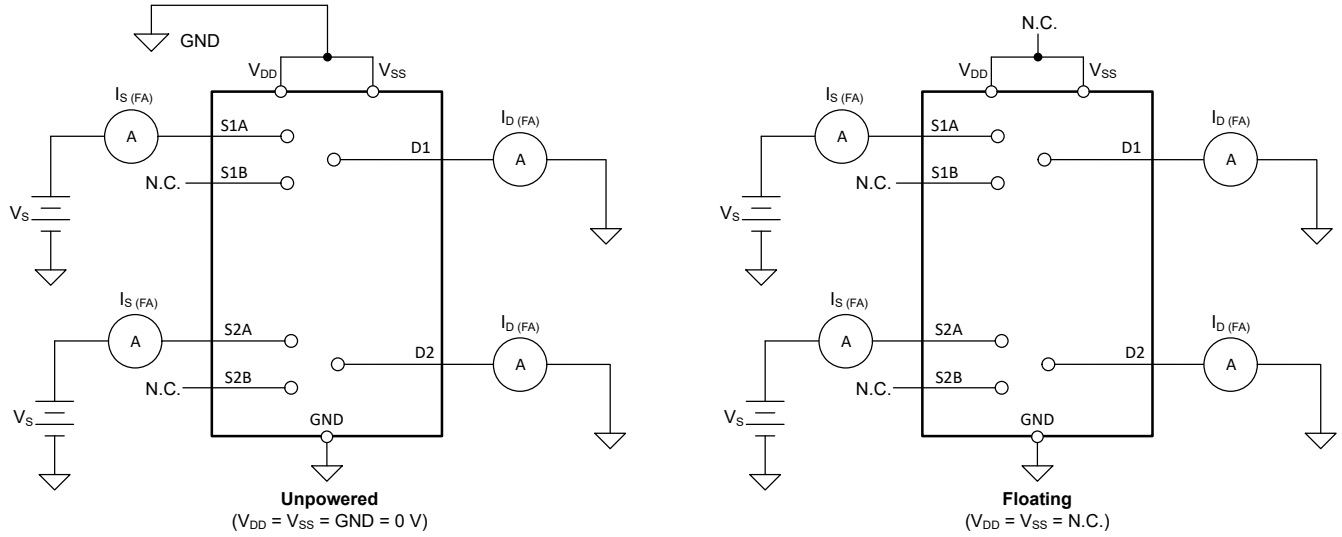


Figure 7-5. Measurement Setup for Input and Output Leakage Current under Overvoltage Fault With Unpowered or Floating Supplies

7.5 Enable Delay Time

$t_{ON(EN)}$ is defined as the time taken by the output of the TMUX7436F to rise to a 90% final value after the EN signal has past the 50% threshold. $t_{OFF(EN)}$ is defined as the time taken by the output of the TMUX7436F to fall to a 10% initial value after the EN signal has past the 50% threshold. Figure 7-6 shows the setup used to measure t_{ON} and t_{OFF}.

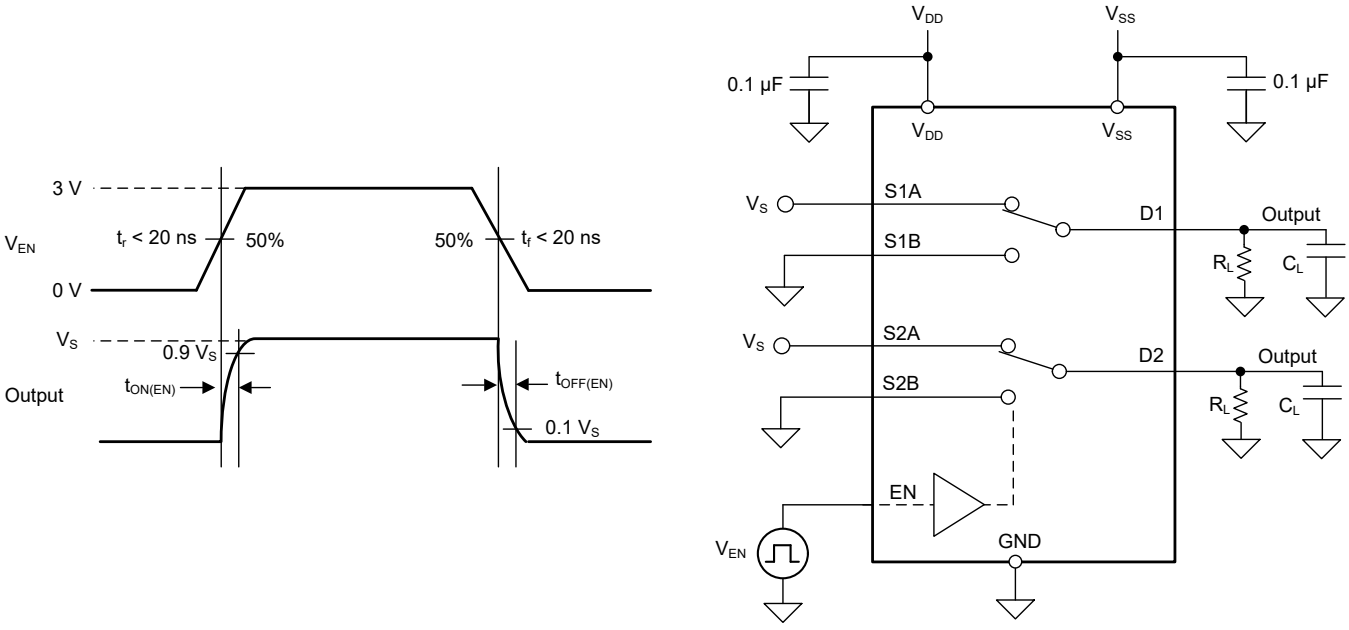


Figure 7-6. Enable Delay Measurement Setup

7.6 Break-Before-Make Delay

The break-before-make delay is a safety feature of the TMUX7436F switch. The ON switches of the TMUX7436F first break the connection before the OFF switches make connection. The time delay between the break and the make is known as break-before-make delay. Figure 7-7 shows the setup used to measure break-before-make delay, denoted by the symbol t_{BBM}.

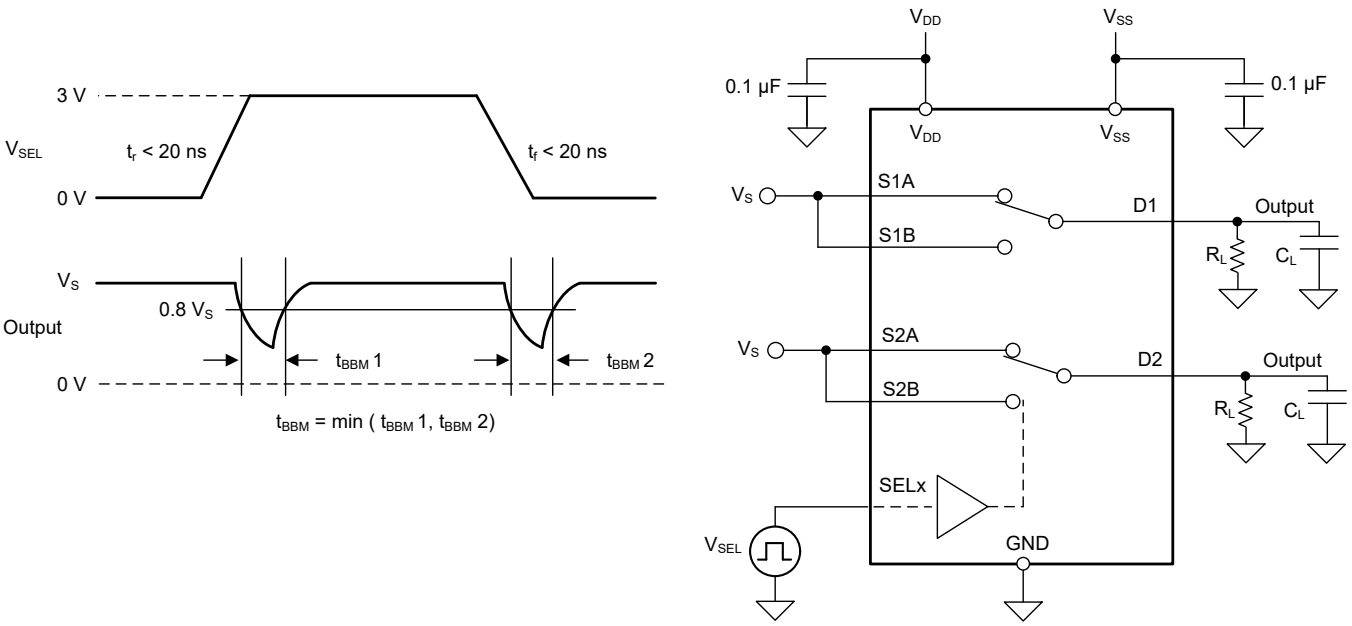


Figure 7-7. Break-Before-Make Delay Measurement Setup

7.7 Transition Time

Transition time is defined as the time taken by the output of the device to rise (to 90% of the transition) or fall (to 10% of the transition) after the select signal (SELx) has fallen or risen to 50% of the transition. Figure 7-8 shows the setup used to measure transition time, denoted by the symbol t_{TRAN}.

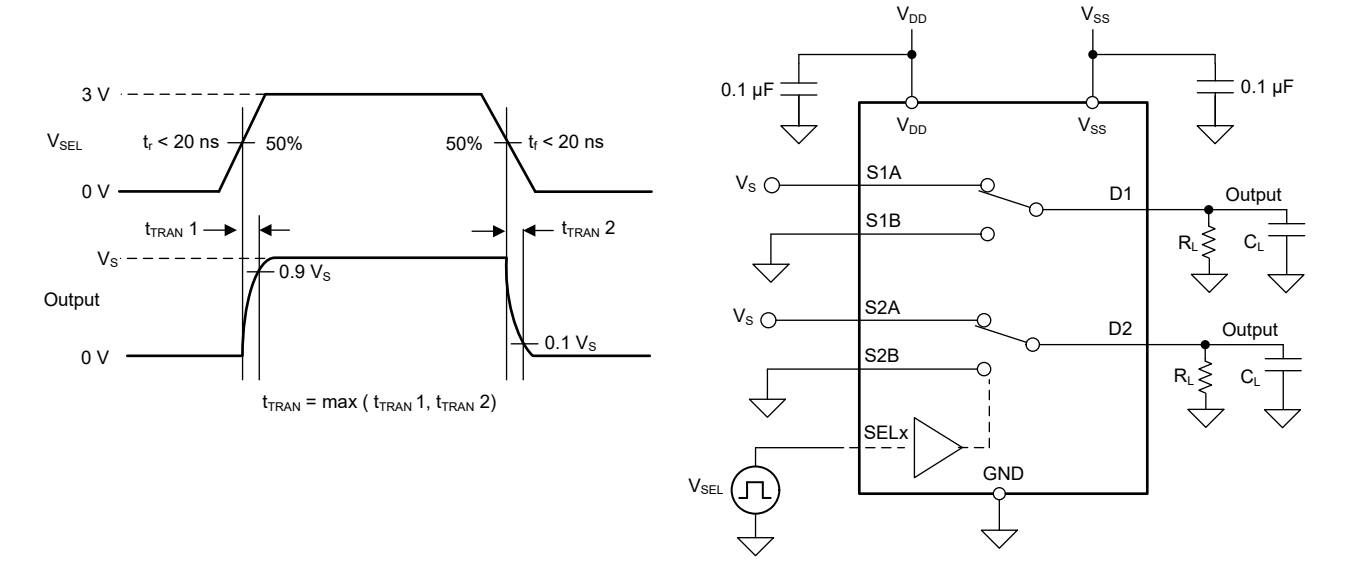


Figure 7-8. Transition Time Measurement Setup

7.8 Fault Response Time

Fault response time ($t_{RESPONSE}$) measures the delay between the source voltage exceeding the supply voltage (V_{DD} or V_{SS}) by 0.5 V and the drain voltage failing to 50% of the maximum output voltage. Figure 7-9 shows the setup used to measure $t_{RESPONSE}$.

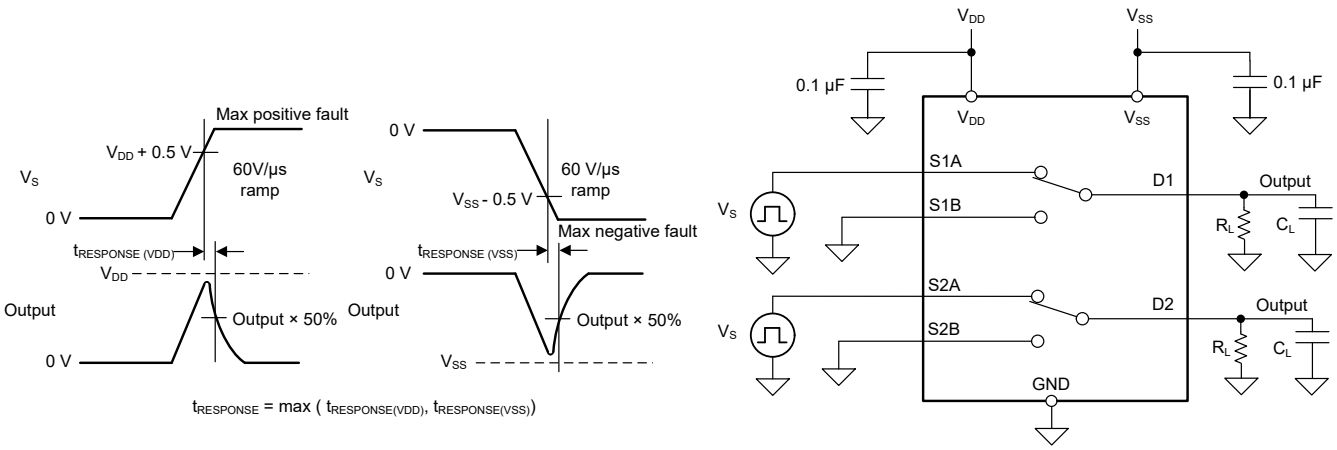


Figure 7-9. Fault Response Time Measurement Setup

7.9 Fault Recovery Time

Fault recovery time ($t_{RECOVERY}$) measures the delay between the source voltage falling from overvoltage condition to below supply voltage (V_{DD} or V_{SS}) plus 0.5 V and the drain voltage rising from 0 V to 50% of the final output voltage. Figure 7-10 shows the setup used to measure $t_{RECOVERY}$.

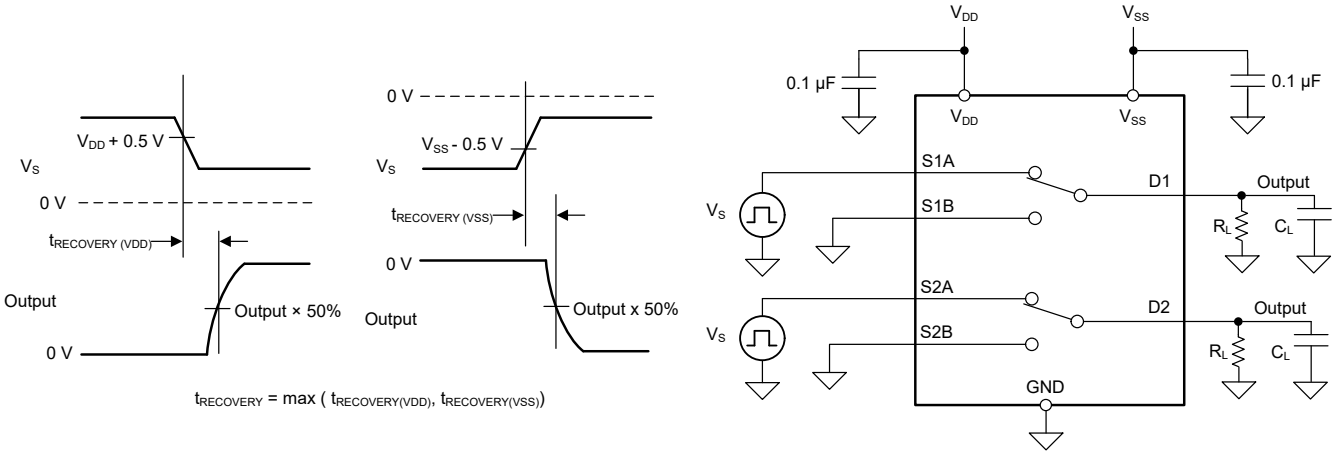


Figure 7-10. Fault Recovery Time Measurement Setup

7.10 Fault Flag Response Time

Fault flag response time ($t_{RESPONSE(FLAG)}$) measures the delay between the source voltage exceeding the fault supply voltage (V_{DD} or V_{SS}) by 0.5 V and the general fault flag (FF) pin to go below 10% of its original value. Figure 7-11 shows the setup used to measure $t_{RESPONSE(FLAG)}$.

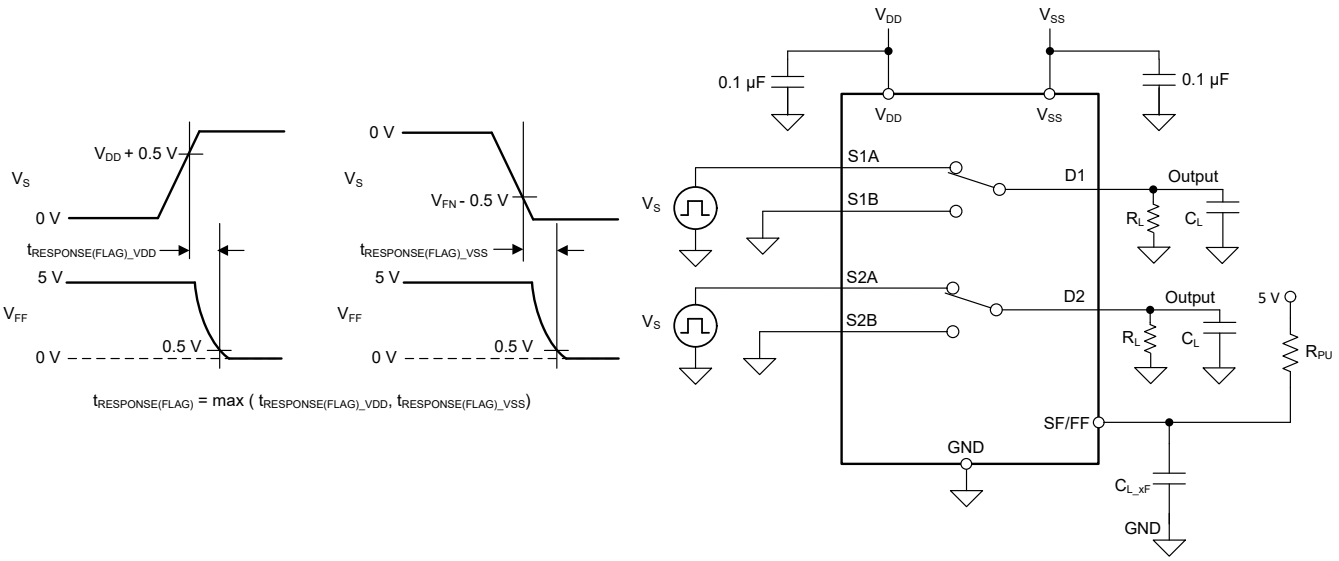


Figure 7-11. Fault Flag Response Time Measurement Setup

7.11 Fault Flag Recovery Time

Fault flag recovery time ($t_{RECOVERY(FLAG)}$) measures the delay between the source voltage falling from overvoltage condition to below fault supply voltage (V_{DD} or V_{SS}) plus 0.5 V and the general fault flag (FF) pin to rise above 3 V with 5 V external pull-up. Figure 7-12 shows the setup used to measure $t_{RECOVERY(FLAG)}$.

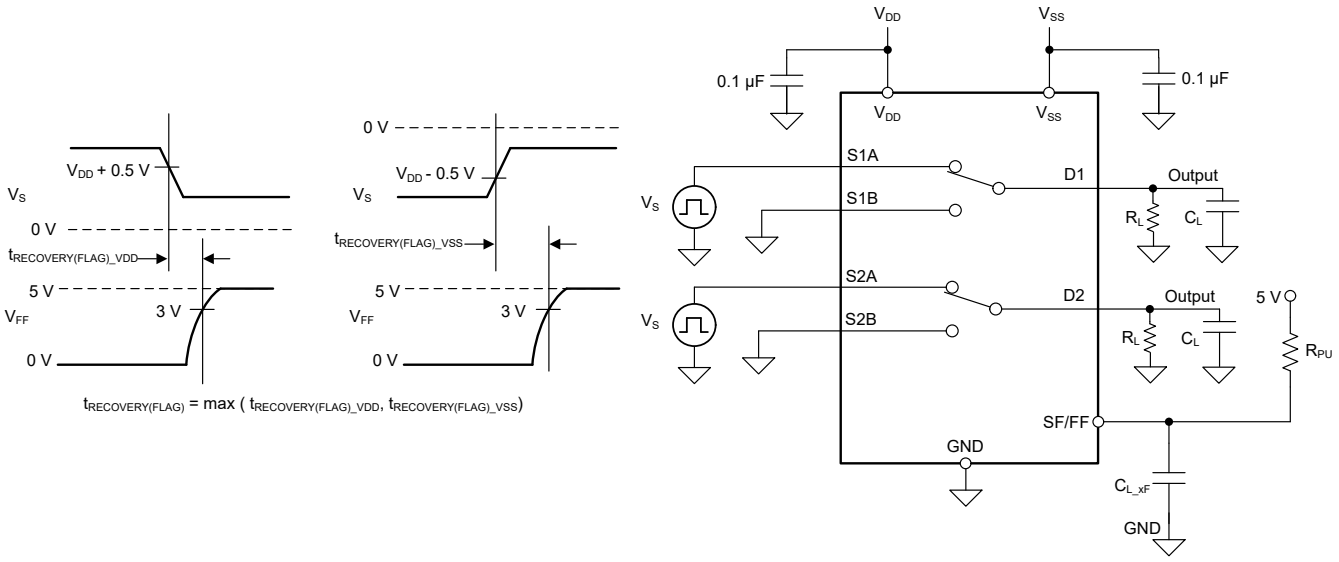


Figure 7-12. Fault Flag Recovery Time Measurement Setup

7.12 Charge Injection

Charge injection is a measure of the glitch impulse transferred from the logic input to the signal path during logic pin switching, and is denoted by the symbol Q_{INJ}. Figure 7-13 shows the setup used to measure charge injection from the source to drain.

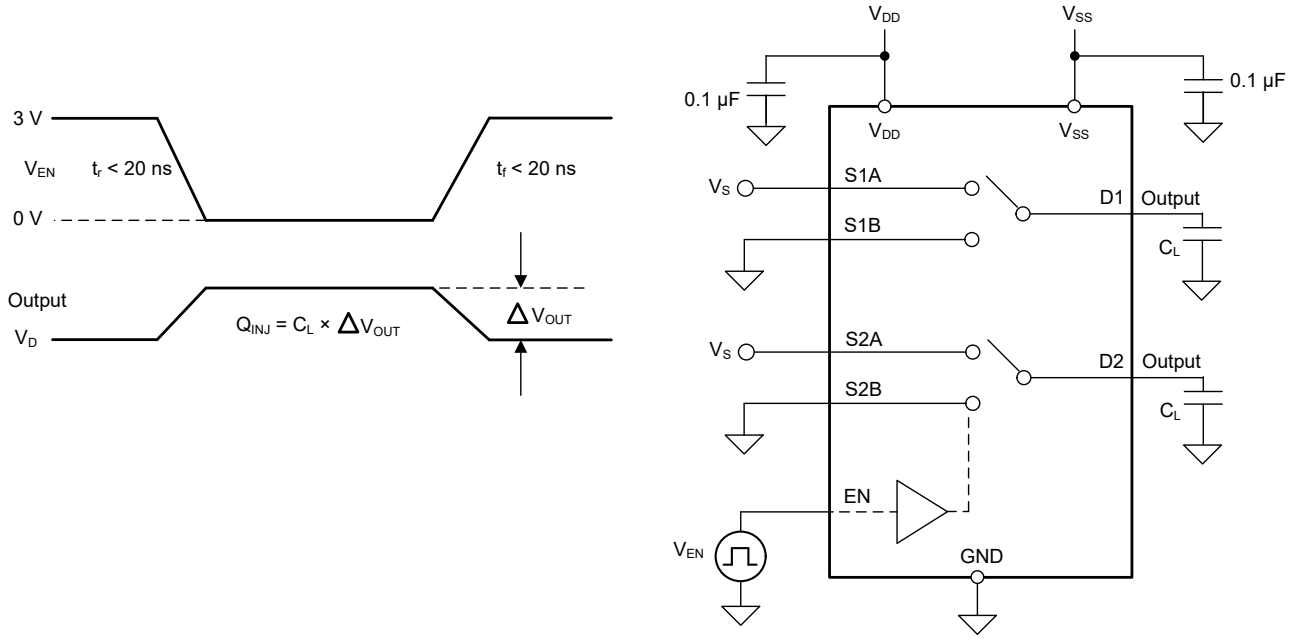


Figure 7-13. Charge-Injection Measurement Setup

7.13 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (Dx) of the device when a signal is applied to the source pin (Sx) of an off-channel. Figure 7-14 shows the setup used to measure off isolation.

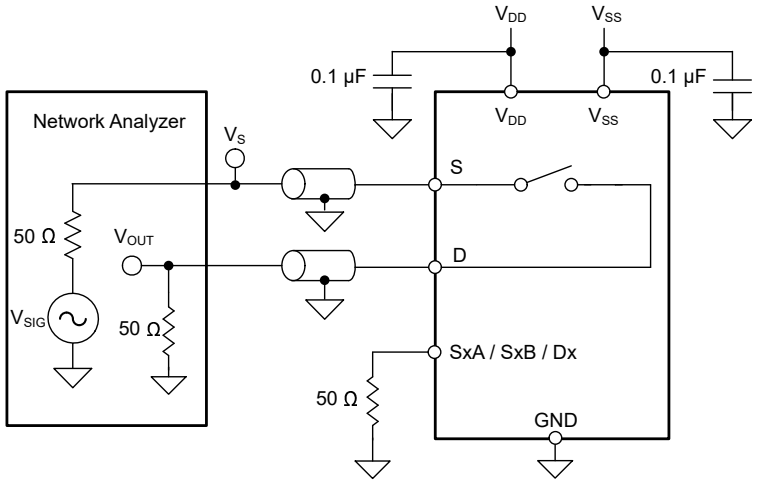


Figure 7-14. Off Isolation Measurement Setup

7.14 Crosstalk

The following are two types of crosstalk that can be defined for the devices:

1. Intra-channel crosstalk ($X_{TALK(INTRA)}$): the voltage at the source pin (Sx) of an off-switch input, when a 1-V_{RMS} signal is applied at the source pin of an on-switch input in the same channel, as shown in Figure 7-15.
2. Inter-channel crosstalk ($X_{TALK(INTER)}$): the voltage at the source pin (Sx) of an on-switch input, when a 1-V_{RMS} signal is applied at the source pin of an on-switch input in a different channel, as shown in Figure 7-16.

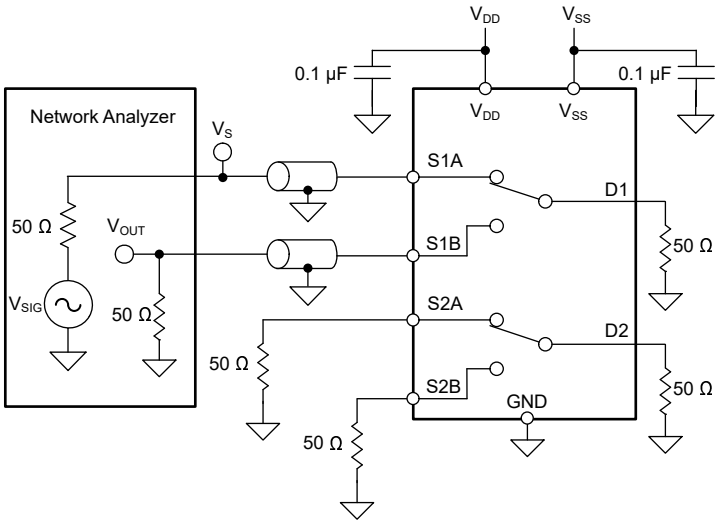


Figure 7-15. Intra-Channel Crosstalk Measurement Setup

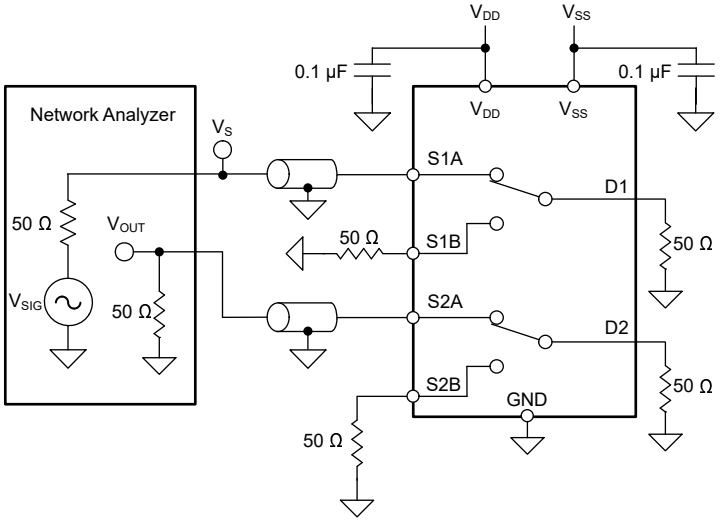


Figure 7-16. Inter-Channel Crosstalk Measurement Setup

7.15 Bandwidth

Bandwidth (BW) is defined as the range of frequencies that are attenuated by < 3 dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (Dx) of the device. Figure 7-17 shows the setup used to measure bandwidth of the switch.

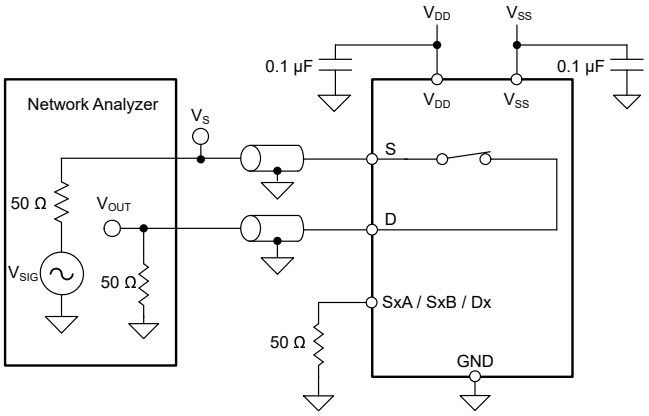


Figure 7-17. Bandwidth Measurement Setup

7.16 THD + Noise

The total harmonic distortion (THD) of a signal is a measurement of the harmonic distortion, and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency at the switch output. The on-resistance of the device varies with the amplitude of the input signal and results in distortion when the drain pin is connected to a low-impedance load. Total harmonic distortion plus noise is denoted as THD+N. Figure 7-18 shows the setup used to measure THD+N of the devices.

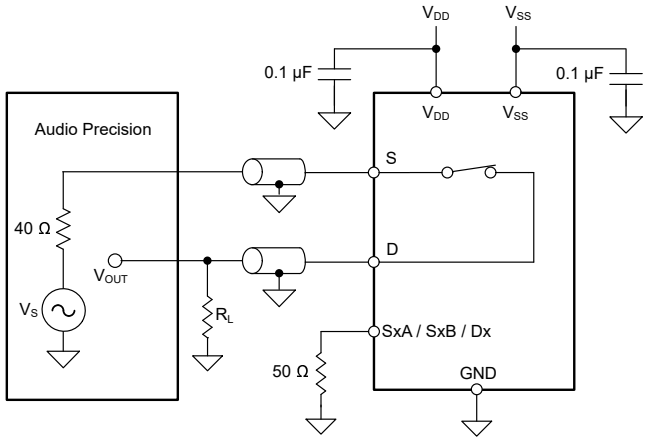


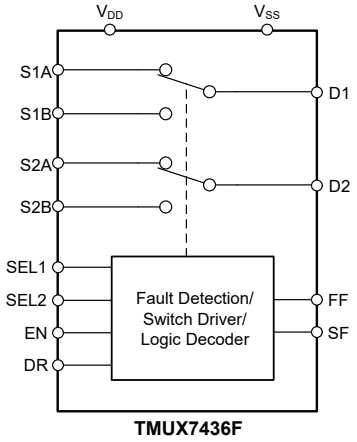
Figure 7-18. THD+N Measurement Setup

8 Detailed Description

8.1 Overview

The TMUX7436F device is a 44-V fault protected multiplexer with latch-up immunity in a 2:1, 2 channel configuration. The device works well with dual supplies (±5 V to ±22 V), a single supply (8 V to 44 V), or asymmetric supplies (such as VDD = 15 V, VSS = –5 V). The overvoltage protection feature on the source pins works under powered and powered-off conditions, allowing for use in harsh industrial environments. The powered-off condition includes floating power supplies, grounded power supplies, or power supplies at any level that are below the undervoltage (UV) threshold.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Flat ON-Resistance

The TMUX7436F is designed with a special switch architecture to produce ultra-flat on-resistance (R_{ON}) across most of the switch input operation region. The flat R_{ON} response allows the device to be used in precision sensor applications since the R_{ON} is controlled regardless of the signals sampled. The architecture is implemented without a charge pump so no unwanted noise is produced from the device to affect sampling accuracy.

8.3.2 Protection Features

The TMUX7436F offers a number of protection features to enable robust system implementations.

8.3.2.1 Input Voltage Tolerance

The maximum voltage that can be applied to any source input pin is +60 V or –60 V, regardless of supply voltage. This allows the device to handle typical voltage fault condition in industrial applications. Caution: the device is rated to handle a maximum stress of 85 V across different pins, such as the following:

1. **Between source pins and supply rails: 85 V**

   For example, if the device is powered by V_{DD} supply of 25 V, then the maximum negative signal level on any source pin is –60 V to maintain the 60 V maximum rating on any source pin. If the device is powered by V_{DD} supply of 40 V, then the maximum negative signal level on any source pin is reduced to –45 V to maintain the 85 V maximum rating across the source pin and the supply.
2. **Between source pins and the drain pin: 85 V**

   For example, if channel S1A is ON and the voltage on S1A pin is 40 V, then the drain voltage D1 is also 40 V. In this case, the maximum negative voltage allowed on S1B is –45 V to maintain the 85 V maximum rating across the source pin and the drain pin.

8.3.2.2 Powered-Off Protection

When the supplies of TMUX7436F are removed (V_{DD}/ V_{SS} = 0 V or floating), the source (Sx) pins of the device remain in high impedance (Hi-Z) state, and the source (Sx) and drain (Dx) pins of the device remain within the leakage performance mentioned in the *Electrical Characteristics*. Powered-off protection minimizes system complexity by removing the need to control power supply sequencing of the system. The feature prevents errant voltages on the input source pins from reaching the rest of the system and maintains isolation when the system is powering up. Without powered-off protection, signals on the input source pins can back-power the supply rails through internal ESD diodes and cause potential damage to the system. For more information on powered-off protection, refer to the *Eliminate Power Sequencing with Powered-Off Protection Signal Switches* application brief.

A GND reference must always be present to ensure proper operation. Source and drain voltage levels of up to ±60 V are blocked in the powered-off condition.

8.3.2.3 Fail-Safe Logic

Fail-safe logic circuitry allows voltages on the logic control pins to be applied before the supply pins, protecting the device from potential damage. The switch is specified to be in the OFF state, regardless of the state of the logic signals. The logic inputs are protected against positive faults of up to +44 V in powered-off condition, but do not offer protection against negative overvoltage condition.

Fail-safe logic also allows the TMUX7436F device to interface with a voltage greater than V_{DD} during normal operation to add maximum flexibility in system design. For example, with a V_{DD} of = 15 V, the logic control pins could be connected to +24 V for a logic high signal which allows different types of signals, such as analog feedback voltages, to be used when controlling the logic inputs. Regardless of the supply voltage, the logic inputs can be interfaced as high as 44 V.

8.3.2.4 Overvoltage Protection and Detection

The TMUX7436F detects overvoltage inputs by comparing the voltage on a source pin (Sx) with the supplies (V_{DD} and V_{SS}). A signal is considered overvoltage if it exceeds the supply voltages by the threshold voltage (V_T).

The switch automatically turns OFF regardless of the logic controls when an overvoltage is detected. The source pin becomes high impedance and ensures only small leakage current flows through the switch. The drain pin (Dx) behavior can be adjusted by controlling the drain response (DR) pin in the following ways:

1. **DR pin floating or driven above V_{IH}:**

   If the DR pin is driven above VIH level of the pin, then the drain pin becomes high impedance (Hi-Z) upon overvoltage fault.
2. **DR driven below V_{IL}:**

   If the DR pin is driven below VIL level of the pin, and the channel expeirencing the overvoltage fault condition is currently being selected by the logic controls (EN, SELx), then the drain pin (Dx) is pulled to the supply that was exceeded through a 40 kΩ resistor. For example, if the source voltage exceeds V_{DD}, then the drain output is pulled to V_{DD}. If the source voltage exceeds V_{SS}, then the drain output is pulled to V_{SS}. The pull-up/pull-down impedance is approximately 40 kΩ, and as a result, the drain current is limited during a shorted load (to GND) condition.

Figure 8-1 shows a detailed view of the how the DR pin, SELx pin, and EN pin controls the output state of the drain pin under a fault scenario.

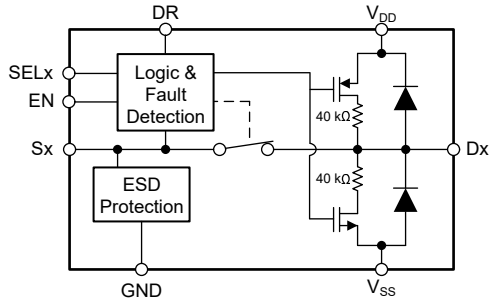


Figure 8-1. Detailed Functional Diagram

8.3.2.5 Adjacent Channel Operation During Fault

When the logic pins are set to a channel under a fault, the overvoltage detection will trigger, the switch will open, and the drain pin will operate as described in Section 8.3.2.4. During such an event, all other channels not under a fault can continue to operate as normal. For example, if S1A voltage exceeds V_{DD}, and the logic pins are set to S1A, and the DR pin is set to logic low, then the drain output is pulled to V_{DD}. Afterwards if the logic pins are changed to set S1B, which is not in overvoltage or undervoltage, then the drain will disconnect from the pullup to V_{DD} and the S1B switch will be enabled and connected to the drain, operating as normal, although there is still an overvoltage condition present on S1A. If the logic pins are switched back to S1A, then the S1B switch will be disabled, the drain pin will be pulled up to V_{DD} again, and the switch from S1A to drain will be disabled until the overvoltage fault is removed.

8.3.2.6 ESD Protection

All pins on the TMUX7436F support HBM ESD protection level up to ±6 kV, which helps prevent the device from being damaged by ESD events during the manufacturing process.

The drain pins (Dx) have internal ESD protection diodes to the supplies V_{DD} and V_{SS}; therefore the voltage at the drain pins must not exceed the supply voltages to prevent excessive diode current. The source pins have specialized ESD protection that allows the signal voltage to reach ±60 V regardless of supply voltage level. Exceeding ±60 V on any source input may damage the ESD protection circuitry on the device and cause the device to malfunction if the damage is excessive.

8.3.2.7 Latch-Up Immunity

Latch-up is a condition where a low impedance path is created between a supply pin and ground. This condition is caused by a trigger (current injection or overvoltage), but once activated, the low impedance path remains even after the trigger is no longer present. This low impedance path may cause system upset or catastrophic damage due to excessive current levels. The latch-up condition typically requires a power cycle to eliminate the low impedance path.

The TMUX7436F device is constructed on silicon on insulator (SOI) based process where an oxide layer is added between the PMOS and NMOS transistor of each CMOS switch to prevent parasitic structures from forming. The oxide layer is also known as an insulating trench and prevents triggering of latch up events due to overvoltage or current injections. The latch-up immunity feature allows the TMUX7436F to be used in harsh environments. For more information on latch-up immunity, refer to *Using Latch Up Immune Multiplexers to Help Improve System Reliability*.

8.3.2.8 EMC Protection

The TMUX7436F is not intended for standalone electromagnetic compatibility (EMC) protection in industrial applications. There are three common high voltage transient specifications that govern industrial high voltage transient specification: IEC61000-4-2 (ESD), IEC61000-4-4 (EFT), and IEC61000-4-5 (surge immunity). A transient voltage suppressor (TVS), along with some low-value series current limiting resistor, are required to prevent source input voltages from going above the rated ±60 V limits.

When selecting a TVS protection device, it is critical to ensure that the maximum working voltage is greater than both the normal operating range of the input source pins to be protected and any known system common-mode overvoltage that may be present due to miswiring, loss of power, or short circuit. Figure 8-2 shows an example of the proper design window when selecting a TVS device.

Region 1 denotes normal operation region of TMUX7436F, where the input source voltages stay below the supplies V_{DD} and V_{SS}. Region 2 represents the range of possible persistent DC (or long duration AC overvoltage fault) presented on the source input pins. Region 3 represents the margin between any known DC overvoltage level and the absolute maximum rating of the TMUX7436F. The TVS breakdown voltage must be selected to be less than the absolute maximum rating of the TMUX7436F, but greater than any known possible persistent DC or long duration AC overvoltage fault to avoid triggering the TVS inadvertently. Region 4 represents the margin system designers must impose when selecting the TVS protection device to prevent accidental triggering of ESD cells of the TMUX7436F device.

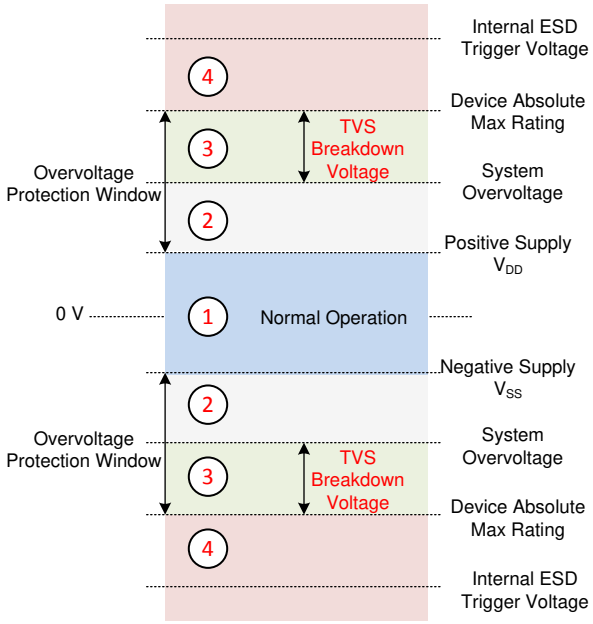


Figure 8-2. System Operation Regions and Proper Region of Selecting a TVS Protection Device

8.3.3 Overvoltage Fault Flags

The voltages on the source input pins of the TMUX7436F are continuously monitored, and the status of whether an overvoltage condition occurs is indicated by an active low general fault flag (FF). The voltage on the FF pin indicates if any of the source input pins are experiencing an overvoltage condition. If any source pin voltage exceeds the fault supply voltages by a V_T, then the FF output is pulled-down to below V_{OL}.

The specific fault (SF) output pins, on the other hand, can be used to decode which inputs are experiencing an overvoltage condition. As provided in the Table 8-1, the SF pin is pulled-down to below V_{OL} when an overvoltage condition is detected on a specific source input pin, depending on the state of the SEL1, SEL2, and EN logic pins.

Both the FF pin and the SF pin are an open-drain output and an external pull-up resistor of 1 kΩ is recommended. The pull-up voltage can be in the range of 1.8 V to 5.5 V, depending on the controller voltage the device interfaces with.

8.3.4 Bidirectional Operation

The TMUX7436F conducts equally well from source (Sx) to drain (Dx) or from drain (Dx) to source (Sx). However, it is noted that the overvoltage protection is implemented only on the source (Sx) side. The voltage on the drain is only allowed to swing between V_{DD} and V_{SS} and no overvotlage protection is available on the drain side.

The flatest on-resistance region extends from V_{SS} to roughly 3 V below V_{DD}. Once the signal is within 3 V of V_{DD} the on-resistance will expoentially increase and may impact desired signal transmission.

8.3.5 1.8 V Logic Compatible Inputs

The TMUX7436F device has 1.8 V logic compatible control for all logic control inputs. 1.8 V logic level inputs allows the TMUX7436F to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and BOM cost. For more information on 1.8 V logic implementations, refer to *Simplifying Design with 1.8 V logic Muxes and Switches*.

8.3.6 Integrated Pull-Down Resistor on Logic Pins

The TMUX7436F has internal weak pull-down resistors to GND to ensure the logic pins are not left floating. The value of this pull-down resistor is approximately 4 MΩ, but is clamped to about 1 µA at higher voltages. This feature integrates up to four external components and reduces system size and cost.

8.4 Device Functional Modes

The TMUX7436F offers two modes of operation (normal mode and fault mode) depending on whether any of the input pins experience an overvoltage condition.

8.4.1 Normal Mode

In Normal mode operation, signals of up to V_{DD} and V_{SS} can be passed through the switch from source (Sx) to drain (Dx) or from drain (Dx) to source (Sx). As provided in Table 8-1, the select pins (SELx) and enable pin (EN) determines which switch path to turn on. The following conditions must be satisfied for the switch to stay in the ON condition:

- The difference between the supples (V_{DD} – V_{SS}) must be greater than or equal to 8 V, with a minimum V_{DD} of 5 V.
- The input signals on the source (Sx) or the drain (Dx) must be be between V_{DD}+ V_T and V_{SS} – V_T.
- The logic control (SELx and EN) must have selected the switch.

8.4.2 Fault Mode

The TMUX7436F enters into Fault mode when any of the input signals on the source (Sx) pins exceed V_{DD} or V_{SS} by a threshold voltage V_T. Under the overvoltage condition, the switch input experiencing the fault automatically turns off regardless of the logic status, and the source pin becomes high impedance with negligible amount of leakage current flowing through the switch. For more information about how the drain pain (Dx) behavior under the Fault mode can be programmed, see Section 8.3.2.4.

In the Fault mode, the general fault flag (FF) is asserted low. Table 8-1 provides how the specific flag (SF) is asserted low depending on the status of the logic control pins SELx and EN.

The overvoltage protection is provided only for the source (Sx) input pins. The drain (Dx) pin, if used as signal input, must stay in between V_{DD} and V_{SS} at all times since no overvoltage protection is implemented on the drain pin.

8.4.3 Truth Tables

Table 8-1 and Table 8-2 provides the truth tables for the TMUX7436F under normal and fault conditions.

Table 8-1. TMUX7436F Truth Table

EN	SEL2	SEL1	Normal Condition	Fault Condition			
				State of Specific Flag (SF) when fault occurs on			
			On Switch	S1A	S1B	S2A	S2B
0	0	0	None	0	1	1	1
0	0	1	None	1	0	1	1
0	1	0	None	1	1	1	0
0	1	1	None	1	1	0	1
1	0	0	S1B, S2B	0	1	1	1
1	0	1	S1A, S2B	1	0	1	1
1	1	0	S1B, S2A	1	1	1	0
1	1	1	S1A, S2A	1	1	0	1

Take note, more than one source pin can be in fault at a given time. As Table 8-1 provides, the SF pin will assert low even when multiple source pins are under fault.

Table 8-2. TMUX7436F DR Truth Table

DR PIN STATE	Dx State During Fault Condition
0	Pulled up to V_{DD} or V_{SS}
1	Open (HI-Z)

If unused, then SELx pins must be tied to GND to ensure the device does not consume additional current (for more information, refer to *Implications of Slow or Floating CMOS Inputs*. Unused signal path inputs (Sx or Dx) should be connected to GND.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TMUX7436F is a part of the fault protected switches and multiplexers family of devices. The abilty to protect downstream components from overvoltage events up to ±60 V and latch-up immunity features makes these switches and multiplexers suitable for harsh environments.

9.2 Typical Application

The need to monitor remote sensors is common among factory automation control systems. For example, an analog input module or mixed module (AI, AO, DI, and DO) of a programmable logic controller (PLC) will interface to a field transmitter to monitor various process sensors at remote locations around the factory. A switch or multiplexer is often used to connect multiple inputs from the system and reduce the number of downstream channels.

There are a number of fault cases that may occur that can be damaging to many of the integrated circuits. Such fault conditions may include, but are not limited to, human error from wiring the connections incorrectly, component failure, wire shorts, electromagnetic interference (EMI), transient distrubances, and more.

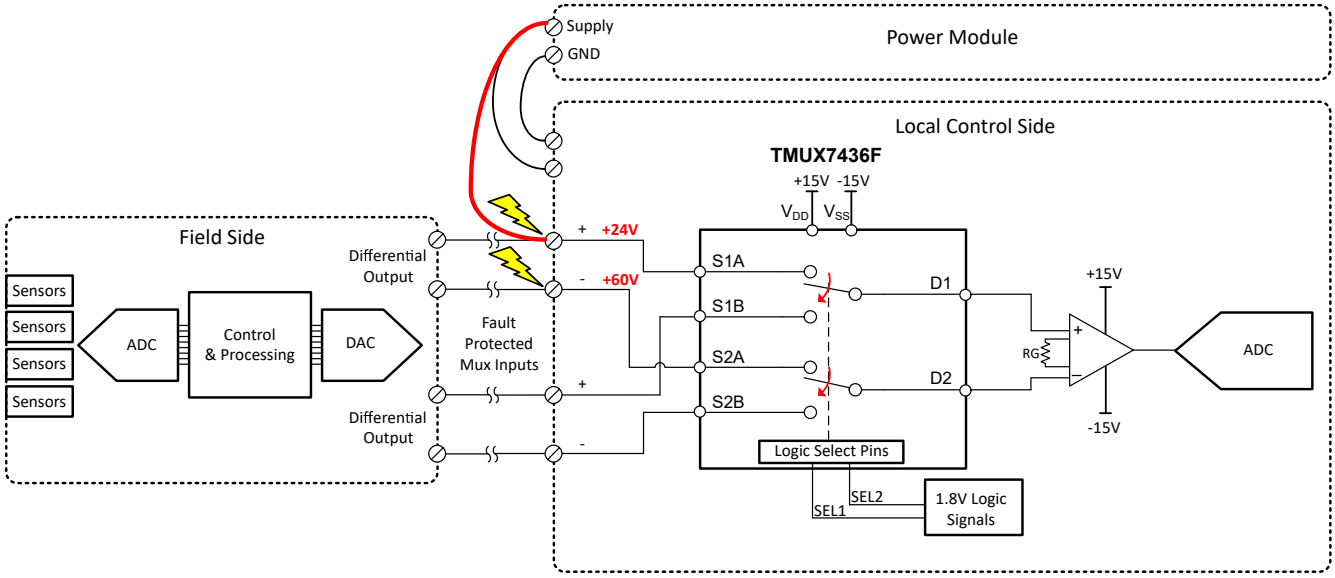


Figure 9-1. Typical Application

9.2.1 Design Requirements

Table 9-1. Design Parameters

PARAMETER	VALUE
Positive supply (V_{DD}) mux	+15 V
Negative supply (V_{SS}) mux	−15 V
Power board supply voltage	24 V
Input or output signal range non-faulted	−15 V to 15 V
Overvoltage protection levels	−60 V to 60 V
Control logic thresholds	1.8 V compatible, up to 44 V
Temperature range	−40°C to +125°C

9.2.2 Detailed Design Procedure

The normal operation of the application is to take multiple differential inputs and use a 2:1 multiplexer to pass the signal to the downstream instrumentation amplifier. A fault protected switch can add extra robustness to the sytem against fault conditions while also reducing the number of components required to interface with the systems physical input channels.

The Figure 9-1 shows the case where a human wired the condition incorrectly and one of the input connectors shorted to the power board supply voltage. If the board supply voltage is higher than the power supply of the multiplexer, then the TMUX7436F device will disconnect the source input from passing the signal to protect the downstream components. The drain pin of the channels can either be pulled up to the supply voltage (V_{DD} and V_{SS}) through a 40 kΩ resistor or be left floating depending on the state of the DR pin. This can be configured to match the system requirements on how to handle a fault condition.

9.2.3 Application Curves

The previous example shows how the fault protection of the TMUX7436F is utilized to protect downstream components from damage due to wiring the connections incorrectly from the power module. Figure 9-2 shows an example of positive overvoltage fault response with a fast fault ramp rate of 40 V/µs. Figure 9-3 shows the extremely flat on-resistance across source voltage while operating within a common signal range of ±10 V. These features make the TMUX7436F an ideal solution for factory automation applications that can face various fault conditions but also require excellent linearity and low distortion.

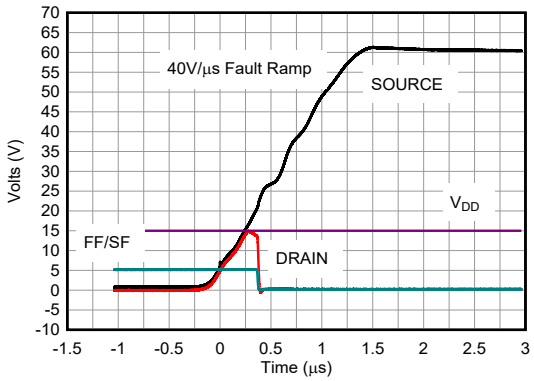


Figure 9-2. Positive Overvoltage Response

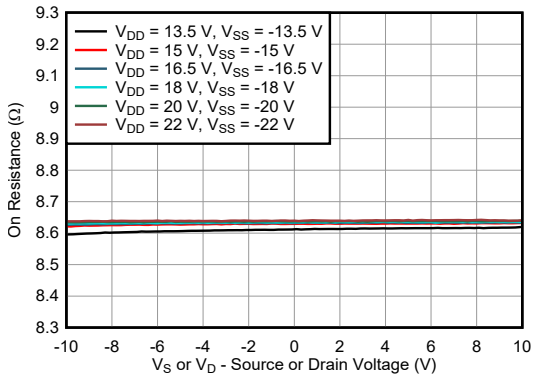


Figure 9-3. R_{ON} Flatness in Non-Fault Region

10 Power Supply Recommendations

The TMUX7436F operates across a wide supply range of ±5 V to ±22 V (8 V to 44 V in single-supply mode). It also performs well with asymmetrical supplies such as V_{DD} = 12 V and V_{SS} = –5 V. Use a supply decoupling capacitor ranging from 1 µF to 10 µF at the V_{DD} and V_{SS} pins to ground for improved supply noise immunity. Always ensure the ground (GND) connection is established before supplies are ramped.

11 Layout

11.1 Layout Guidelines

Figure 11-1 and Figure 11-2 shows an example of a PCB layout with the TMUX7436F. The following are some key considerations:

- Decouple the V_{DD} and V_{SS} pins with a 1-µF capacitor, placed as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the V_{DD} and V_{SS} supplies.
- Multiple decoupling capacitors can be used if their is a lot of noise in the system. For example, a 0.1-µF and 1-µF can be placed on the supply pins. If multiple capacitors are used, placing the lowest value capacitor closest to the supply pin is recommended.
- Keep the input lines as short as possible.
- Use a solid ground plane to help distribute heat and reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

11.2 Layout Example

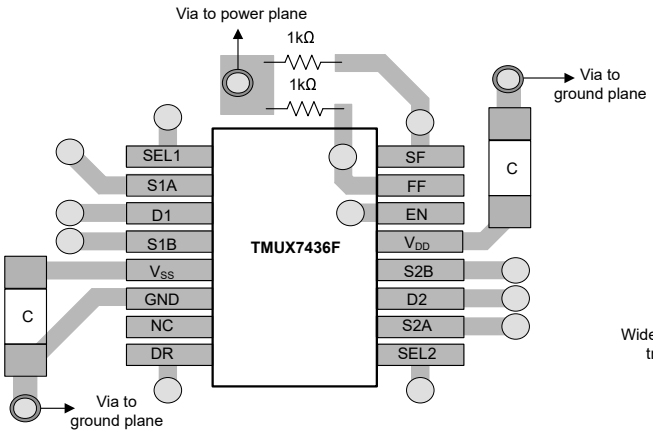


Figure 11-1. TSSOP Layout Example

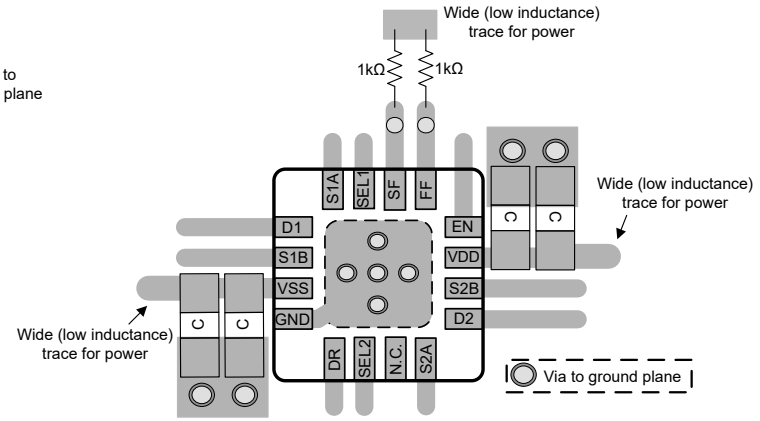


Figure 11-2. WQFN Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application note
- Texas Instruments, *Improving Analog Input Modules Reliability Using Fault Protected Multiplexers* application report
- Texas Instruments, *Multiplexers and Signal Switches Glossary* application report
- Texas Instruments, *Protection Against Overvoltage Events, Miswiring, and Common Mode Voltages* application report
- Texas Instruments, *Using Latch-Up Immune Multiplexers to Help Improve System Reliability* application report
- Texas Instruments, *Using Latch Up Immune Multiplexers to Help Improve System Reliability*

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

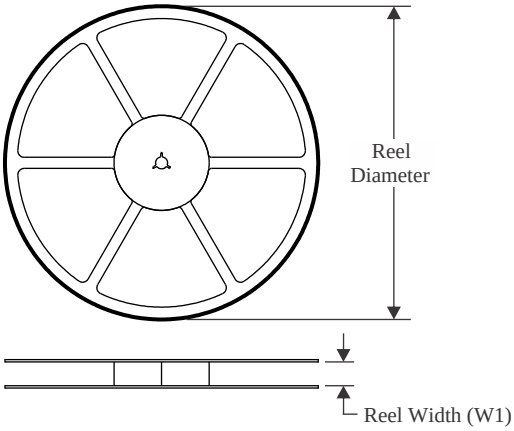
TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

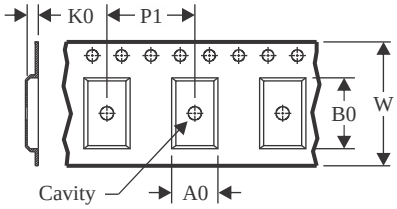
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

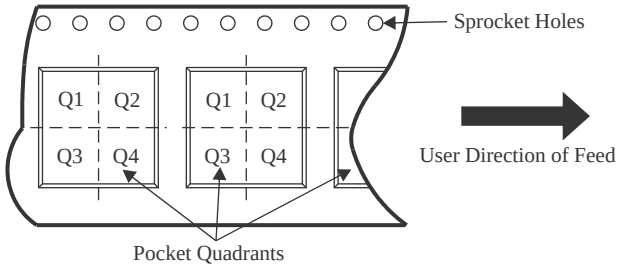


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

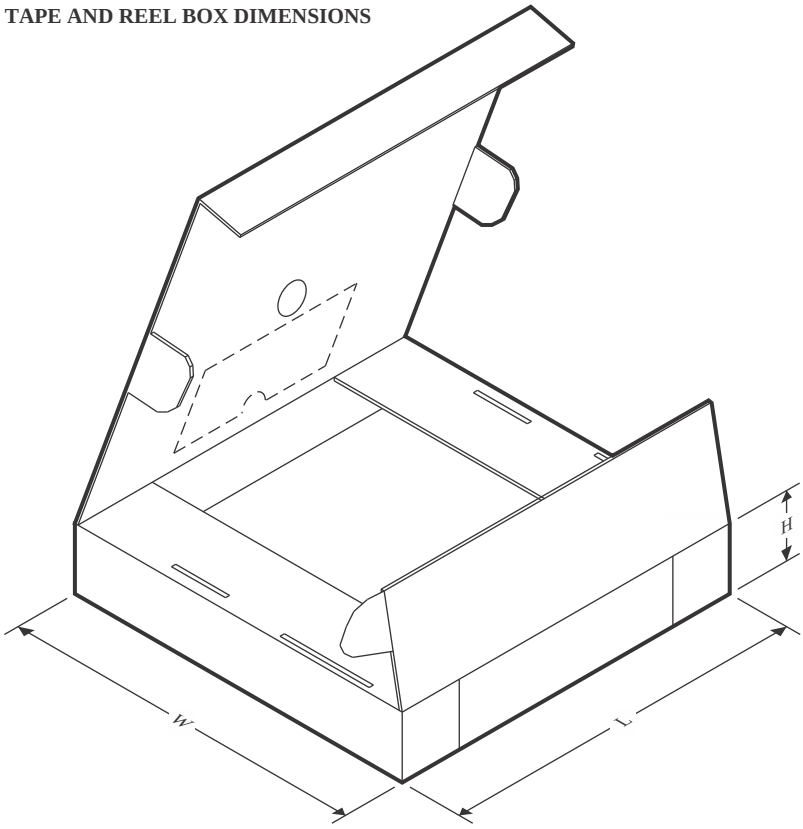
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUX7436FPWR	TSSOP	PW	16	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

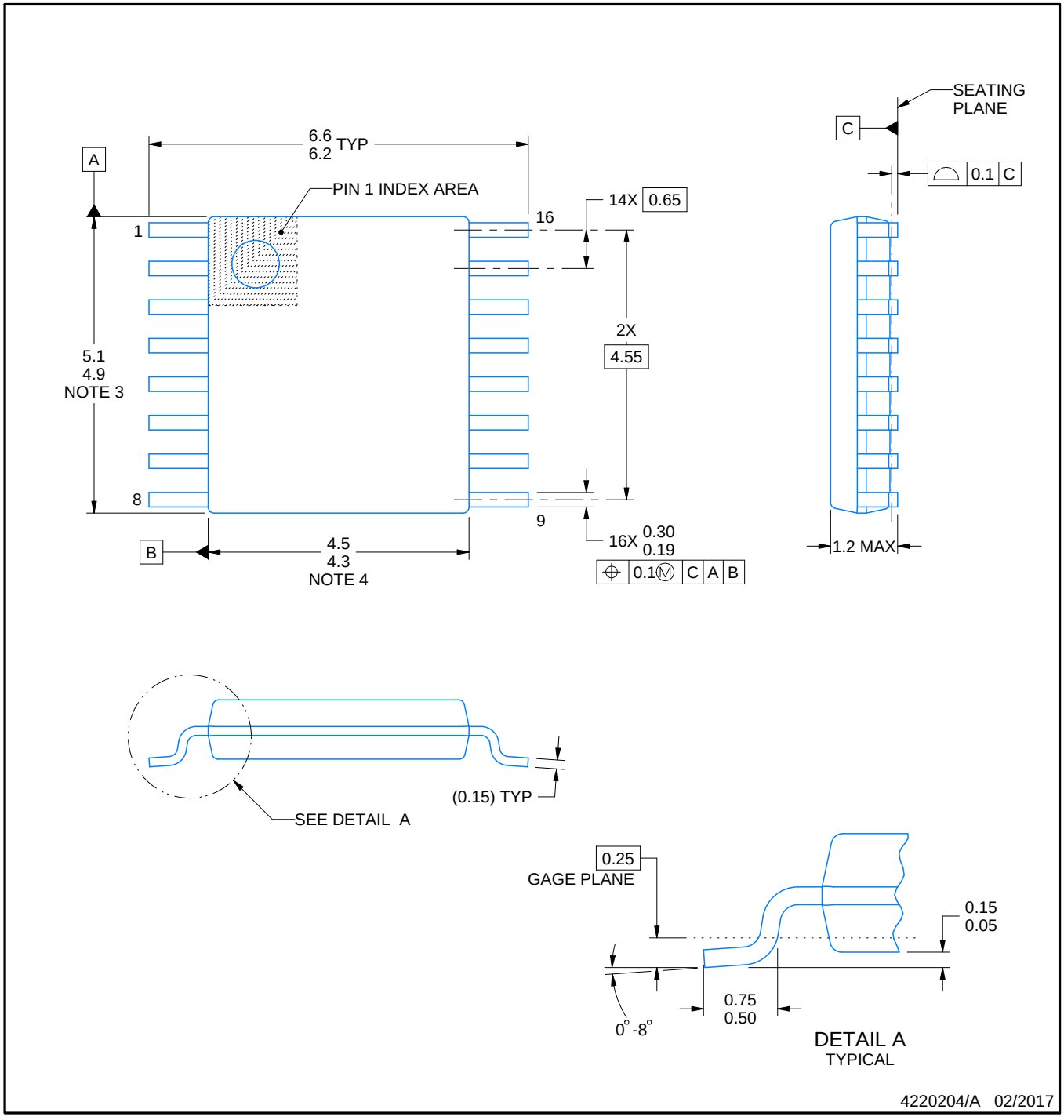
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUX7436FPWR	TSSOP	PW	16	3000	356.0	356.0	35.0

PACKAGE OUTLINE

PW0016A

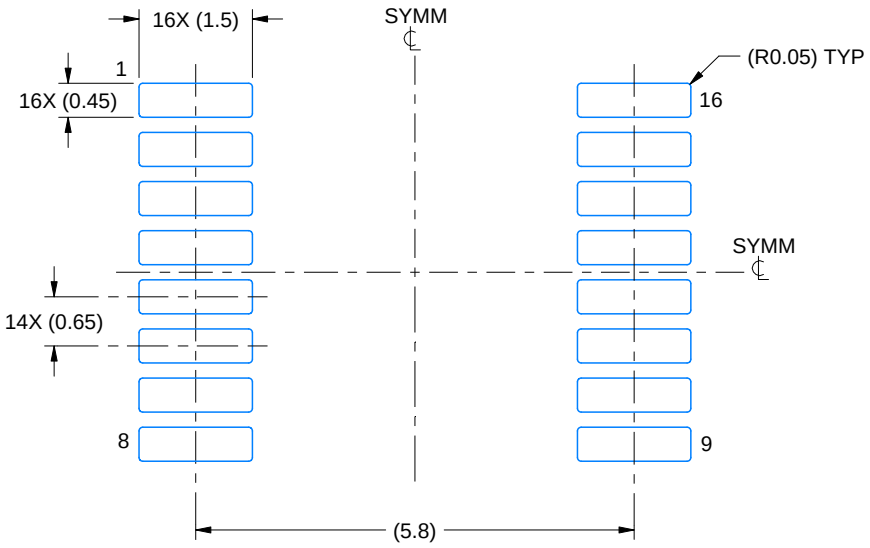
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

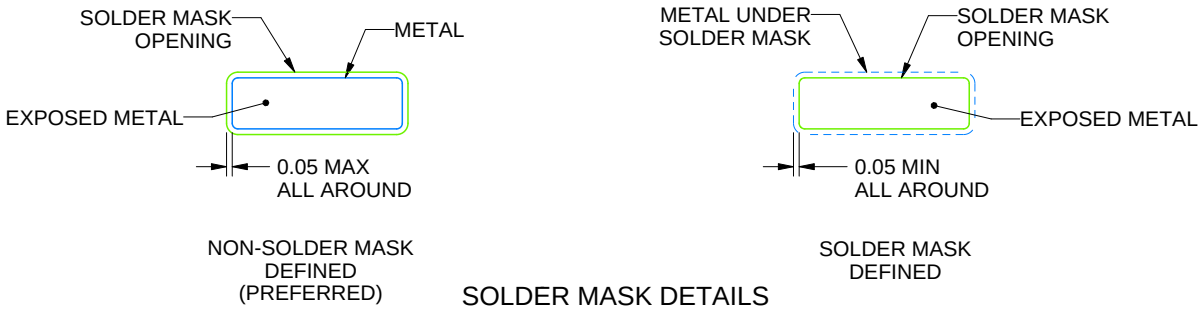


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

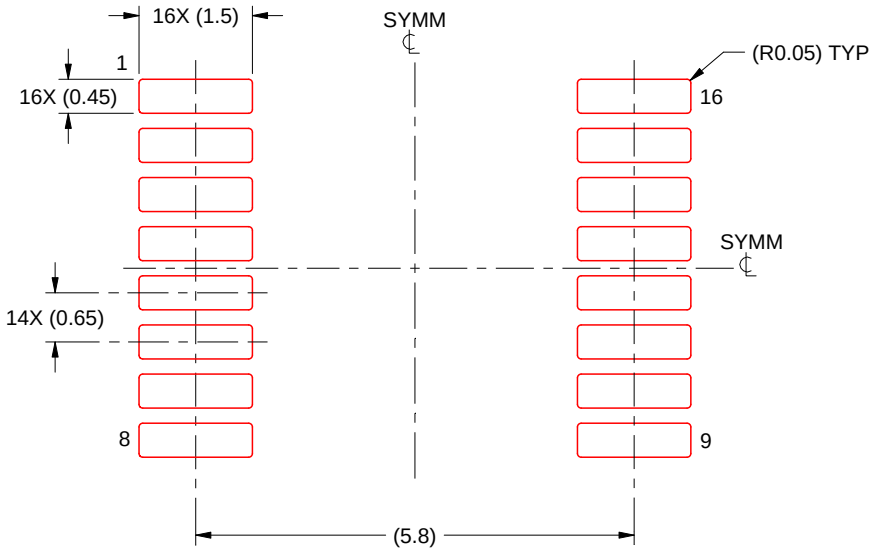


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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