

# SN74AHC74Q-Q1 Automotive Dual Positive-Edge-Triggered D-Type Flip-Flops With Clear and Preset

## 1 Features

- AEC-Q100 qualified for automotive applications:
  - Device temperature grade 1: -40°C to +125°C
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C4B
- Available in *wettable flank* QFN package
- Operating range 2-V to 5.5-V  $V_{CC}$
- Latch-up performance exceeds 250 mA per JESD 17

## 2 Applications

- Convert a momentary switch to a toggle switch
- [Hold a signal during controller reset](#)
- Divide a clock signal by two

## 3 Description

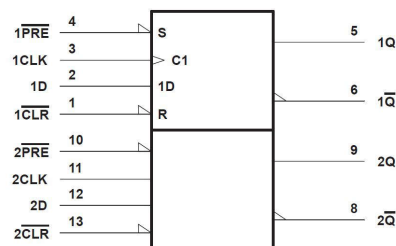
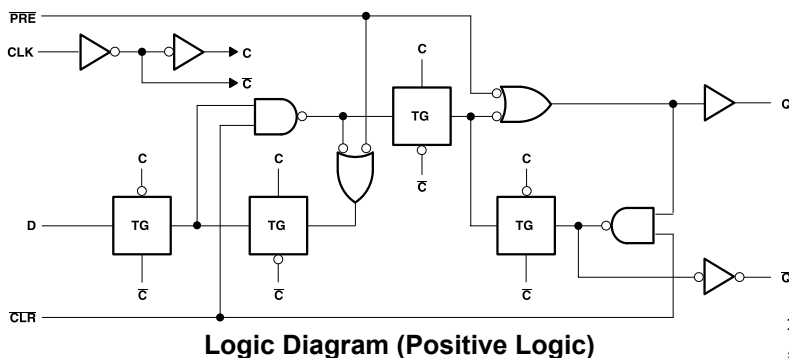
The SN74AHC74Q-Q1 dual positive-edge-triggered device is a D-type flip-flop.

A low level at the preset ( $\overline{PRE}$ ) or clear ( $\overline{CLR}$ ) inputs sets or resets the outputs, regardless of the levels of the other inputs. When  $\overline{PRE}$  and  $\overline{CLR}$  are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

### Package Information

| PART NUMBER   | PACKAGE <sup>(1)</sup> | PACKAGE SIZE <sup>(2)</sup> | BODY SIZE (NOM) <sup>(3)</sup> |
|---------------|------------------------|-----------------------------|--------------------------------|
| SN74AHC74Q-Q1 | BQA (WQFN, 14)         | 3 mm × 2.5 mm               | 3 mm × 2.5 mm                  |
|               | D (SOIC, 14)           | 8.65 mm × 6 mm              | 8.65 mm × 3.9 mm               |
|               | PW (TSSOP, 14)         | 5 mm × 6.4 mm               | 5 mm × 4.4 mm                  |

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.
- (3) The body size (length × width) is a nominal value and does not include pins.



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### Logic Symbol‡



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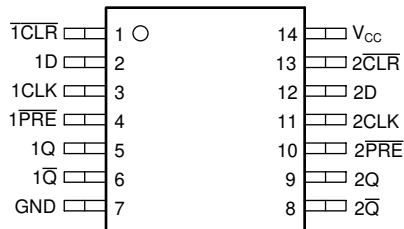
## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

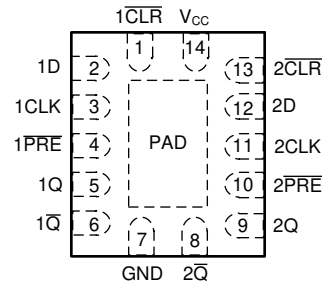
| <b>Changes from Revision B (August 2023) to Revision C (October 2023)</b>   | <b>Page</b> |
|---|-------------|
| • Updated R $\theta$ JA values: PW = 113 to 147.7, all values in °C/W ..... | 5           |

| <b>Changes from Revision A (April 2008) to Revision B (August 2023)</b>                               | <b>Page</b> |
|---|-------------|
| • Updated the numbering format for tables, figures, and cross-references throughout the document..... | 1           |
| • Added the <i>BQA</i> package to the data sheet.....   | 1           |
| • Added the <i>Applications</i> section.....  | 1           |
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## 5 Pin Configuration and Functions



**Figure 5-1. SN74AHC74Q-Q1 D or PW Package, 14-Pin SOIC or TSSOP (Top View)**



**Figure 5-2. SN74AHC74Q-Q1 BQA Package, 14-Pin WQFN (Transparent Top View)**

**Table 5-1. Pin Functions**

| PIN                        |     | TYPE <sup>(1)</sup> | DESCRIPTION  |
|----------------------------|-----|---------------------|--|
| NAME                       | NO. |                     |  |
| 1CLR                       | 1   | I                   | Asynchronous clear for channel 1, active low   |
| 1D                         | 2   | I                   | Data for channel 1   |
| 1CLK                       | 3   | I                   | Clock for channel 1, rising edge triggered   |
| 1PRE                       | 4   | I                   | Asynchronous preset for channel 1, active low  |
| 1Q                         | 5   | O                   | Output for channel 1   |
| 1Q                         | 6   | O                   | Inverted output for channel 1  |
| GND                        | 7   | G                   | Ground   |
| 2Q                         | 8   | O                   | Inverted output for channel 2  |
| 2Q                         | 9   | O                   | Output for channel 2   |
| 2PRE                       | 10  | I                   | Asynchronous preset for channel 2, active low  |
| 2CLK                       | 11  | I                   | Clock for channel 2, rising edge triggered   |
| 2D                         | 12  | I                   | Data for channel 2   |
| 2CLR                       | 13  | I                   | Asynchronous clear for channel 2, active low   |
| V <sub>CC</sub>            | 14  | P                   | Positive supply  |
| Thermal Pad <sup>(2)</sup> |     | —                   | The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply |

(1) I = input, O = output, P = power, G = ground

(2) BQA package only

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                               |   | MIN   | MAX                   | UNIT |
|-------------------------------|---|---|-----------------------|------|
| V <sub>CC</sub>               | Supply voltage range                              | -0.5  | 7                     | V    |
| V <sub>I</sub> <sup>(2)</sup> | Input voltage range                               | -0.5  | 7                     | V    |
| V <sub>O</sub> <sup>(2)</sup> | Output voltage range                              | -0.5  | V <sub>CC</sub> + 0.5 | V    |
| I <sub>IK</sub>               | Input clamp current                               | (V <sub>I</sub> < 0)                                      | -20                   | mA   |
| I <sub>OK</sub>               | Output clamp current                              | (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> ) | ±20                   | mA   |
| I <sub>O</sub>                | Continuous output current                         | (V <sub>O</sub> = 0 to V <sub>CC</sub> )                  | ±25                   | mA   |
|                               | Continuous current through V <sub>CC</sub> or GND |   | ±50                   | mA   |
| T <sub>stg</sub>              | Storage temperature range                         | -65   | 150                   | °C   |

- (1) Operation outside the *Absolute Maximum Rating* may cause permanent device damage. *Absolute Maximum Rating* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Condition*. If used outside the *Recommended Operating Condition* but within the *Absolute Maximum Rating*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 6.2 ESD Ratings

|                    |                         | VALUE  | UNIT  |
|--------------------|-------------------------|--|-------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±2000 |
|                    |                         | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±1000 |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

|                                |                                    | MIN                             | MAX             | UNIT |
|--------------------------------|------------------------------------|---------------------------------|-----------------|------|
| V <sub>CC</sub>                | Supply voltage                     | 2                               | 5.5             | V    |
| V <sub>IH</sub>                | High-level input voltage           | V <sub>CC</sub> = 2 V           | 1.5             | V    |
|                                |                                    | V <sub>CC</sub> = 3 V           | 2.1             |      |
|                                |                                    | V <sub>CC</sub> = 5.5 V         | 3.85            |      |
| V <sub>IL</sub>                | Low-level input voltage            | V <sub>CC</sub> = 2 V           | 0.5             | V    |
|                                |                                    | V <sub>CC</sub> = 3 V           | 0.9             |      |
|                                |                                    | V <sub>CC</sub> = 5.5 V         | 1.65            |      |
| V <sub>I</sub> <sup>(1)</sup>  | Input voltage                      | 0                               | 5.5             | V    |
| V <sub>O</sub>                 | Output voltage                     | 0                               | V <sub>CC</sub> | V    |
| I <sub>OH</sub> <sup>(2)</sup> | High-level output current          | V <sub>CC</sub> = 2 V           | -50             | μA   |
|                                |                                    | V <sub>CC</sub> = 3.3 V ± 0.3 V | -4              | mA   |
|                                |                                    | V <sub>CC</sub> = 5 V ± 0.5 V   | -8              |      |
| I <sub>OL</sub> <sup>(2)</sup> | Low-level output current           | V <sub>CC</sub> = 2 V           | 50              | μA   |
|                                |                                    | V <sub>CC</sub> = 3.3 V ± 0.3 V | 4               | mA   |
|                                |                                    | V <sub>CC</sub> = 5 V ± 0.5 V   | 8               |      |
| Δt/Δv                          | Input transition rise or fall rate | V <sub>CC</sub> = 3.3 V ± 0.3 V | 100             | ns/V |
|                                |                                    | V <sub>CC</sub> = 5 V ± 0.5 V   | 20              |      |
| T <sub>A</sub>                 | Operating free-air temperature     | -40                             | 125             | °C   |

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND for proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

- (2) Recommended current values provided to maintain appropriate output state as per the relevant output voltage specification ( $V_{OL}$  for  $I_{OL}$ ,  $V_{OH}$  for  $I_{OH}$ ). See *Electrical Characteristics* table for details.

## 6.4 Thermal Information — SN74AHC74Q-Q1

| THERMAL METRIC <sup>(1)</sup> |  | BQA (WQFN) | D (SOIC) | PW (TSSOP) | UNIT |
|-------------------------------|--|------------|----------|------------|------|
|                               |  | 14 PINS    | 14 PINS  | 14 PINS    |      |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance | 88.3       | 86       | 147.7      | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS                  | $V_{CC}$     | $T_A = 25^\circ\text{C}$ |     |           | $-40$ to $+125^\circ\text{C}$ |         | UNIT          |
|-----------|----------------------------------|--------------|--------------------------|-----|-----------|-------------------------------|---------|---------------|
|           |                                  |              | MIN                      | TYP | MAX       | MIN                           | MAX     |               |
| $V_{OH}$  | $I_{OH} = -50\ \mu\text{A}$      | 2 V          | 1.9                      | 2   |           | 1.9                           | V       |               |
|           |                                  | 3 V          | 2.9                      | 3   |           | 2.9                           |         |               |
|           |                                  | 4.5 V        | 4.4                      | 4.5 |           | 4.4                           |         |               |
|           | $I_{OH} = -4\ \text{mA}$         | 3 V          | 2.58                     |     |           | 2.48                          |         |               |
|           | $I_{OH} = -8\ \text{mA}$         | 4.5 V        | 3.94                     |     |           | 3.8                           |         |               |
| $V_{OL}$  | $I_{OL} = 50\ \mu\text{A}$       | 2 V          |                          |     | 0.1       |                               | 0.1     | V             |
|           |                                  | 3 V          |                          |     | 0.1       |                               | 0.1     |               |
|           |                                  | 4.5 V        |                          |     | 0.1       |                               | 0.1     |               |
|           | $I_{OL} = 4\ \text{mA}$          | 3 V          |                          |     | 0.36      |                               | 0.5     |               |
|           | $I_{OL} = 8\ \text{mA}$          | 4.5 V        |                          |     | 0.36      |                               | 0.5     |               |
| $I_I$     | $V_I = 5.5\ \text{V}$ or GND     | 0 V to 5.5 V |                          |     | $\pm 0.1$ |                               | $\pm 1$ | $\mu\text{A}$ |
| $I_{CC}$  | $V_I = V_{CC}$ or GND, $I_O = 0$ | 5.5 V        |                          |     | 2         |                               | 20      | $\mu\text{A}$ |
| $C_i$     | $V_I = V_{CC}$ or GND            | 5 V          |                          | 2   | 10        |                               | 10      | pF            |

## 6.6 Timing Requirements — $V_{CC} = 3.3\ \text{V} \pm 0.3\ \text{V}$

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | DESCRIPTION                          | CONDITION   | $T_A = 25^\circ\text{C}$ |     | $-40^\circ\text{C}$ to $125^\circ\text{C}$ |     | UNIT |
|-----------|--------------------------------------|---|--------------------------|-----|--|-----|------|
|           |                                      |   | MIN                      | MAX | MIN  | MAX |      |
| $t_w$     | Pulse duration                       | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ LOW      | 6                        |     | 7  |     | ns   |
|           |                                      | CLK   | 6                        |     | 7  |     | ns   |
| $t_{su}$  | Setup time before CLK $\uparrow$     | Data  | 6                        |     | 7  |     | ns   |
|           |                                      | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ Inactive | 5                        |     | 5  |     | ns   |
| $t_h$     | Hold time, data after CLK $\uparrow$ |   | 0.5                      |     | 0.5  |     | ns   |

## 6.7 Timing Requirements — $V_{CC} = 5\ \text{V} \pm 0.5\ \text{V}$

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | DESCRIPTION                      | CONDITION   | $T_A = 25^\circ\text{C}$ |     | $-40^\circ\text{C}$ to $125^\circ\text{C}$ |     | UNIT |
|-----------|----------------------------------|---|--------------------------|-----|--|-----|------|
|           |                                  |   | MIN                      | MAX | MIN  | MAX |      |
| $t_w$     | Pulse duration                   | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ LOW      | 5                        |     | 5  |     | ns   |
|           |                                  | CLK   | 5                        |     | 5  |     | ns   |
| $t_{su}$  | Setup time before CLK $\uparrow$ | Data  | 5                        |     | 5  |     | ns   |
|           |                                  | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ Inactive | 3                        |     | 3  |     | ns   |

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER      | DESCRIPTION                | CONDITION | T <sub>A</sub> = 25°C |     | -40°C to 125°C |     | UNIT |
|----------------|----------------------------|-----------|-----------------------|-----|----------------|-----|------|
|                |                            |           | MIN                   | MAX | MIN            | MAX |      |
| t <sub>h</sub> | Hold time, data after CLK↑ |           | 0.5                   |     | 0.5            |     | ns   |

## 6.8 Switching Characteristics, V<sub>CC</sub> = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (see Section 7)

| PARAMETER        | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE       | T <sub>A</sub> = 25°C |      |      | -40 to +125 °C |      | UNIT |
|------------------|--------------|-------------|------------------------|-----------------------|------|------|----------------|------|------|
|                  |              |             |                        | MIN                   | TYP  | MAX  | MIN            | MAX  |      |
| f <sub>max</sub> |              |             | C <sub>L</sub> = 15 pF | 80                    | 125  |      | 70             |      | ns   |
|                  |              |             | C <sub>L</sub> = 50 pF | 50                    | 75   |      | 45             |      |      |
| t <sub>PLH</sub> | PRE or CLR   | Q or Q̄     | C <sub>L</sub> = 15 pF |                       | 7.6  | 12.3 | 1              | 14.5 | ns   |
| t <sub>PHL</sub> |              |             |                        |                       | 7.6  | 12.3 | 1              | 14.5 |      |
| t <sub>PLH</sub> | CLK          | Q or Q̄     | C <sub>L</sub> = 15 pF |                       | 6.7  | 11.9 | 1              | 14   | ns   |
| t <sub>PHL</sub> |              |             |                        |                       | 6.7  | 11.9 | 1              | 14   |      |
| t <sub>PLH</sub> | PRE or CLR   | Q or Q̄     | C <sub>L</sub> = 50 pF |                       | 10.1 | 15.8 | 1              | 18   | ns   |
| t <sub>PHL</sub> |              |             |                        |                       | 10.1 | 15.8 | 1              | 18   |      |
| t <sub>PLH</sub> | CLK          | Q or Q̄     | C <sub>L</sub> = 50 pF |                       | 9.2  | 15.4 | 1              | 17.5 | ns   |
| t <sub>PHL</sub> |              |             |                        |                       | 9.2  | 15.4 | 1              | 17.5 |      |

## 6.9 Switching Characteristics, V<sub>CC</sub> = 5 V ± 0.5 V

over recommended operating free-air temperature range, (see Section 7)

| PARAMETER        | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE       | T <sub>A</sub> = 25°C |     |     | -40 to +125 °C |      | UNIT |
|------------------|--------------|-------------|------------------------|-----------------------|-----|-----|----------------|------|------|
|                  |              |             |                        | MIN                   | TYP | MAX | MIN            | MAX  |      |
| f <sub>max</sub> |              |             | C <sub>L</sub> = 15 pF | 130                   | 170 |     | 110            |      | ns   |
|                  |              |             | C <sub>L</sub> = 50 pF | 90                    | 115 |     | 75             |      |      |
| t <sub>PLH</sub> | PRE or CLR   | Q or Q̄     | C <sub>L</sub> = 15 pF |                       | 4.8 | 7.7 | 1              | 9    | ns   |
| t <sub>PHL</sub> |              |             |                        |                       | 4.8 | 7.7 | 1              | 9    |      |
| t <sub>PLH</sub> | CLK          | Q or Q̄     | C <sub>L</sub> = 15 pF |                       | 4.6 | 7.3 | 1              | 8.5  | ns   |
| t <sub>PHL</sub> |              |             |                        |                       | 4.6 | 7.3 | 1              | 8.5  |      |
| t <sub>PLH</sub> | PRE or CLR   | Q or Q̄     | C <sub>L</sub> = 50 pF |                       | 6.3 | 9.7 | 1              | 11   | ns   |
| t <sub>PHL</sub> |              |             |                        |                       | 6.3 | 9.7 | 1              | 11   |      |
| t <sub>PLH</sub> | CLK          | Q or Q̄     | C <sub>L</sub> = 50 pF |                       | 6.1 | 9.3 | 1              | 10.5 | ns   |
| t <sub>PHL</sub> |              |             |                        |                       | 6.1 | 9.3 | 1              | 10.5 |      |

## 6.10 Noise Characteristics

V<sub>CC</sub> = 5 V, C<sub>L</sub> = 50 pF, T<sub>A</sub> = 25°C<sup>(1)</sup>

| PARAMETER          | DESCRIPTION                                   | MIN | TYP | MAX  | UNIT |
|--------------------|---|-----|-----|------|------|
| V <sub>OL(P)</sub> | Quiet output, maximum dynamic V <sub>OL</sub> |     |     | 0.8  | V    |
| V <sub>OL(V)</sub> | Quiet output, minimum dynamic V <sub>OL</sub> |     |     | -0.8 | V    |
| V <sub>OH(V)</sub> | Quiet output, minimum dynamic V <sub>OH</sub> | 4.7 |     |      | V    |
| V <sub>IH(D)</sub> | High-level dynamic input voltage              | 3.5 |     |      | V    |
| V <sub>IL(D)</sub> | Low-level dynamic input voltage               |     |     | 1.5  | V    |

(1) Characteristics are for surface-mount packages only.

### 6.11 Operating Characteristics

$V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

| PARAMETER                              | TEST CONDITIONS             | TYP | UNIT |
|--|-----------------------------|-----|------|
| $C_{pd}$ Power dissipation capacitance | No load, $f = 1\text{ MHz}$ | 32  | pF   |

### 6.12 Typical Characteristics

$T_A = 25^\circ\text{C}$  (unless otherwise noted)

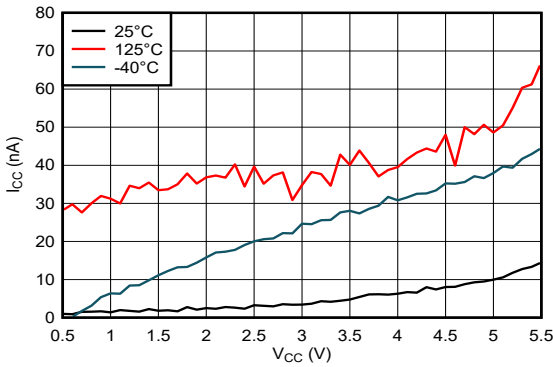


Figure 6-1. Supply Current Across Supply Voltage

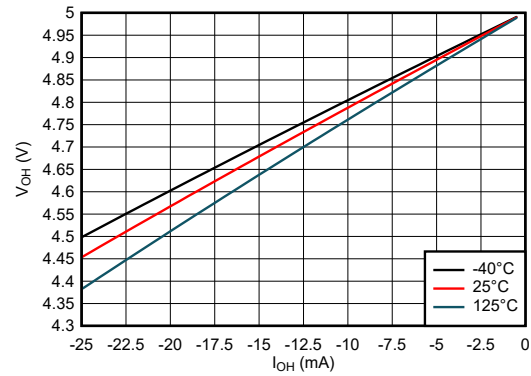


Figure 6-2. Output Voltage vs Current in HIGH State; 5-V Supply

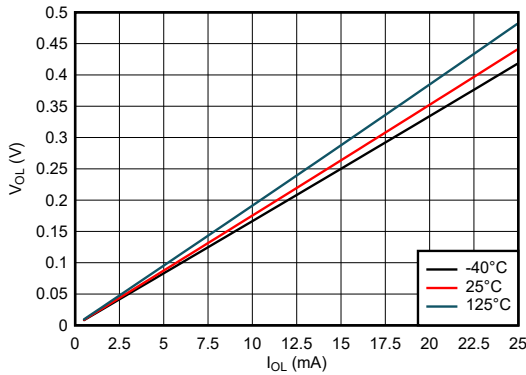


Figure 6-3. Output Voltage vs Current in LOW State; 5-V Supply

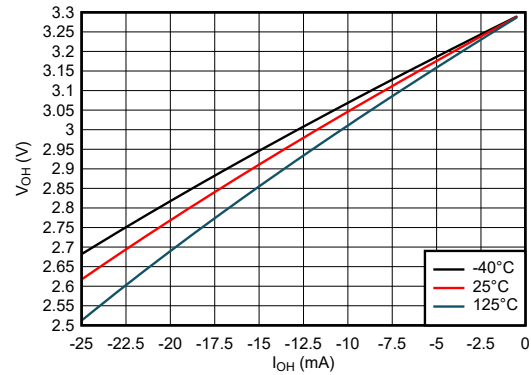


Figure 6-4. Output Voltage vs Current in HIGH State; 3.3-V Supply

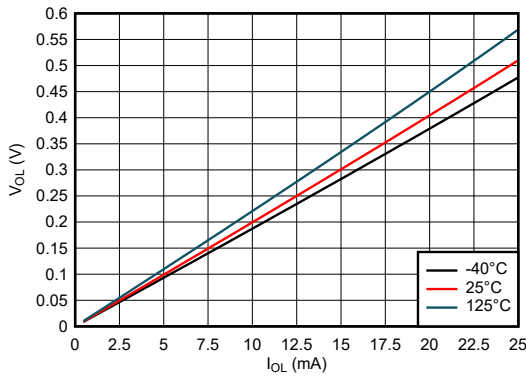


Figure 6-5. Output Voltage vs Current in LOW State; 3.3-V Supply

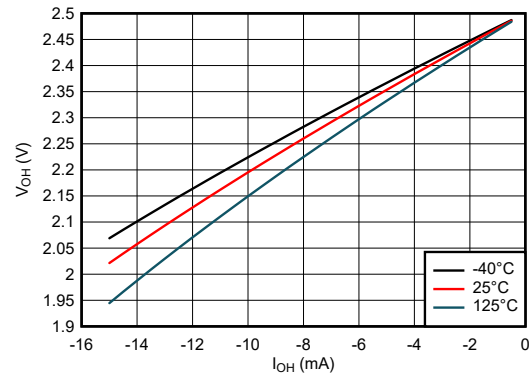


Figure 6-6. Output Voltage vs Current in HIGH State; 2.5-V Supply

## 6.12 Typical Characteristics (continued)

T<sub>A</sub> = 25°C (unless otherwise noted)

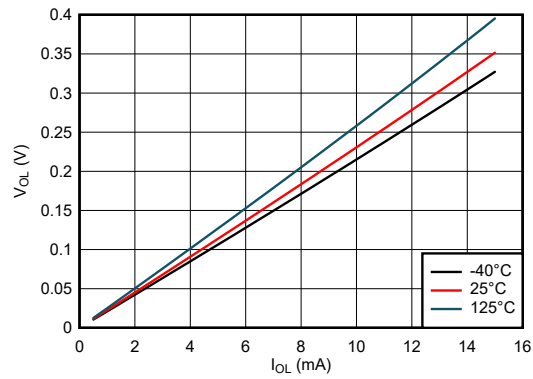
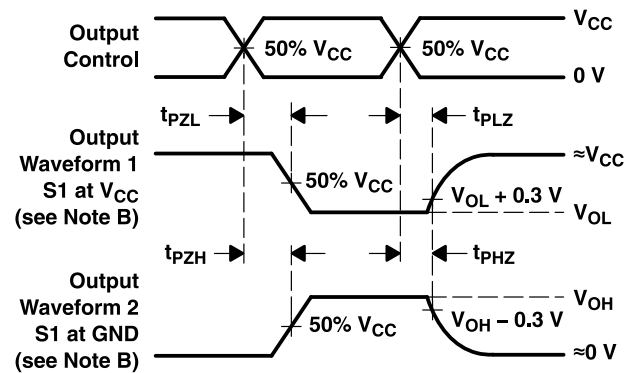
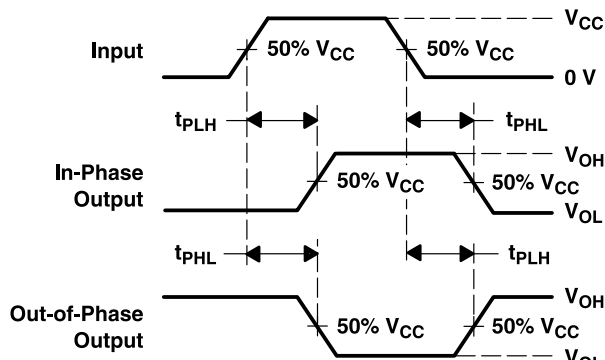
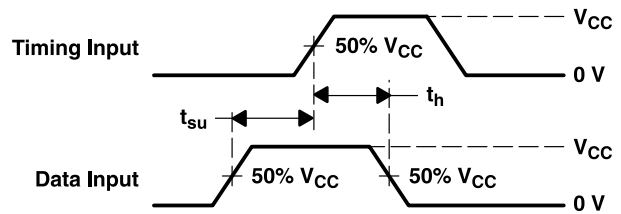
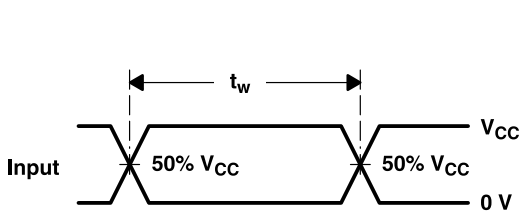
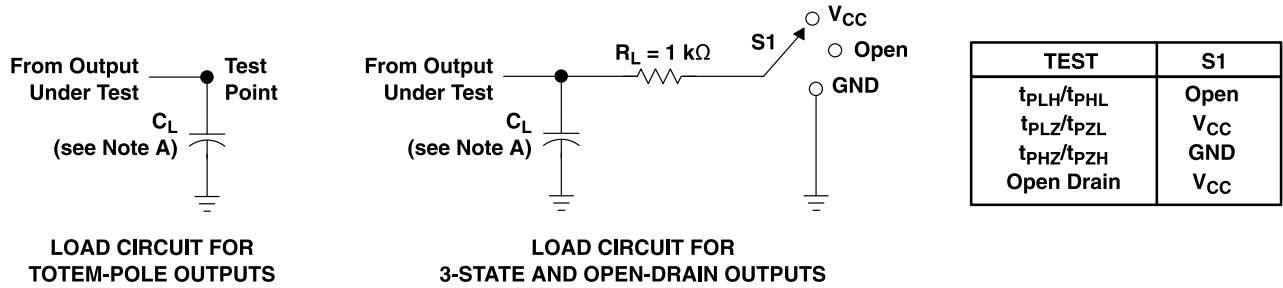


Figure 6-7. Output Voltage vs Current in LOW State; 2.5-V Supply



## 7 Parameter Measurement Information



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 3$  ns,  $t_f \leq 3$  ns.  
 D. The outputs are measured one at a time with one input transition per measurement.  
 E. All parameters and waveforms are not applicable to all devices.

Figure 7-1. Load Circuit And Voltage Waveforms

## 8 Detailed Description

### 8.1 Overview

The SN74AHC74Q-Q1 dual positive-edge-triggered devices are D-type flip-flops.

A low level at the preset ( $\overline{\text{PRE}}$ ) or clear ( $\overline{\text{CLR}}$ ) inputs sets or resets the outputs, regardless of the levels of the other inputs. When  $\overline{\text{PRE}}$  and  $\overline{\text{CLR}}$  are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

### 8.2 Functional Block Diagram

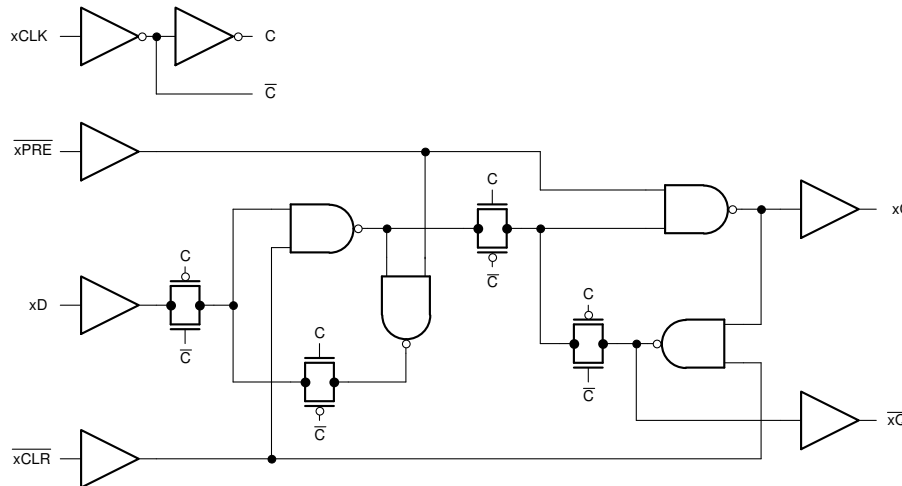


Figure 8-1. Logic Diagram (Positive Logic) for One Channel of SN74AHC74Q-Q1

### 8.3 Feature Description

#### 8.3.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs should be left disconnected.

#### 8.3.2 Latching Logic

This device includes latching logic circuitry. Latching circuits commonly include D-type latches and D-type flip-flops, but include all logic circuits that act as volatile memory.

When the device is powered on, the state of each latch is unknown. There is no default state for each latch at start-up.

The output state of each latching logic circuit only remains stable as long as power is applied to the device within the supply voltage range specified in the *Recommended Operating Conditions* table.

#### 8.3.3 Standard CMOS Inputs

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst

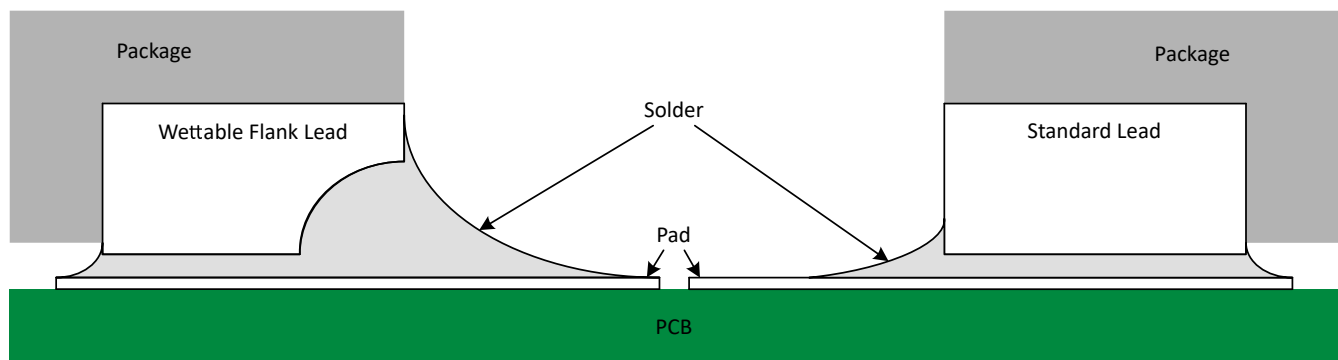
case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law ( $R = V \div I$ ).

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in [Implications of Slow or Floating CMOS Inputs](#).

Do not leave standard CMOS inputs floating at any time during operation. Unused inputs must be terminated at  $V_{CC}$  or GND. If a system will not be actively driving an input at all times, then a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; a 10-k $\Omega$  resistor, however, is recommended and will typically meet all requirements.

### 8.3.4 Wettable Flanks

This device includes wettable flanks for at least one package. See the *Features* section on the front page of the data sheet for which packages include this feature.



**Figure 8-2. Simplified Cutaway View of Wettable-Flank QFN Package and Standard QFN Package After Soldering**

Wettable flanks help improve side wetting after soldering, which makes QFN packages easier to inspect with automatic optical inspection (AOI). As shown in [Figure 8-2](#), a wettable flank can be dimpled or step-cut to provide additional surface area for solder adhesion which assists in reliably creating a side fillet. See the mechanical drawing for additional details.

### 8.3.5 Clamp Diode Structure

As [Figure 8-3](#) shows, the outputs to this device have both positive and negative clamping diodes, and the inputs to this device have negative clamping diodes only.

#### **CAUTION**

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

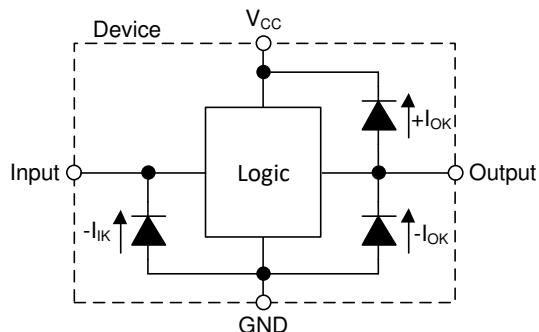


Figure 8-3. Electrical Placement of Clamping Diodes for Each Input and Output

### 8.4 Device Functional Modes

Table 8-1 shows the function table for each input and output.

Table 8-1. Function Table (Each Flip-Flop)

| INPUTS                  |                         |     |   | OUTPUTS          |                         |
|-------------------------|-------------------------|-----|---|------------------|-------------------------|
| $\overline{\text{PRE}}$ | $\overline{\text{CLR}}$ | CLK | D | Q                | $\overline{\text{Q}}$   |
| L                       | H                       | X   | X | H                | L                       |
| H                       | L                       | X   | X | L                | H                       |
| L                       | L                       | X   | X | H <sup>(1)</sup> | H <sup>(1)</sup>        |
| H                       | H                       | ↑   | H | H                | L                       |
| H                       | H                       | ↑   | L | L                | H                       |
| H                       | H                       | L   | X | Q <sub>0</sub>   | $\overline{\text{Q}}_0$ |

- (1) This configuration is unstable; that is, it does not persist when  $\overline{\text{PRE}}$  or  $\overline{\text{CLR}}$  returns to its inactive (high) level.

## 9 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Application Information

Toggle switches are typically large, mechanically complex and relatively expensive. It is desirable to use a momentary switch instead because they are small, mechanically simple and low cost. Some systems require a toggle switch's functionality but are space or cost constrained and must use a momentary switch instead.

If the data input (D) of the D-type flip-flop is tied to the inverted output ( $\overline{Q}$ ), then each clock pulse will cause the value at the output (Q) to toggle. The momentary switch can be debounced and connected through a Schmitt-trigger buffer to the clock input (CLK) to toggle the output.

This application also utilizes a power-on reset circuit so that the output always starts in the LOW state when power is applied.

### 9.2 Typical Application

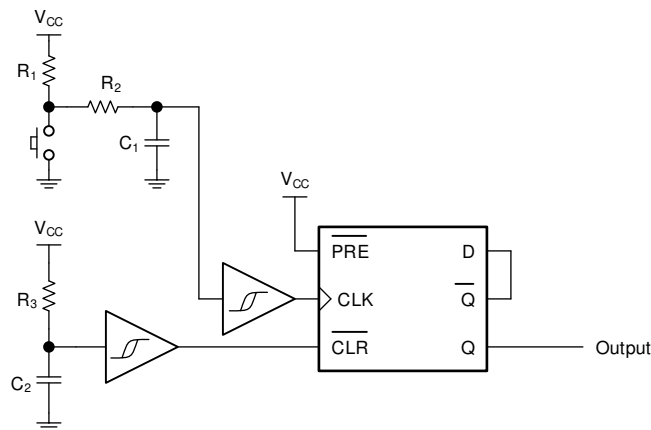


Figure 9-1. Typical Application Schematic

#### 9.2.1 Design Requirements

##### 9.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics - 74*.

The supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74AHC74Q-Q1 plus the maximum supply current,  $I_{CC}$ , listed in the *Electrical Characteristics - 74*. The logic device can only source or sink as much current as it is provided at the supply and ground pins, respectively. Be sure to not exceed the maximum total current through GND or  $V_{CC}$  listed in the *Absolute Maximum Ratings*.

Total power consumption can be calculated using the information provided in [CMOS Power Consumption and  \$C\_{pd}\$  Calculation](#).

Thermal increase can be calculated using the information provided in [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#).

**CAUTION**

The maximum junction temperature,  $T_{J(max)}$  listed in the *Absolute Maximum Ratings*, is an *additional limitation* to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

**9.2.1.2 Input Considerations**

Unused inputs must be terminated to either  $V_{CC}$  or ground. These can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The resistor size is limited by drive current of the controller, leakage current into the SN74AHC74Q-Q1, as specified in the *Electrical Characteristics - 74*, and the desired input transition rate. A 10-k $\Omega$  resistor value is often used due to these factors.

The SN74AHC74Q-Q1 has standard CMOS inputs, so input signal edge rates cannot be slow. Slow input edge rates can cause oscillations and damaging shoot-through current. The recommended rates are defined in the *Recommended Operating Conditions*.

Refer to the *Feature Description* for additional information regarding the inputs for this device.

**9.2.1.3 Output Considerations**

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the  $V_{OH}$  specification in the *Electrical Characteristics - 74*. Similarly, the ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the  $V_{OL}$  specification in the *Electrical Characteristics - 74*.

Unused outputs can be left floating. Do not connect outputs directly to  $V_{CC}$  or ground.

Refer to *Feature Description* for additional information regarding the outputs for this device.

**9.2.1.4 Timing Considerations**

The SN74AHC74Q-Q1 is a clocked device. As such, it requires special timing considerations for normal operation.

Primary timing factors to consider:

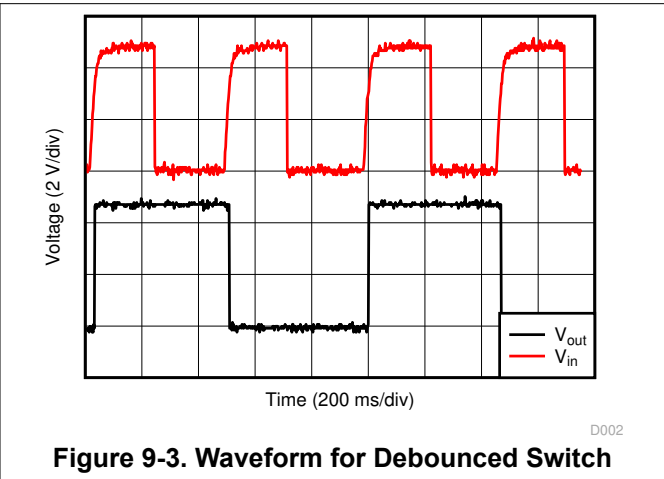
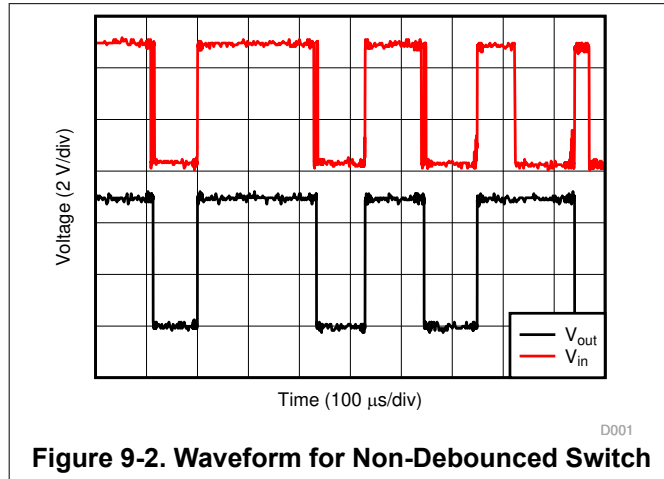
- Maximum clock frequency: the maximum operating clock frequency defined in *Timing Requirements - 74* is the maximum frequency at which the device is designed to function. This value refers specifically to the triggering waveform, measuring from one trigger level to the next.
- Pulse duration: ensure that the triggering event duration is larger than the minimum pulse duration, as defined in the *Timing Requirements - 74*.
- Setup time: ensure that the data has changed at least one setup time prior to the triggering event, as defined in the *Timing Requirements - 74*.
- Hold time: ensure that the data remains in the desired state at least one hold time after the triggering event, as defined in the *Timing Requirements - 74*.

**9.2.2 Detailed Design Procedure**

1. Add a decoupling capacitor from  $V_{CC}$  to GND. The capacitor needs to be placed physically close to the device and electrically close to both the  $V_{CC}$  and GND pins. An example layout is shown in the *Layout Example*.
2. Ensure the capacitive load at the output is  $\leq 70$  pF. This is not a hard limit; however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN74AHC74Q-Q1 to the receiving device.
3. Ensure the resistive load at the output is larger than  $(V_{CC} / I_{O(max)}) \Omega$ , so that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in mega ohms; much larger than the minimum calculated above.

- Thermal issues are rarely a concern for logic gates, however the power consumption and thermal increase can be calculated using the steps provided in the application report, [CMOS Power Consumption and Cpd Calculation](#)

### 9.2.3 Application Curves



## 9.3 Power Supply Recommendations

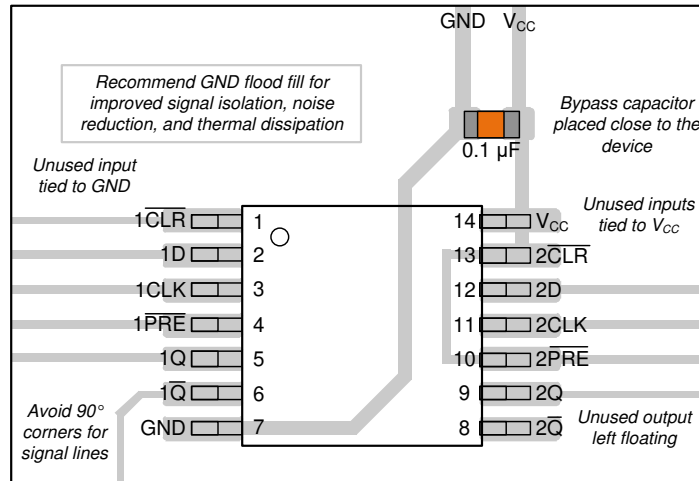
The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a bypass capacitor to prevent power disturbance. A 0.1- $\mu\text{F}$  capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1- $\mu\text{F}$  and 1- $\mu\text{F}$  capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in the *Layout Example*.

## 9.4 Layout

### 9.4.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

### 9.4.2 Layout Example



**Figure 9-4. Example Layout for the SN74AHC74Q-Q1**



## 10 Device and Documentation Support

### 10.1 Documentation Support

#### 10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [CMOS Power Consumption and Cpd Calculation](#)
- Texas Instruments, [Implications of Slow or Floating CMOS Inputs](#)
- Texas Instruments, [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#)

### 10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 10.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 10.4 Trademarks

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All trademarks are the property of their respective owners.

### 10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 10.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable Device  | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|-------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74AHC74QDRG4Q1  | ACTIVE        | SOIC         | D               | 14   | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | AHC74Q                  | <a href="#">Samples</a> |
| SN74AHC74QDRQ1    | ACTIVE        | SOIC         | D               | 14   | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | AHC74Q                  | <a href="#">Samples</a> |
| SN74AHC74QPWRG4Q1 | ACTIVE        | TSSOP        | PW              | 14   | 2000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | HA74Q                   | <a href="#">Samples</a> |
| SN74AHC74QPWRQ1   | ACTIVE        | TSSOP        | PW              | 14   | 2000        | RoHS & Green    | NIPDAU                               | Level-3-260C-168 HR  | -40 to 125   | HA74Q                   | <a href="#">Samples</a> |
| SN74AHC74QWBQARQ1 | ACTIVE        | WQFN         | BQA             | 14   | 3000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | AHC74Q                  | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74AHC74QPWRG4Q1 | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74AHC74QPWRQ1   | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74AHC74QWBQARQ1 | WQFN         | BQA             | 14   | 3000 | 180.0              | 12.4               | 2.8     | 3.3     | 1.1     | 4.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74AHC74QPWRG4Q1 | TSSOP        | PW              | 14   | 2000 | 367.0       | 367.0      | 35.0        |
| SN74AHC74QPWRQ1   | TSSOP        | PW              | 14   | 2000 | 356.0       | 356.0      | 35.0        |
| SN74AHC74QWBQARQ1 | WQFN         | BQA             | 14   | 3000 | 210.0       | 185.0      | 35.0        |

## GENERIC PACKAGE VIEW

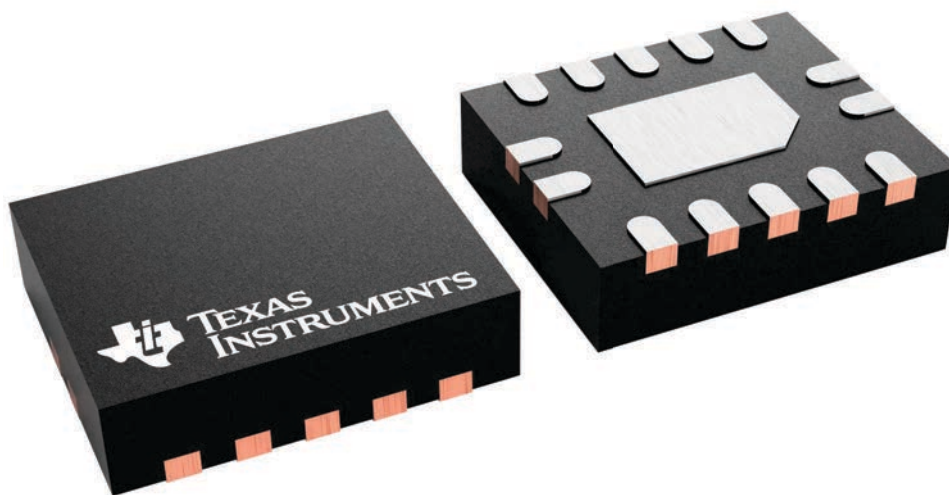
**BQA 14**

**WQFN - 0.8 mm max height**

2.5 x 3, 0.5 mm pitch

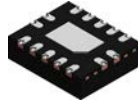
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4227145/A

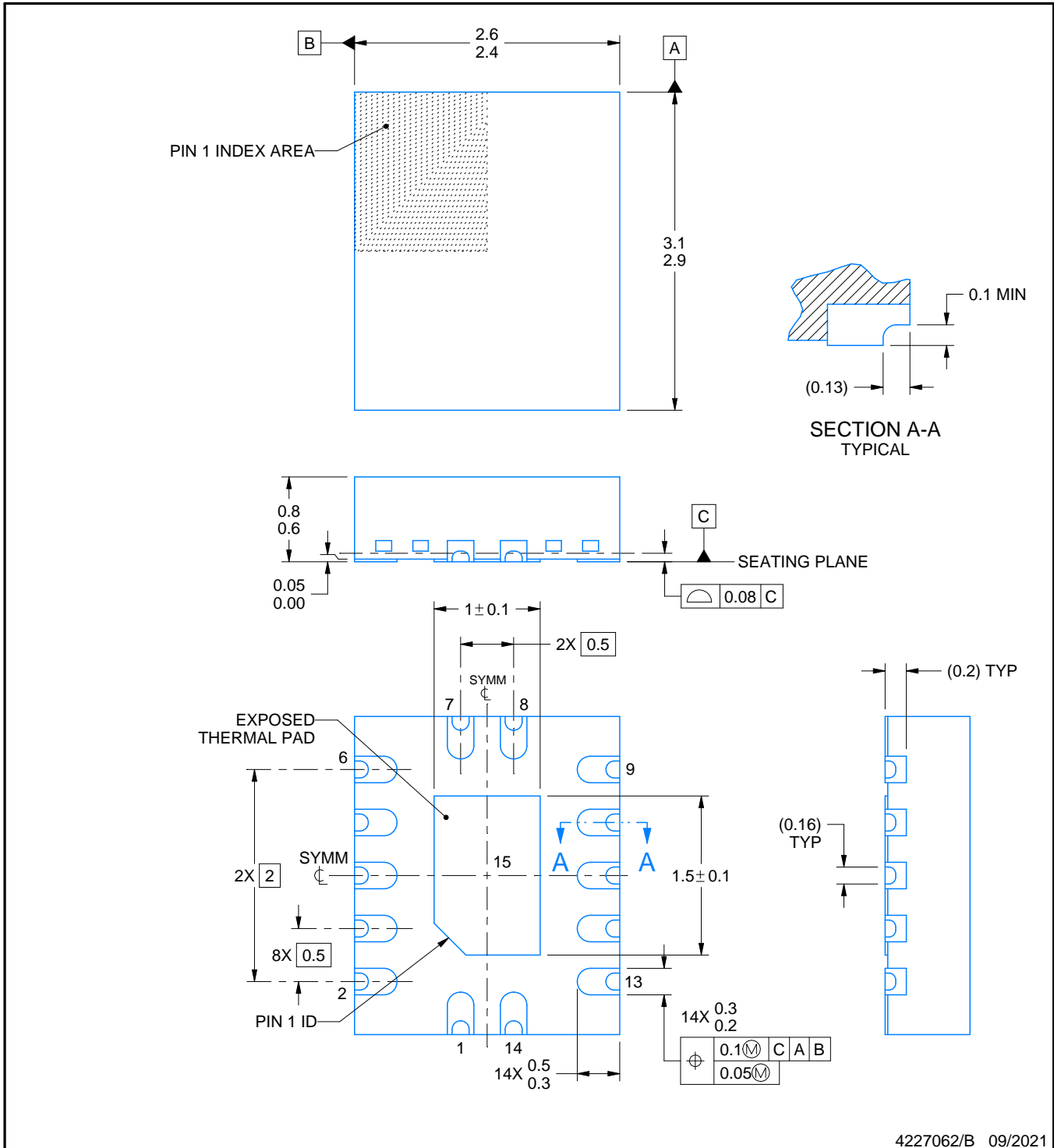
# BQA0014B



## PACKAGE OUTLINE

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4227062/B 09/2021

**NOTES:**

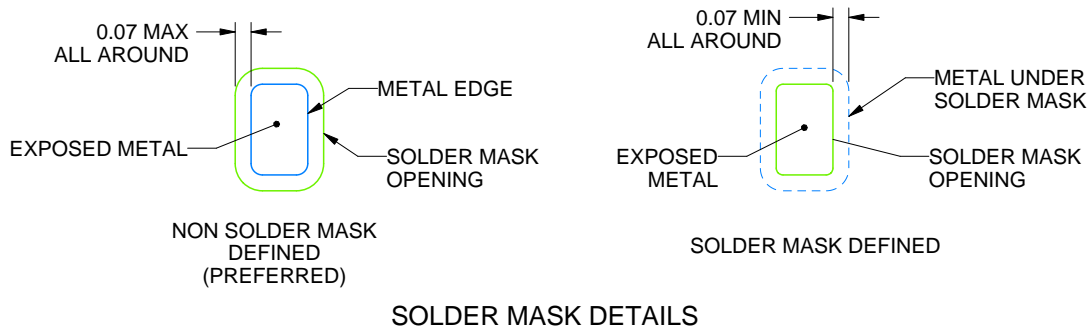
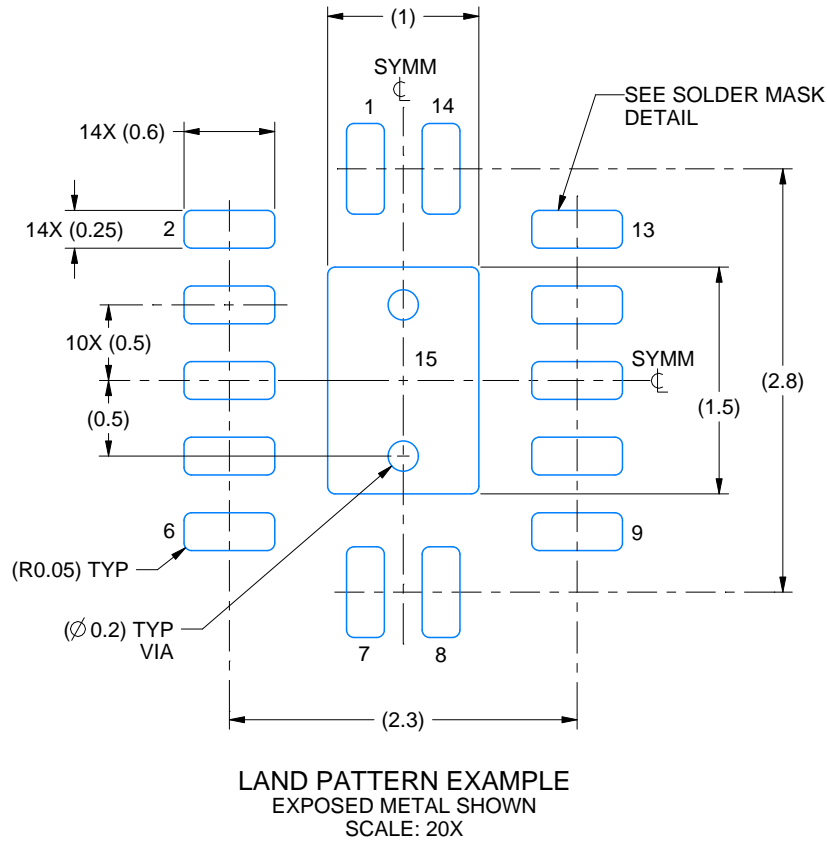
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

**BQA0014B**

**WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



4227062/B 09/2021

NOTES: (continued)

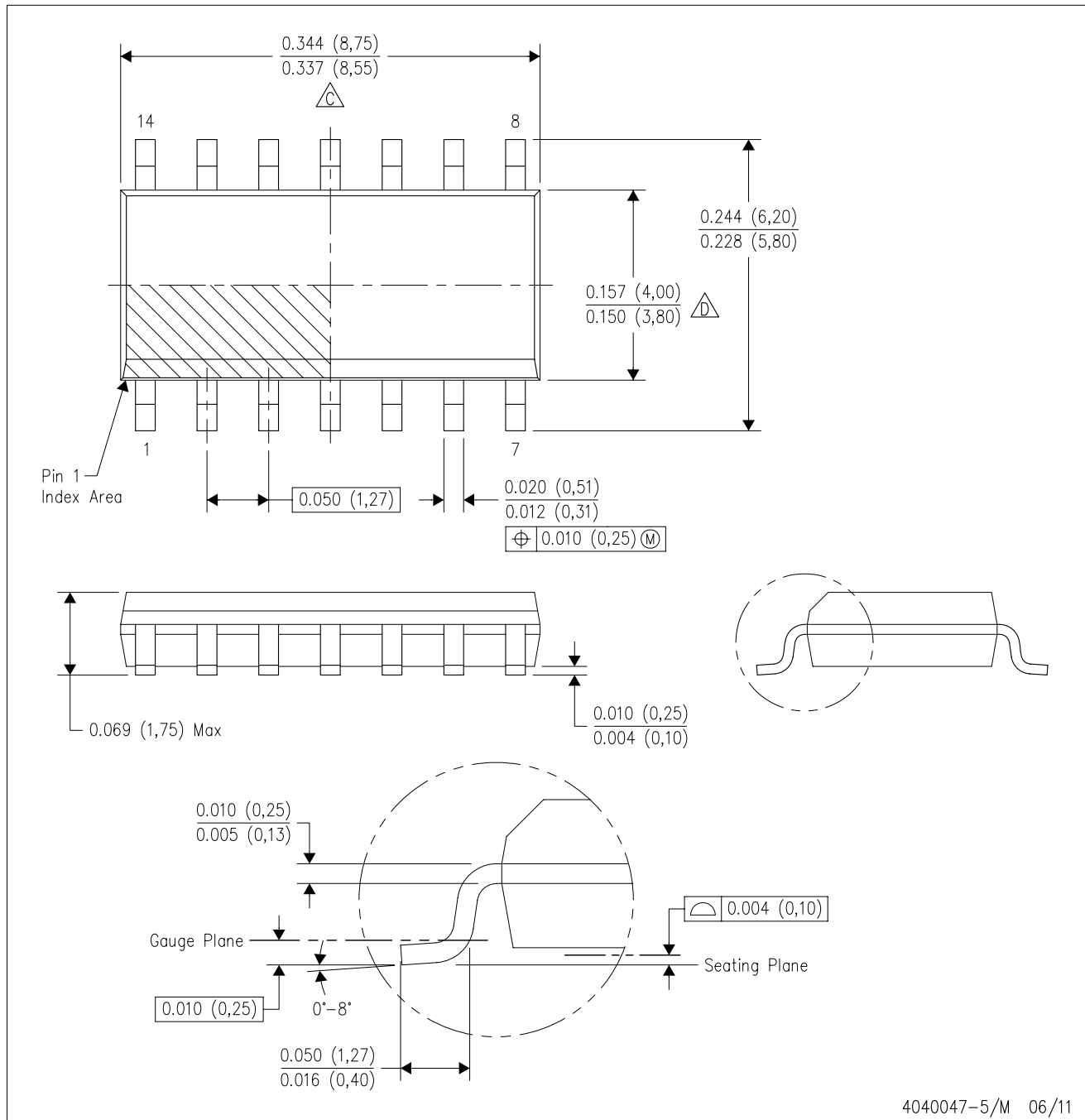
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.





D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.



PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/G 08/15

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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