# 74ALVC541-Q100

## Octal buffer/line driver; 3-state

Rev. 4 — 11 July 2023 Product data sheet

## 1. General description

The 74ALVC541-Q100 is an 8-bit buffer/line driver with 3-state outputs. The device features two output enables ($\overline{OE}1$ and $\overline{OE}2$). A HIGH on $\overline{OE}n$ causes the associated outputs to assume a high-impedance OFF-state.

Schmitt trigger action on all inputs makes the device tolerant of slow rise and fall times.

This device is fully specified for partial power down applications using $I_{OFF}$. The $I_{OFF}$ circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

## 2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 1.65 V to 3.6 V
- CMOS low power dissipation
- Overvoltage tolerant inputs to 3.6 V
- Direct interface with TTL levels
- $I_{OFF}$ circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 250 mA per JESD78 Class II.A
- Complies with JEDEC standard:
  - JESD8-7 (1.65 V to 1.95 V )
  - JESD8-5 (2.3 V to 2.5 V)
  - JESD8B (2.7 V to 3.6 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- DHVQFN package with Side-Wettable Flanks enabling Automatic Optical Inspection (AOI) of solder joints

## 3. Ordering information

**Table 1. Ordering information**

| Type number | Package | | | |
|---|---|---|---|---|
| | Temperature range | Name | Description | Version |
| 74ALVC541D-Q100 | -40 °C to +125 °C | SO20 | plastic small outline package; 20 leads; body width 7.5 mm | SOT163-1 |
| 74ALVC541PW-Q100 | -40 °C to +125 °C | TSSOP20 | plastic thin shrink small outline package; 20 leads; body width 4.4 mm | SOT360-1 |
| 74ALVC541BQ-Q100 | -40 °C to +125 °C | DHVQFN20 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm | SOT764-1 |

## 4. Functional diagram

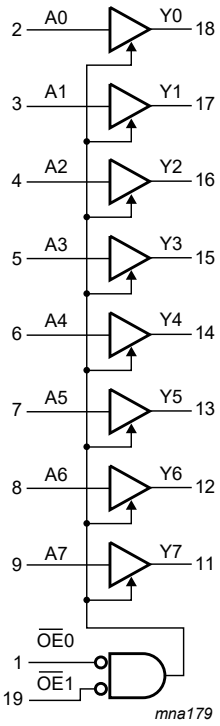



**Fig. 1. Logic symbol**

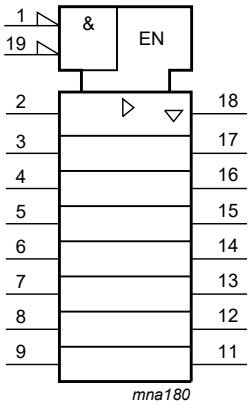
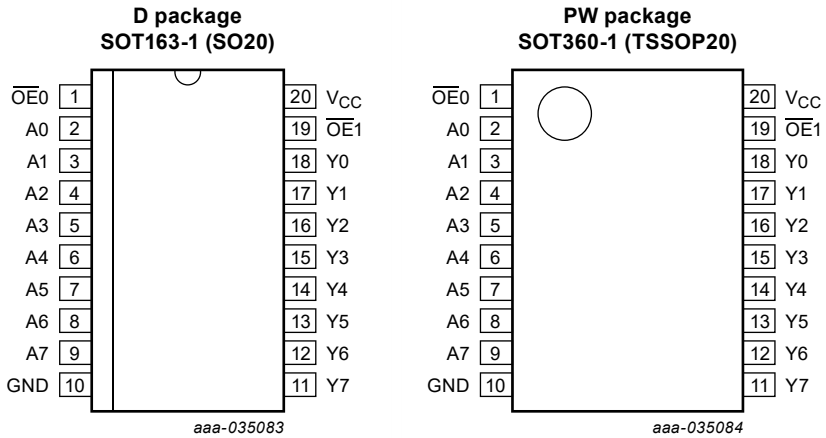
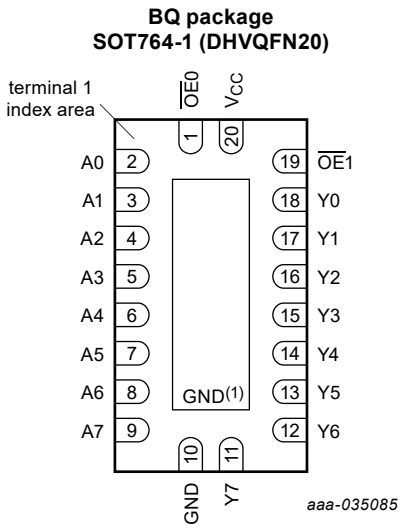



**Fig. 2. IEC logic symbol**

# 5. Pinning information

## 5.1. Pinning




Transparent top view

(1) This is not a ground pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.

## 5.2. Pin description

**Table 2. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| $\overline{OE}0$ | 1 | output enable input (active LOW) |
| A0, A1, A2, A3, A4, A5, A6, A7 | 2, 3, 4, 5, 6, 7, 8, 9 | data input |
| GND | 10 | ground (0 V) |
| Y0, Y1, Y2, Y3, Y4, Y5, Y6, Y7 | 18, 17, 16, 15, 14, 13, 12, 11 | data output |
| $\overline{OE}1$ | 19 | output enable input (active LOW) |
| $V_{CC}$ | 20 | supply voltage |

# 6. Functional description

**Table 3. Functional table**

*H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.*

| Control | | Input | Output |
|---|---|---|---|
| $\overline{OE0}$ | $\overline{OE1}$ | An | Yn |
| L | L | L | L |
| L | L | H | H |
| X | H | X | Z |
| H | X | X | Z |

# 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | -0.5 | +4.6 | V |
| $V_I$ | input voltage | [1] | -0.5 | +4.6 | V |
| $V_O$ | output voltage | output HIGH or LOW state [1] | -0.5 | $V_{CC}$ + 0.5 | V |
| | | output 3-state | -0.5 | +4.6 | V |
| | | power-down mode; $V_{CC}$ = 0 V | -0.5 | +4.6 | V |
| $I_{IK}$ | input clamping current | $V_I$ < 0 V | -50 | - | mA |
| $I_{OK}$ | output clamping current | $V_O$ > $V_{CC}$ or $V_O$ < 0 V | - | ±50 | mA |
| $I_O$ | output current | $V_O$ = 0 V to $V_{CC}$ | - | ±50 | mA |
| $I_{CC}$ | supply current | | - | 100 | mA |
| $I_{GND}$ | ground current | | -100 | - | mA |
| $T_{stg}$ | storage temperature | | -65 | +150 | °C |
| $P_{tot}$ | total power dissipation | $T_{amb}$ = -40 °C to +125 °C [2] | - | 500 | mW |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] For SOT163-1 (SO20) package: $P_{tot}$ derates linearly with 12.3 mW/K above 109 °C.
For SOT360-1 (TSSOP20) package: $P_{tot}$ derates linearly with 10.0 mW/K above 100 °C.
For SOT764-1 (DHVQFN20) package: $P_{tot}$ derates linearly with 12.9 mW/K above 111 °C.

# 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | 1.65 | 3.6 | V |
| $V_I$ | input voltage | | 0 | 3.6 | V |
| $V_O$ | output voltage | output HIGH or LOW state | 0 | $V_{CC}$ | V |
| | | output 3-state | 0 | 3.6 | V |
| | | power-down mode; $V_{CC}$ = 0 V | 0 | 3.6 | V |
| $T_{amb}$ | ambient temperature | | -40 | +125 | °C |
| Δt/ΔV | input transition rise and fall rate | $V_{CC}$ = 1.65 V to 2.7 V | - | 20 | ns/V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | - | 10 | ns/V |

# 9. Static characteristics

**Table 6. Static characteristics**

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | Min | Max | |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | 0.65 × $V_{CC}$ | - | - | 0.65 × $V_{CC}$ | - | V |
| | | $V_{CC}$ = 2.3 V to 2.7V | 1.7 | - | - | 1.7 | - | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 2.0 | - | - | 2.0 | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | - | - | 0.35 × $V_{CC}$ | - | 0.35 × $V_{CC}$ | V |
| | | $V_{CC}$ = 2.3 V to 2.7V | - | - | 0.7 | - | 0.7 | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | - | - | 0.8 | - | 0.8 | V |
| $V_{OH}$ | HIGH-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | | |
| | | $I_O$ = -100 µA; $V_{CC}$ = 1.65 V to 3.6 V | $V_{CC}$ - 0.2 | - | - | $V_{CC}$ - 0.2 | - | V |
| | | $I_O$ = -6mA ; $V_{CC}$ = 1.65 V | 1.25 | 1.51 | - | 1.25 | - | V |
| | | $I_O$ = -12 mA; $V_{CC}$ = 2.3 V | 1.8 | 2.10 | - | 1.8 | - | V |
| | | $I_O$ = -18 mA; $V_{CC}$ = 2.3 V | 1.7 | 2.01 | - | 1.7 | - | V |
| | | $I_O$ = -12 mA; $V_{CC}$ = 2.7 V | 2.2 | 2.53 | - | 2.2 | - | V |
| | | $I_O$ = -18 mA; $V_{CC}$ = 3.0 V | 2.4 | 2.76 | - | 2.4 | - | V |
| | | $I_O$ = -24 mA; $V_{CC}$ = 3.0 V | 2.2 | 2.68 | - | 2.2 | - | V |
| $V_{OL}$ | LOW-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | | |
| | | $I_O$ = 100 µA; $V_{CC}$ = 1.65 V to 3.6 V | - | - | 0.2 | - | 0.2 | V |
| | | $I_O$ = 6 mA ; $V_{CC}$ = 1.65 V | - | 0.11 | 0.3 | - | 0.3 | V |
| | | $I_O$ = 12 mA; $V_{CC}$ = 2.3 V | - | 0.17 | 0.4 | - | 0.4 | V |
| | | $I_O$ = 18 mA; $V_{CC}$ = 2.3 V | - | 0.25 | 0.6 | - | 0.6 | V |
| | | $I_O$ = 12 mA; $V_{CC}$ = 2.7 V | - | 0.16 | 0.4 | - | 0.4 | V |
| | | $I_O$ = 18 mA; $V_{CC}$ = 3.0 V | - | 0.23 | 0.4 | - | 0.45 | V |
| | | $I_O$ = 24 mA; $V_{CC}$ = 3.0 V | - | 0.30 | 0.55 | - | 0.55 | V |
| $I_I$ | input leakage current | $V_I$ = $V_{CC}$ or GND; $V_{CC}$ = 3.6 V | - | ±0.1 | ±5.0 | - | ±20 | µA |
| $I_{OZ}$ | OFF-state output current | $V_I$ = $V_{IH}$ or $V_{IL}$; $V_{CC}$ = 1.65 V to 3.6 V; $V_O$ = 3.6 V or GND | - | ±0.1 | ±10.0 | - | ±80 | µA |
| $I_{OFF}$ | power-off leakage current | $V_I$ or $V_O$ = 0 V to 3.6 V; $V_{CC}$ = 0 V | - | ±0.1 | ±10.0 | - | ±80 | µA |
| $I_{CC}$ | supply current | $V_I$ = $V_{CC}$ or GND; $I_O$ = 0 A; $V_{CC}$ = 3.6 V | - | 0.2 | 10 | - | 80 | µA |
| $\Delta I_{CC}$ | additional supply current | per input pin; $V_{CC}$ = 3.0 V to 3.6 V; $V_I$ = $V_{CC}$ - 0.6 V; $I_O$ = 0 A | - | 5 | 750 | - | 750 | µA |
| $C_I$ | input capacitance | | - | 3.5 | - | - | - | pF |

[1] All typical values are measured at $T_{amb}$ = 25 °C and $V_{CC}$ = 1.8 V, 2.5 V, 2.7 V and 3.3 V.

# 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

*Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 5.*

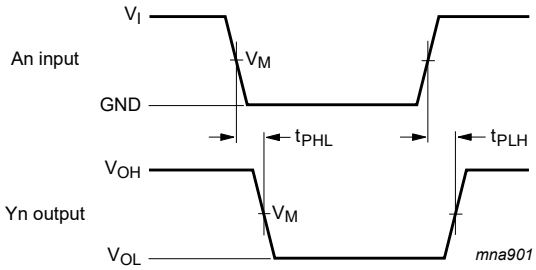
| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | Min | Max | |
| $t_{pd}$ | propagation delay | An to Yn; see Fig. 3 [2] | | | | | | |
| | | $V_{CC}$ = 1.65V to 1.95 V | 1.0 | 3.0 | 4.6 | 1.0 | 5.3 | ns |
| | | $V_{CC}$ = 2.3V to 2.7 V | 1.0 | 2.2 | 3.3 | 1.0 | 3.8 | ns |
| | | $V_{CC}$ = 2.7 V | 1.0 | 2.5 | 3.3 | 1.0 | 3.8 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1.0 | 2.3 | 3.0 | 1.0 | 3.5 | ns |
| $t_{en}$ | enable time | $\overline{OE}$n to Yn; see Fig. 4 [2] | | | | | | |
| | | $V_{CC}$ = 1.65V to 1.95 V | 1.0 | 4.2 | 7.5 | 1.0 | 8.6 | ns |
| | | $V_{CC}$ = 2.3V to 2.7 V | 1.0 | 3.3 | 5.4 | 1.0 | 6.2 | ns |
| | | $V_{CC}$ = 2.7 V | 1.0 | 3.7 | 5.8 | 1.0 | 6.7 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1.0 | 3.3 | 4.9 | 1.0 | 5.6 | ns |
| $t_{dis}$ | disable time | $\overline{OE}$n to Yn; see Fig. 4 [2] | | | | | | |
| | | $V_{CC}$ = 1.65V to 1.95 V | 1.0 | 4.8 | 7.5 | 1.0 | 8.6 | ns |
| | | $V_{CC}$ = 2.3V to 2.7 V | 1.0 | 3.1 | 4.5 | 1.0 | 5.2 | ns |
| | | $V_{CC}$ = 2.7 V | 1.0 | 3.1 | 4.8 | 1.0 | 5.5 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1.0 | 2.9 | 4.6 | 1.0 | 5.3 | ns |
| $C_{PD}$ | power dissipation capacitance | per buffer; $V_I$ = GND to $V_{CC}$; $V_{CC}$ = 3.3 V [3] | | | | | | |
| | | outputs HIGH or LOW state | - | 25 | - | - | - | pF |
| | | outputs 3-state | - | 1 | - | - | - | pF |

[1] All typical values are measured at Tamb = 25 °C and $V_{CC}$ = 1.8 V, 2.5 V, 2.7 V and 3.3 V.

[2] $t_{pd}$ is the same as $t_{PLH}$ and $t_{PHL}$.
$t_{en}$ is the same as $t_{PZL}$ and $t_{PZH}$.
$t_{dis}$ is the same as $t_{PLZ}$ and $t_{PHZ}$.

[3] $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
$f_i$ = input frequency in MHz;
$f_o$ = output frequency in MHz;
$C_L$ = output load capacitance in pF;
$V_{CC}$ = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

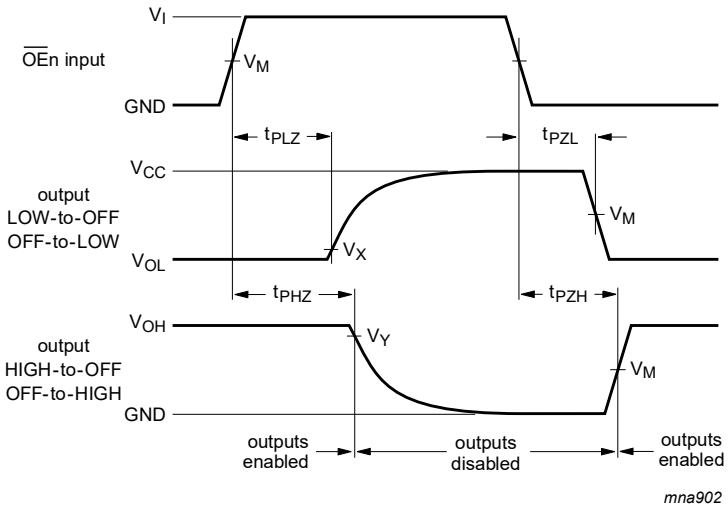
## 10.1. Waveforms and test circuit




Measurement points are given in Table 8.

$V_{OL}$ and $V_{OH}$ are typical voltage output levels that occur with the output load.

**Fig. 3. Propagation delay input (An) to output (Yn)**



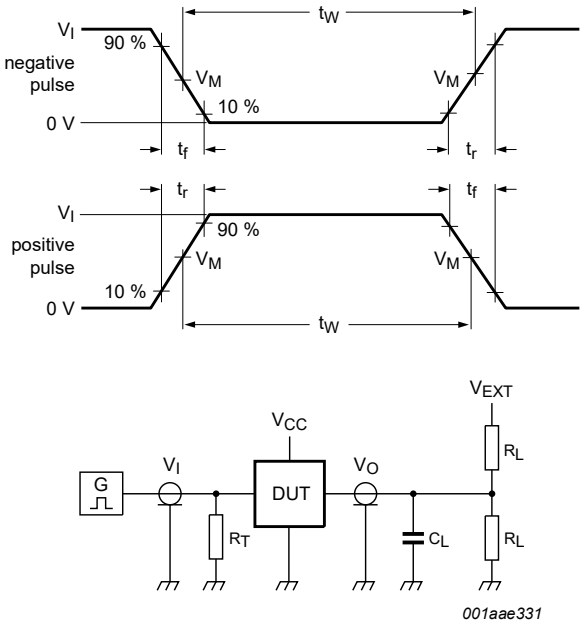

Measurement points are given in Table 8.

$V_{OL}$ and $V_{OH}$ are typical voltage output levels that occur with the output load.

**Fig. 4. Enable and disable times**

**Table 8. Measurement points**

| Supply voltage | Input | | Output | | |
|---|---|---|---|---|---|
| $V_{CC}$ | $V_I$ | $V_M$ | $V_M$ | $V_X$ | $V_Y$ |
| 1.65 V to 1.65V | $V_{CC}$ | 0.5 × $V_{CC}$ | 0.5 × $V_{CC}$ | $V_{OL}$ + 0.15 V | $V_{OH}$ - 0.15 V |
| 2.3 V to 2.7 V | $V_{CC}$ | 0.5 × $V_{CC}$ | 0.5 × $V_{CC}$ | $V_{OL}$ + 0.15 V | $V_{OH}$ - 0.15 V |
| 2.7 V | 2.7 V | 1.5 V | 1.5 V | $V_{OL}$ + 0.3 V | $V_{OH}$ - 0.3 V |
| 3.0 V to 3.6 V | 2.7 V | 1.5 V | 1.5 V | $V_{OL}$ + 0.3 V | $V_{OH}$ - 0.3 V |




Test data is given in Table 9.

Definitions test circuit:

$R_T$ = Termination resistance should be equal to output impedance $Z_o$ of the pulse generator;

$C_L$ = Load capacitance including jig and probe capacitance;

$R_L$ = Load resistor.

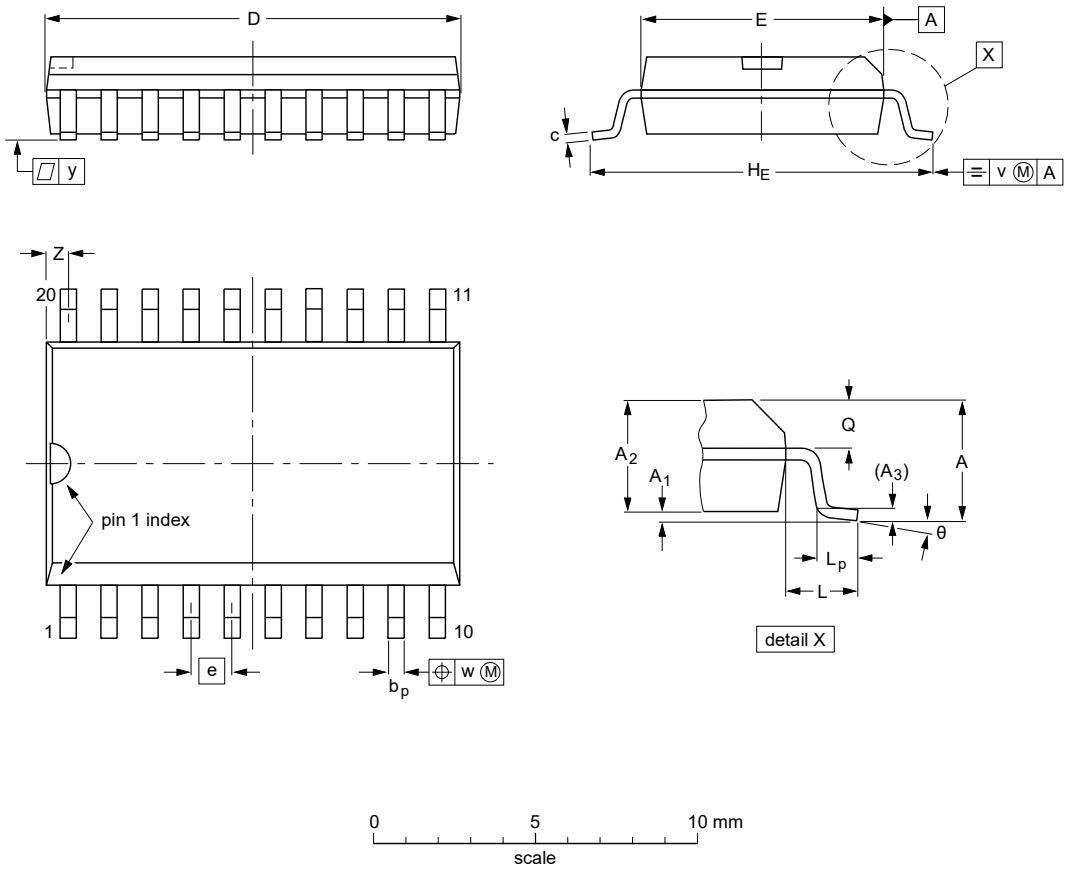
**Fig. 5. Test circuit for measuring switching times**

**Table 9. Test data**

| Supply voltage | Input | | Load | | $V_{EXT}$ | | |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | $V_I$ | $t_r$, $t_f$ | $C_L$ | $R_L$ | $t_{PLH}$, $t_{PHL}$ | $t_{PLZ}$, $t_{PZL}$ | $t_{PHZ}$, $t_{PZH}$ |
| 1.65 V to 1.95 V | $V_{CC}$ | ≤ 2.0 ns | 30 pF | 1 kΩ | open | 2 × $V_{CC}$ | GND |
| 2.3 V to 2.7 V | $V_{CC}$ | ≤ 2.0 ns | 30 pF | 500 Ω | open | 2 × $V_{CC}$ | GND |
| 2.7 V | 2.7 V | ≤ 2.5 ns | 50 pF | 500 Ω | open | 6 V | GND |
| 3.0 V to 3.6 V | 2.7 V | ≤ 2.5 ns | 50 pF | 500 Ω | open | 6 V | GND |

# 11. Package outline

**SO20: plastic small outline package; 20 leads; body width 7.5 mm** **SOT163-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2.65 | 0.3<br>0.1 | 2.45<br>2.25 | 0.25 | 0.49<br>0.36 | 0.32<br>0.23 | 13.0<br>12.6 | 7.6<br>7.4 | 1.27 | 10.65<br>10.00 | 1.4 | 1.1<br>0.4 | 1.1<br>1.0 | 0.25 | 0.25 | 0.1 | 0.9<br>0.4 | 8°<br>0° |
| inches | 0.1 | 0.012<br>0.004 | 0.096<br>0.089 | 0.01 | 0.019<br>0.014 | 0.013<br>0.009 | 0.51<br>0.49 | 0.30<br>0.29 | 0.05 | 0.419<br>0.394 | 0.055 | 0.043<br>0.016 | 0.043<br>0.039 | 0.01 | 0.01 | 0.004 | 0.035<br>0.016 | |

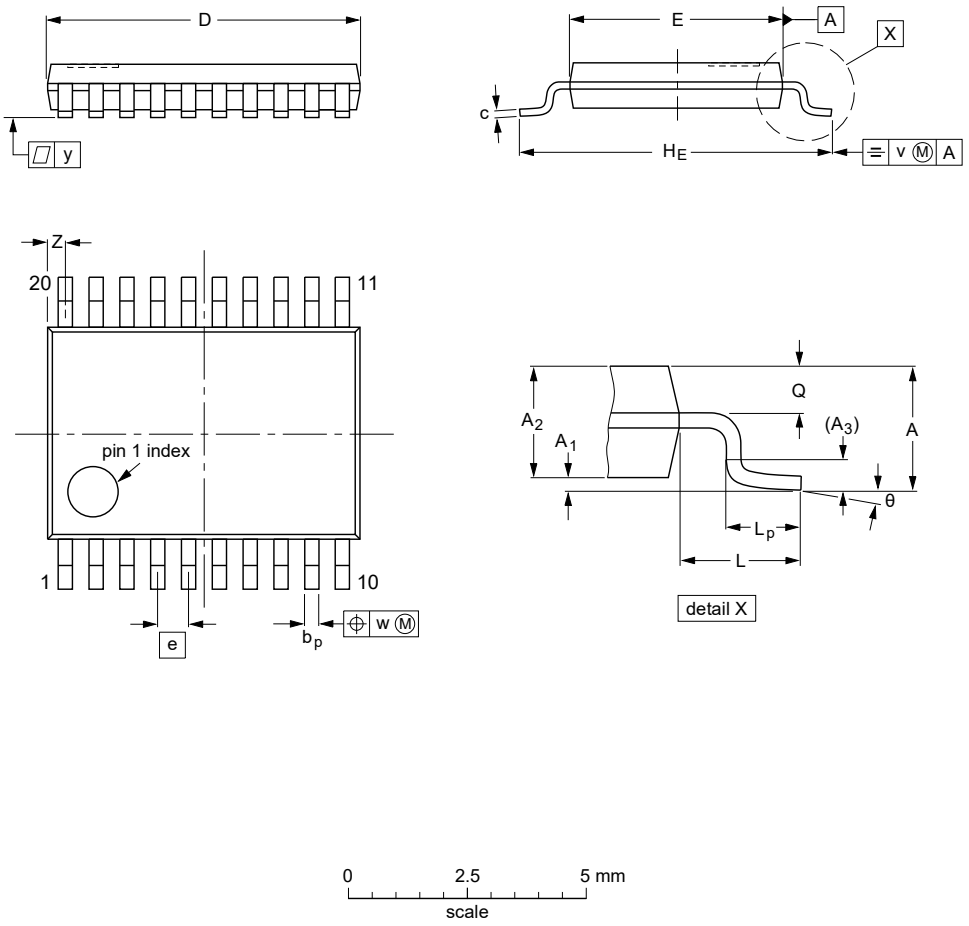
**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT163-1 | 075E04 | MS-013 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig. 6. Package outline SOT163-1 (SO20)**

**TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm** **SOT360-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (2) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1 | 0.15<br>0.05 | 0.95<br>0.80 | 0.25 | 0.30<br>0.19 | 0.2<br>0.1 | 6.6<br>6.4 | 4.5<br>4.3 | 0.65 | 6.6<br>6.2 | 1 | 0.75<br>0.50 | 0.4<br>0.3 | 0.2 | 0.13 | 0.1 | 0.5<br>0.2 | 8°<br>0° |

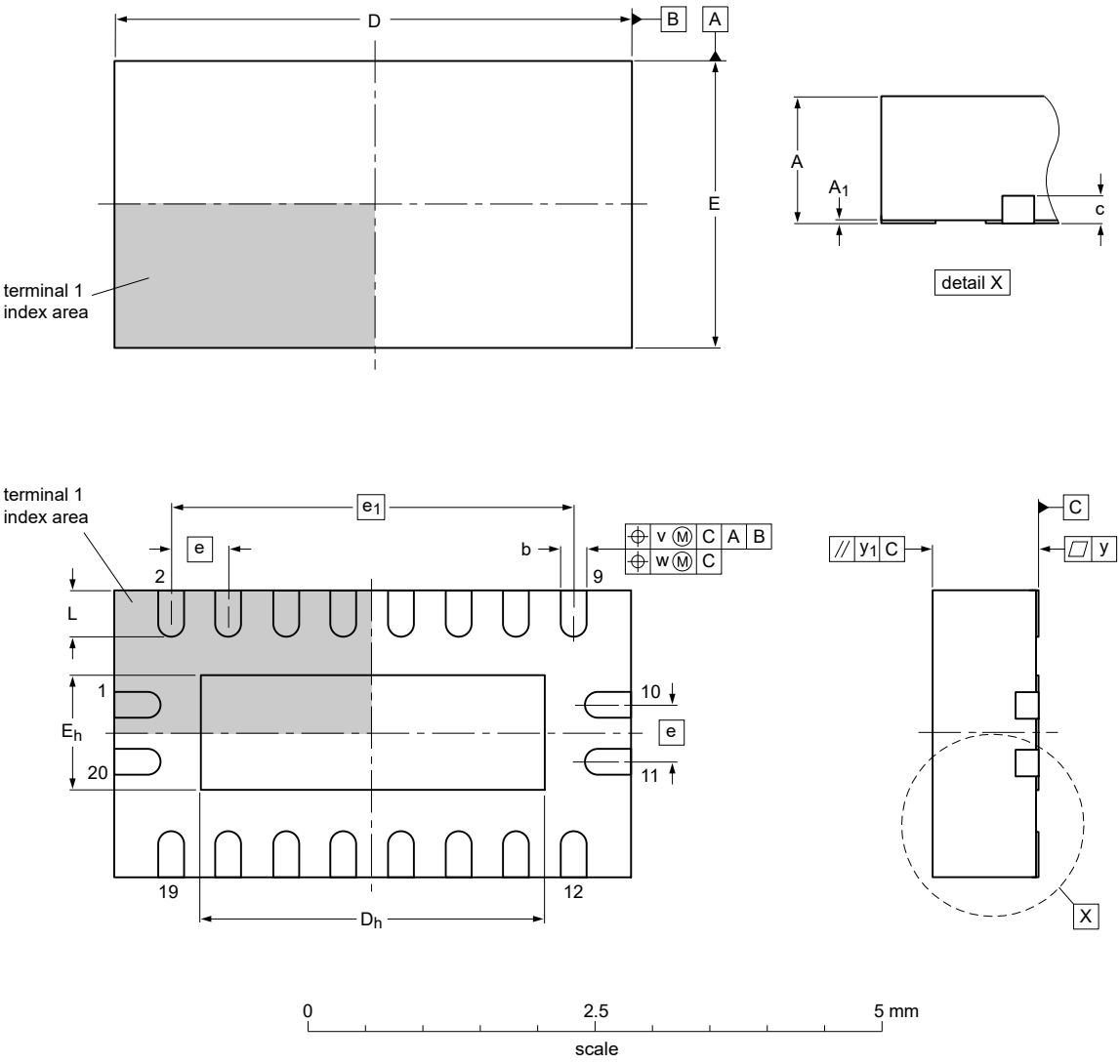
**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT360-1 | | MO-153 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig. 7. Package outline SOT360-1 (TSSOP20)**

**DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm** **SOT764-1**




Dimensions (mm are the original dimensions)

| Unit | | $A^{(1)}$ | $A_1$ | b | c | $D^{(1)}$ | $D_h$ | $E^{(1)}$ | $E_h$ | e | $e_1$ | L | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | max | 1.00 | 0.05 | 0.30 | | 4.6 | 3.15 | 2.6 | 1.15 | | | 0.5 | | | | |
| mm | nom | 0.90 | 0.02 | 0.25 | 0.2 | 4.5 | 3.00 | 2.5 | 1.00 | 0.5 | 3.5 | 0.4 | 0.1 | 0.05 | 0.05 | 0.1 |
| | min | 0.80 | 0.00 | 0.18 | | 4.4 | 2.85 | 2.4 | 0.85 | | | 0.3 | | | | |

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

*sot764-1_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT764-1 | - - - | MO-241 | - - - | | | ~~03-01-27~~ 14-12-12 |

**Fig. 8. Package outline SOT764-1 (DHVQFN20)**

## 12. Abbreviations

**Table 10. Abbreviations**

| Acronym | Description |
|---|---|
| CDM | Charged Device Model |
| CMOS | Complementary Metal Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| TTL | Transistor-Transistor Logic |

## 13. Revision history

**Table 11. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| 74ALVC541_Q100 v.4 | 20230711 | Product data sheet | - | 74ALVC541_Q100 v.3 |
| Modifications: | • Section 1 updated.<br>• Section 2: ESD specification updated according to the latest JEDEC standard.<br>• Table 6: errata. | | | |
| 74ALVC541_Q100 v.3 | 20210430 | Product data sheet | - | 74ALVC541_Q100 v.2 |
| Modifications: | • Section 2: Reference to JESD36 removed.<br>• Table 4: Derating values for $P_{tot}$ total power dissipation removed (errata). | | | |
| 74ALVC541_Q100 v.2 | 20200930 | Product data sheet | - | 74ALVC541_Q100 v.1 |
| Modifications: | • The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.<br>• Legal texts have been adapted to the new company name where appropriate.<br>• Section 2 updated.<br>• Table 4: Derating values for $P_{tot}$ total power dissipation have been updated.<br>• Table 6: typo corrected.<br>• Table 7: typo corrected.<br>• Package outline drawing of SOT764-1 (Fig. 8) updated. | | | |
| 74ALVC541_Q100 v.1 | 20140519 | Product data sheet | - | - |

# 14. Legal information

## Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

## Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Nexperia does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local Nexperia sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification** — The information and data provided in a Product data sheet shall define the specification of the product as agreed between Nexperia and its customer, unless Nexperia and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the Nexperia product is deemed to offer functions and qualities beyond those described in the Product data sheet.

## Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, Nexperia does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. Nexperia takes no responsibility for the content in this document if provided by an information source outside of Nexperia.

In no event shall Nexperia be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, Nexperia's aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of Nexperia.

**Right to make changes** — Nexperia reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use in automotive applications** — This Nexperia product has been qualified for use in automotive applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an Nexperia product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Nexperia and its suppliers accept no liability for inclusion and/or use of Nexperia products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Quick reference data** — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. Nexperia makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using Nexperia products, and Nexperia accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the Nexperia product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

Nexperia does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using Nexperia products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). Nexperia does not accept any liability in this respect.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale** — Nexperia products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nexperia.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Nexperia hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of Nexperia products by customer.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Translations** — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

## Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

# Contents

**1. General description....1**
**2. Features and benefits....1**
**3. Ordering information....2**
**4. Functional diagram....2**
**5. Pinning information....3**
5.1. Pinning....3
5.2. Pin description....3
**6. Functional description....4**
**7. Limiting values....4**
**8. Recommended operating conditions....4**
**9. Static characteristics....5**
**10. Dynamic characteristics....6**
10.1. Waveforms and test circuit....7
**11. Package outline....9**
**12. Abbreviations....12**
**13. Revision history....12**
**14. Legal information....13**


**Date of release: 11 July 2023**