

# NTB5404N, NTP5404N, NVB5404N

## Power MOSFET

40 V, 167 A, Single N-Channel, D<sup>2</sup>PAK & TO-220

### Features

- Low  $R_{DS(on)}$
- High Current Capability
- Low Gate Charge
- AEC-Q101 Qualified and PPAP Capable – NVB5404N
- These Devices are Pb-Free and are RoHS Compliant

### Applications

- Electronic Brake Systems
- Electronic Power Steering
- Bridge Circuits

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter		Symbol	Value	Units	
Drain-to-Source Voltage		$V_{DSS}$	40	V	
Gate-to-Source Voltage		$V_{GS}$	$\pm 20$	V	
Continuous Drain Current – $R_{\theta JC}$	Steady State	$T_C = 25^\circ\text{C}$	$I_D$	167	A
			$T_C = 100^\circ\text{C}$	118	
Power Dissipation – $R_{\theta JC}$	Steady State	$T_C = 25^\circ\text{C}$	$P_D$	254	W
Continuous Drain Current – $R_{\theta JA}$ (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	$I_D$	24	A
			$T_A = 100^\circ\text{C}$	17	
Power Dissipation – $R_{\theta JA}$ (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	$P_D$	5.4	W
Pulsed Drain Current	$t_p = 10 \mu\text{s}$		$I_{DM}$	670	A
Operating Junction and Storage Temperature		$T_J, T_{STG}$	-55 to 175	$^\circ\text{C}$	
Source Current (Body Diode) Pulsed		$I_S$	75	A	
Single Pulse Drain-to-Source Avalanche Energy – ( $V_{DD} = 50 \text{ V}, V_{GS} = 10 \text{ V}, I_{PK} = 45 \text{ A}, L = 1 \text{ mH}, R_G = 25 \Omega$ )		EAS	1000	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		$T_L$	260	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	0.59	$^\circ\text{C/W}$
Junction-to-Ambient (Note 1)	$R_{\theta JA}$	50	$^\circ\text{C/W}$

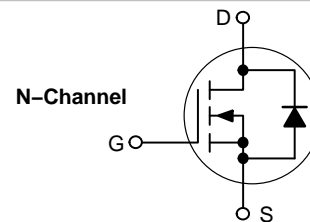
1. Surface mounted on FR4 board using 1 sq in pad size, (Cu Area 1.127 sq in [2 oz] including traces).



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$V_{(BR)DSS}$	$R_{DS(on) MAX}$	$I_D MAX$ (Note 1)
40 V	4.5 m $\Omega$ @ 10 V	167 A



**MARKING DIAGRAMS**

**D<sup>2</sup>PAK  
CASE 418B  
STYLE 2**

**TO-220AB  
CASE 221A  
STYLE 5**

1 = Pb-Free Device  
 A = Assembly Location  
 Y = Year  
 WW = Work Week

### ORDERING INFORMATION

Device	Package	Shipping†
NTB5404NT4G	D <sup>2</sup> PAK (Pb-Free)	800 / Tape & Reel
NTP5404NRG	TO-220 (Pb-Free)	50 Units / Rail
NVB5404NT4G	D <sup>2</sup> PAK (Pb-Free)	800 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise stated)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T <sub>J</sub>			34		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 40 V	T <sub>J</sub> = 25°C		1.0	μA
			T <sub>J</sub> = 100°C		10	
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±30 V			±100	nA

## ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA	1.5		3.5	V
Gate Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>			-8.2		mV/°C
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 40 A		3.5	4.5	mΩ
		V <sub>GS</sub> = 5.0 V, I <sub>D</sub> = 15 A		5.1	7.0	
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 15 A		35		S

## CHARGES AND CAPACITANCES

Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> = 0 V, f = 1.0 MHz, V <sub>DS</sub> = 32 V		4300	7000	pF
Output Capacitance	C <sub>OSS</sub>			1075	1700	
Reverse Transfer Capacitance	C <sub>RSS</sub>			450	1000	
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 32 V, I <sub>D</sub> = 40 A		125		nC
Threshold Gate Charge	Q <sub>G(TH)</sub>			5.5		
Gate-to-Source Charge	Q <sub>GS</sub>			12.5		
Gate-to-Drain Charge	Q <sub>GD</sub>			55		

## SWITCHING CHARACTERISTICS, V<sub>GS</sub> = 10 V (Note 3)

Turn-On Delay Time	t <sub>d(ON)</sub>	V <sub>GS</sub> = 10 V, V <sub>DD</sub> = 32 V, I <sub>D</sub> = 40 A, R <sub>G</sub> = 2.5 Ω		10		ns
Rise Time	t <sub>r</sub>			65		
Turn-Off Delay Time	t <sub>d(OFF)</sub>			85		
Fall Time	t <sub>f</sub>			85		

## SWITCHING CHARACTERISTICS, V<sub>GS</sub> = 5 V (Note 3)

Turn-On Delay Time	t <sub>d(ON)</sub>	V <sub>GS</sub> = 5 V, V <sub>DD</sub> = 20 V, I <sub>D</sub> = 20 A, R <sub>G</sub> = 2.5 Ω		25		ns
Rise Time	t <sub>r</sub>			175		
Turn-Off Delay Time	t <sub>d(OFF)</sub>			46		
Fall Time	t <sub>f</sub>			62		

## DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 20 A	T <sub>J</sub> = 25°C		0.8	1.1	V
			T <sub>J</sub> = 125°C		0.65		
Reverse Recovery Time	t <sub>RR</sub>	V <sub>GS</sub> = 0 V, dI <sub>SD</sub> /dt = 100 A/μs, I <sub>S</sub> = 20 A			75		ns
Charge Time	t <sub>a</sub>				38		
Discharge Time	t <sub>b</sub>				38		
Reverse Recovery Charge	Q <sub>RR</sub>				140		

2. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

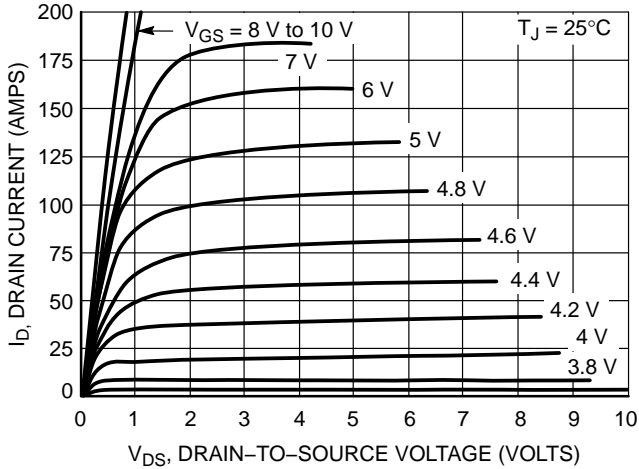


Figure 1. On-Region Characteristics

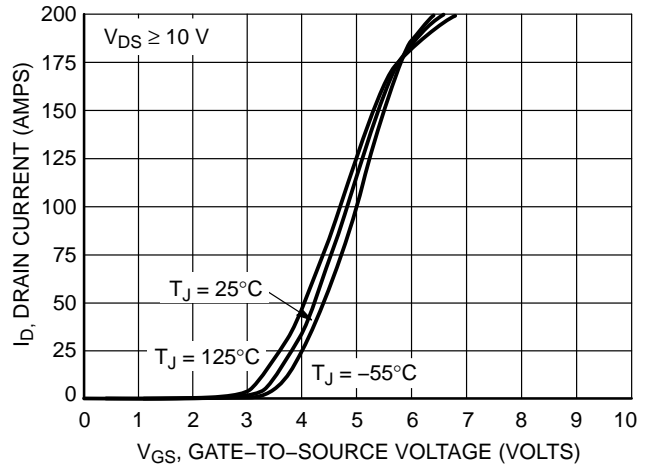


Figure 2. Transfer Characteristics

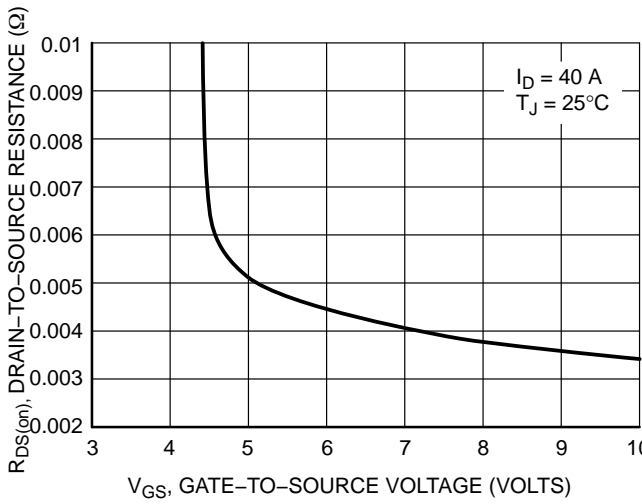


Figure 3. On-Resistance vs. Gate-to-Source Voltage

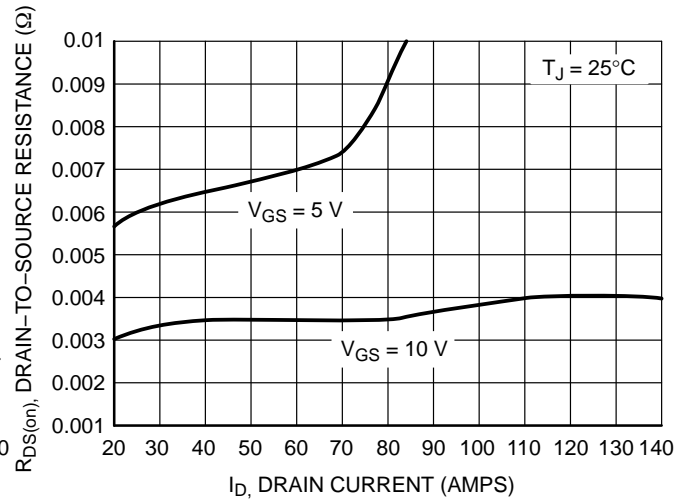


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

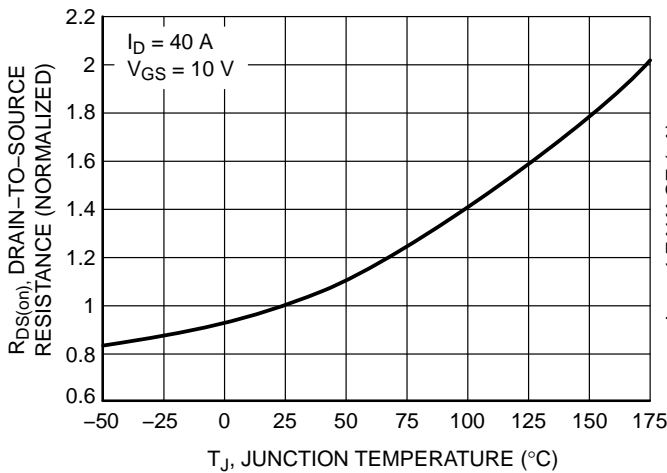


Figure 5. On-Resistance Variation with Temperature

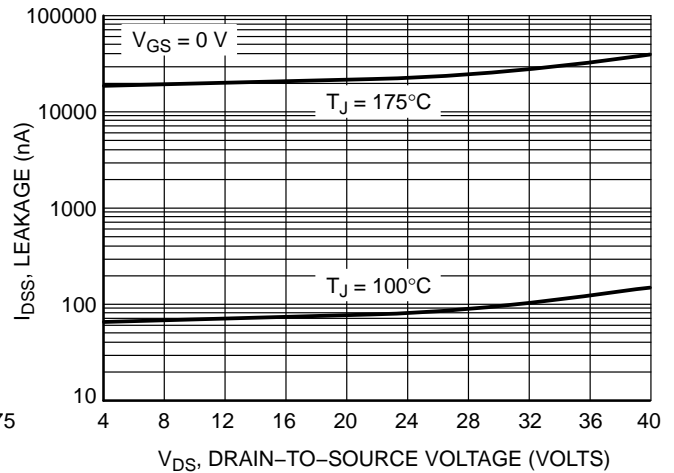


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES

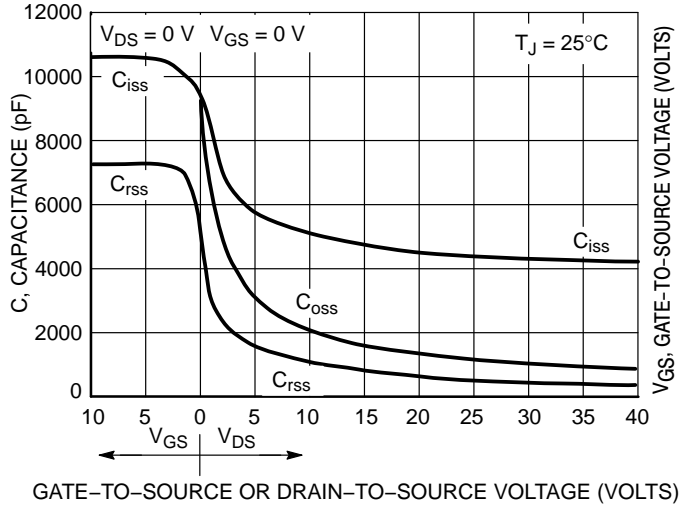


Figure 7. Capacitance Variation

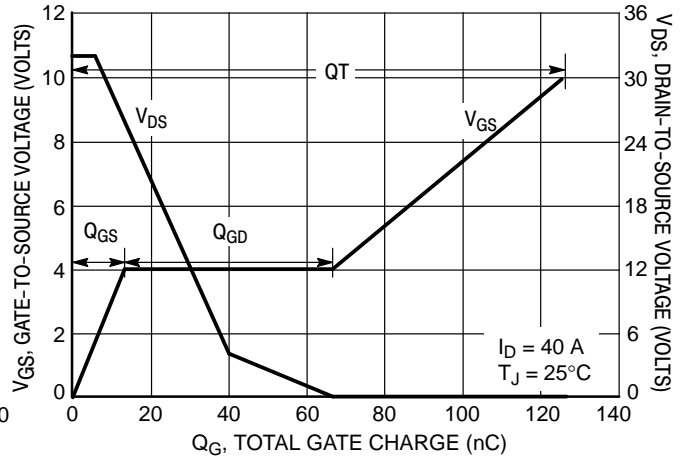


Figure 8. Gate-To-Source and Drain-To-Source Voltage vs. Total Charge

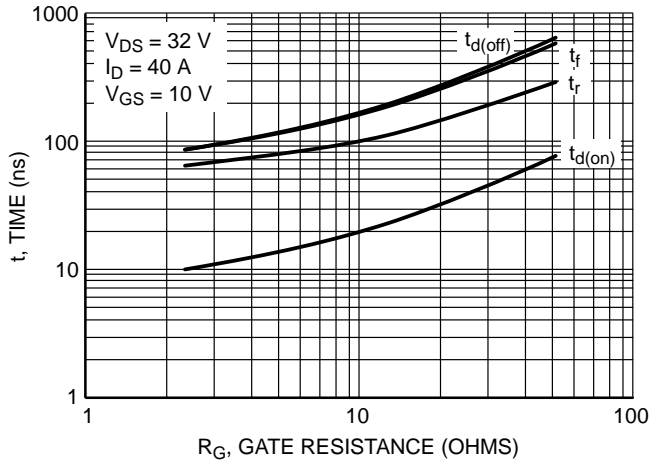


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

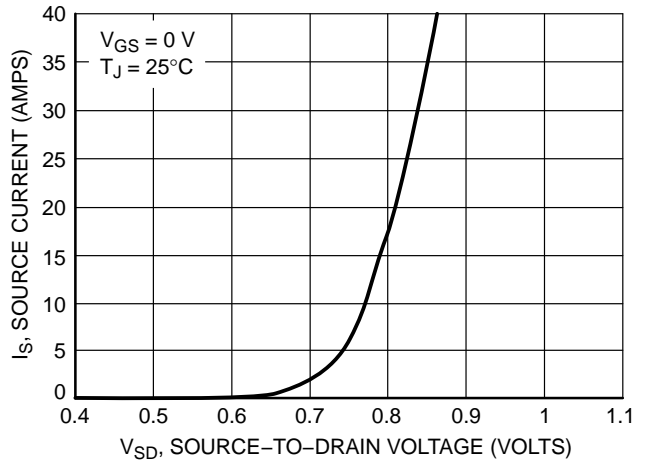


Figure 10. Diode Forward Voltage vs. Current

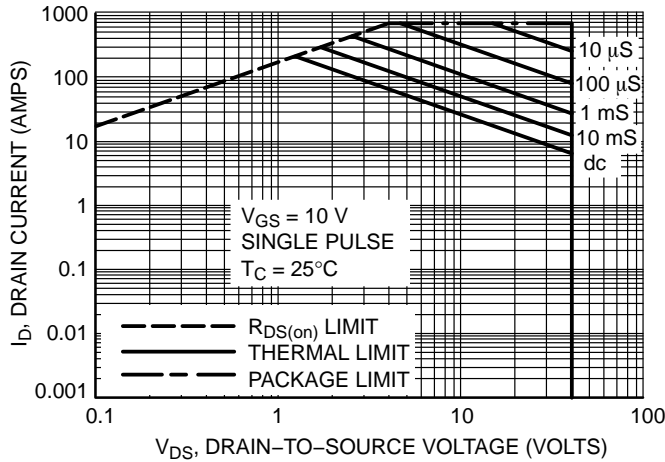


Figure 11. Maximum Rated Forward Biased Safe Operating Area

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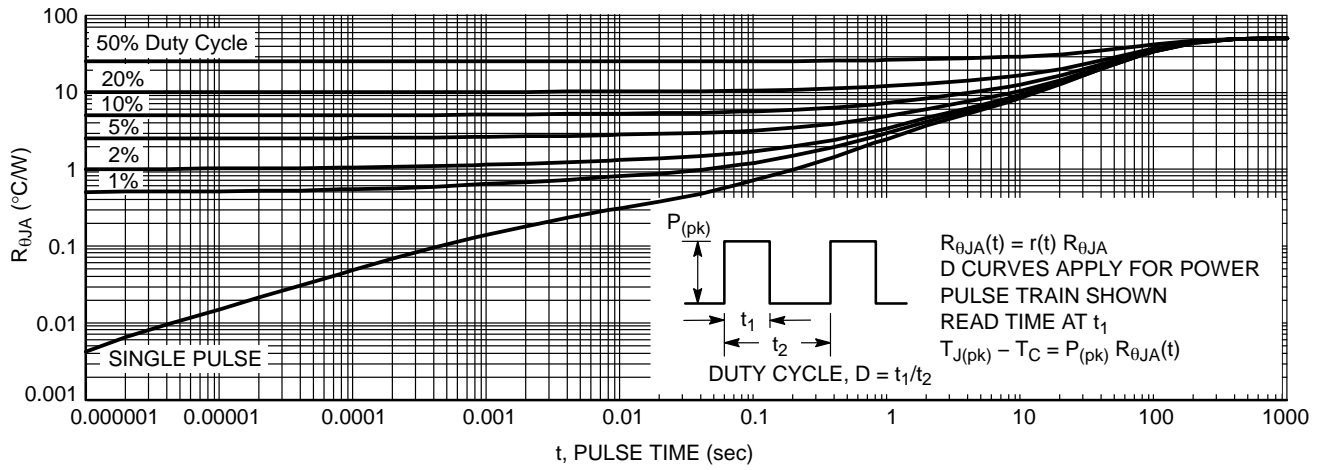
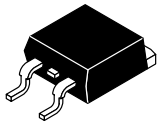


Figure 12. Thermal Response

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

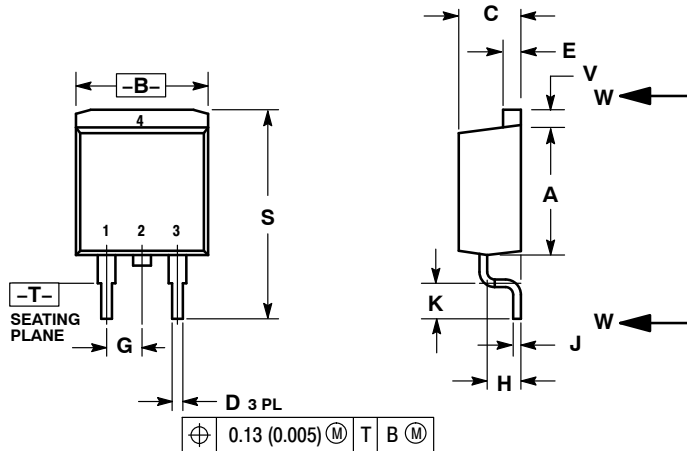
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**D<sup>2</sup>PAK 3**  
CASE 418B-04  
ISSUE L

DATE 17 FEB 2015

SCALE 1:1

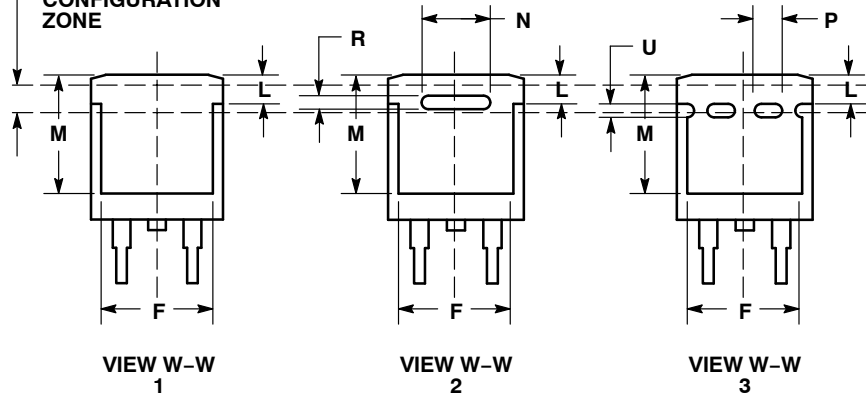


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 418B-01 THRU 418B-03 OBSOLETE, NEW STANDARD 418B-04.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
F	0.310	0.350	7.87	8.89
G	0.100	BSC	2.54	BSC
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
L	0.052	0.072	1.32	1.83
M	0.280	0.320	7.11	8.13
N	0.197	REF	5.00	REF
P	0.079	REF	2.00	REF
R	0.039	REF	0.99	REF
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

**VARIABLE CONFIGURATION ZONE**



- |  |   |   |  |   |  |
|--|---|---|--|---|--|
| <b>STYLE 1:</b><br>PIN 1. BASE<br>2. COLLECTOR<br>3. EMITTER<br>4. COLLECTOR | <b>STYLE 2:</b><br>PIN 1. GATE<br>2. DRAIN<br>3. SOURCE<br>4. DRAIN | <b>STYLE 3:</b><br>PIN 1. ANODE<br>2. CATHODE<br>3. ANODE<br>4. CATHODE | <b>STYLE 4:</b><br>PIN 1. GATE<br>2. COLLECTOR<br>3. EMITTER<br>4. COLLECTOR | <b>STYLE 5:</b><br>PIN 1. CATHODE<br>2. ANODE<br>3. CATHODE<br>4. ANODE | <b>STYLE 6:</b><br>PIN 1. NO CONNECT<br>2. CATHODE<br>3. ANODE<br>4. CATHODE |
|--|---|---|--|---|--|

**MARKING INFORMATION AND FOOTPRINT ON PAGE 2**

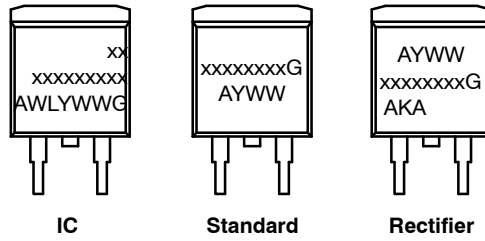
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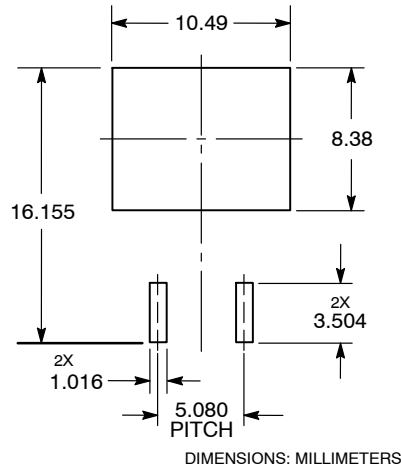
**GENERIC  
MARKING DIAGRAM\***



- xx = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package
- AKA = Polarity Indicator

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

**SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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