

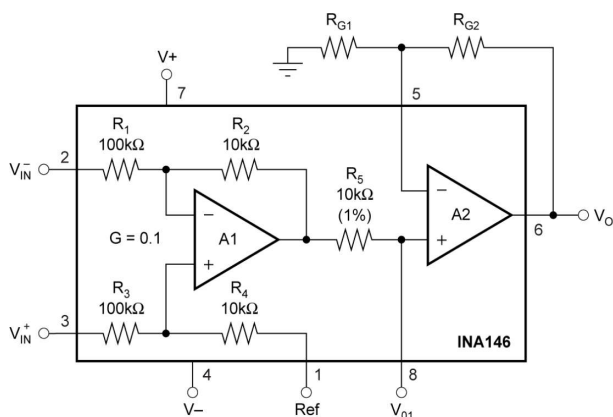
INA146 High-voltage, Programmable Gain Difference Amplifier

1 Features

- High common-mode voltage:
 - 40 V at $V_S = 5\text{ V}$
 - $\pm 100\text{ V}$ at $V_S = \pm 15\text{ V}$
- Differential gain = 0.1 V/V TO 100 V/V:
 - Set with External Resistors
- Low quiescent current: 570 μA
- Wide supply range:
 - Single Supply: 4.5 V to 36 V
 - Dual Supplies: $\pm 2.25\text{ V}$ to $\pm 18\text{ V}$
- Low gain error: 0.025%
- High common-mode rejection: 80 dB

2 Applications

- [Battery cell formation & test equipment](#)
- [AC drive control module](#)
- [HVAC controller](#)
- [Professional audio amplifier \(rack mount\)](#)
- [Programmable DC power source](#)
- [Data acquisition \(DAQ\)](#)



INA146 Simplified Block Diagram

3 Description

The INA146 is a precision difference amplifier that can be used to accurately attenuate high differential voltages and reject high common-mode voltages for compatibility with common signal processing voltage levels. High-voltage capability also affords inherent input protection. The input common-mode range extends beyond both supply rails, making the INA146 an excellent choice for both single and dual supply applications.

On-chip precision resistors are laser-trimmed to achieve accurate gain and high common-mode rejection. Excellent TCR tracking of these resistors provides continued high precision over temperature.

A 10:1 difference amplifier provides 0.1 V/V gain when the output amplifier is used as a unity-gain buffer. In this configuration, input voltages up to $\pm 100\text{ V}$ can be measured. Gains greater than 0.1 V/V can be set with an external resistor pair without affecting the common-mode input range.

The INA146 is available in the SO-8 surface-mount package specified for the extended industrial temperature range, -40°C to 85°C .

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	SPECIFIED TEMPERATURE RANGE	PACKAGE SIZE ⁽²⁾
INA146	SOIC (8)	-40°C to 85°C	4.90 mm × 6.00 mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.



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4 Pin Configuration and Functions

Top View

SO-8

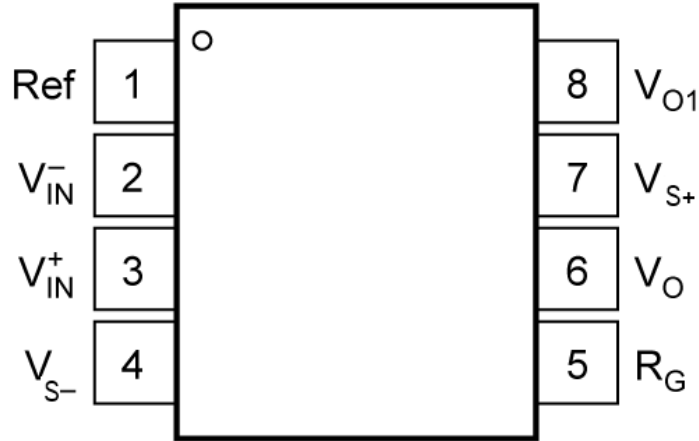


Figure 4-1. INA146 D Package, 8-Pin SOIC (Top View)

Table 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
Ref	1	I	Reference input. This pin must be driven by a low impedance source.
V _{IN-}	2	I	Negative (inverting) input
V _{IN+}	3	I	Positive (non-inverting) input
V _{S-}	4	-	Negative supply
R _G	5	I	Gain setting input. Place a resistor network between pin 1 and pin 5.
V _O	6	O	Output of amplifier A2
V _{S+}	7	-	Positive supply
V _{O1}	8	O	Output of amplifier A1

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _S	Supply voltage	Dual supply, V _S = (V _{S+}) – (V _{S-})		±18	V
		Single supply, V _S = (V _{S+}) – 0 V		36	
V _{IN+} , V _{IN-}	Signal input voltage			±100	V
	Signal input current			±1	mA
	Output short-circuit ⁽²⁾		Continuous		
T _A	Operating temperature		–55	125	°C
T _{stg}	Storage temperature		–55	125	°C
T _J	Junction temperature			150	°C
	Lead temperature (soldering, 10 s)			240	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Short-circuit to V_S / 2.

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
V _S	Supply voltage	Single-supply	4.5	30	36	V
		Dual-supply	±2.25	±15	±18	
T _A	Specified temperature		–40		85	°C

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		INA146	UNIT
		SO-8	
		8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	110.3	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	43.6	°C/W
R _{θJB}	Junction-to-board thermal resistance	55.5	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	6.2	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	54.3	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.5 Electrical Characteristics $V_S = \pm 2.25\text{ V to } \pm 18\text{ V}$

at $T_A = 25^\circ\text{C}$, $V_S = \pm 2.25\text{ V to } \pm 18\text{ V}$, $R_L = 10\text{ k}\Omega$, $V_{REF} = 0\text{ V}$, $V_{CM} = V_S / 2$, and $G = 0.1$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT							
V_{OS}	Offset voltage, V_O	RTI, $V_S = \pm 15\text{ V}$, $V_{CM} = 0\text{ V}$			± 1	± 5	mV
	Offset voltage, V_{O1}	RTI			± 1		mV
	Offset voltage drift	RTI, $T_A = -40^\circ\text{C to } 85^\circ\text{C}$			± 10		$\mu\text{V}/^\circ\text{C}$
PSRR	Power-supply rejection ratio	RTI, $V_S = \pm 1.35\text{ V to } \pm 18\text{ V}$			± 100	± 600	$\mu\text{V}/\text{V}$
V_{CM}	Common-mode voltage ⁽¹⁾	$V_S = \pm 15\text{ V}$, $V_{IN} = 0\text{ V}$		-100		100	V
CMRR	Common-mode voltage rejection	RTI, $11(-V_S) < V_{CM} < 11(V_S - 1)$, $R_S = 0\ \Omega$		70	80		dB
		$T_A = -40^\circ\text{C to } 85^\circ\text{C}$		64	74		
	Differential input impedance	Non-inverting input			110		k Ω
		Inverting input			91.7		
	Common-mode input impedance				55		k Ω
BIAS CURRENT							
I_B	Bias Current	$V_{CM} = V_S / 2$			± 50		nA
I_{OS}	Offset Current				± 5		nA
NOISE							
e_N	Voltage noise	RTI, $f_B = 0.1\text{ Hz to } 10\text{ Hz}$			12		μV_{PP}
		RTI, $f = 1\text{ kHz}$			550		$\text{nV}/\sqrt{\text{Hz}}$
GAIN							
	Gain			0.1		100	V/V
GE	Gain error	$V_O = (V_-) + 0.15\text{ V to } (V_+) - 1\text{ V}$, $R_L = 100\text{ k}\Omega$, $G = 1$			± 0.025	± 0.1	%
		$V_O = (V_-) + 0.3\text{ V to } (V_+) - 1.25\text{ V}$, $R_L = 10\text{ k}\Omega$, $G = 1$			± 0.025	± 0.1	
	Gain error drift ⁽²⁾	$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	$V_O = (V_-) + 0.25\text{ V to } (V_+) - 1\text{ V}$, $R_L = 100\text{ k}\Omega$, $G = 1$		± 1	± 10	ppm/ $^\circ\text{C}$
			$V_O = (V_-) + 0.5\text{ V to } (V_+) - 1.25\text{ V}$, $R_L = 10\text{ k}\Omega$, $G = 1$		± 1	± 10	
	Gain nonlinearity	$V_O = (V_-) + 0.3\text{ V to } (V_+) - 1.25\text{ V}$, $G = 1$			± 0.001	± 0.01	% of FSR
OUTPUT							
	Output voltage	$R_L = 100\text{ k}\Omega$, $G = 1$		$(V_-) + 0.15$		$(V_+) - 1$	V
			$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	$(V_-) + 0.25$		$(V_+) - 1$	
		$R_L = 10\text{ k}\Omega$, $G = 1$		$(V_-) + 0.3$		$(V_+) - 1.25$	
			$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	$(V_-) + 0.5$		$(V_+) - 1.25$	
C_L	Load capacitance	Stable operation			1		nF
I_{SC}	Short-circuit current	Continuous to $V_S / 2$			± 15		mA
FREQUENCY RESPONSE							
BW	Bandwidth, -3 dB	$G = 0.1$			550		kHz
		$G = 1$			50		
SR	Slew rate				0.3		V/ μs
t_S	Settling time	To 0.1%,	$V_O = 10\text{ V-step}$		40		μs
		To 0.01%	$V_O = 10\text{ V-step}$		80		
	Overload recovery	50% input overload			40		μs
POWER SUPPLY							
I_Q	Quiescent current	$V_{IN} = 0\text{ V}$			± 570	± 700	μA
		$T_A = -40^\circ\text{C to } 85^\circ\text{C}$				± 750	

(1) Input common-mode voltage varies with output voltage; see *Typical Characteristics*.

(2) Specified by wafer test.

5.6 Electrical Characteristics $V_S = 5\text{ V}$ Single Supply

at $T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $R_L = 10\text{ k}\Omega$, $V_{REF} = 0\text{ V}$, $V_{CM} = V_S / 2$, and $G = 0.1$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT							
V_{OS}	Offset voltage, V_O	RTI, $V_{CM} = 0\text{ V}$			± 3	± 10	mV
	Offset voltage, V_{O1}	RTI, $V_{CM} = 0\text{ V}$			± 1		mV
	Offset voltage drift	RTI, $T_A = -40^\circ\text{C}$ to 85°C			± 10		$\mu\text{V}/^\circ\text{C}$
PSRR	Power-supply rejection ratio	RTI, $V_S = \pm 1.35\text{ V}$ to $\pm 18\text{ V}$			± 100	± 600	$\mu\text{V}/\text{V}$
V_{CM}	Common-mode voltage ⁽¹⁾	$V_{IN} = 0\text{ V}$		-25		19	V
CMRR	Common-mode voltage rejection	$V_{CM} = -25\text{ V}$ to 19 V , $R_S = 0\ \Omega$		70	80		dB
		$T_A = -40^\circ\text{C}$ to 85°C		64	74		
	Differential input impedance	Non-inverting input			110		k Ω
		Inverting input			91.7		
	Common-mode input impedance				55		k Ω
BIAS CURRENT							
I_B	Bias Current	$V_{CM} = V_S / 2$			± 50		nA
I_{OS}	Offset Current	$V_{CM} = V_S / 2$			± 5		nA
NOISE							
e_N	Voltage noise	RTO, $f_B = 0.1\text{ Hz}$ to 10 Hz			12		μV_{PP}
		RTO, $f = 1\text{ kHz}$			550		$\text{nV}/\sqrt{\text{Hz}}$
GAIN							
	Gain			0.1		100	V/V
GE	Gain error	$V_O = 0.15\text{ V}$ to 4 V , $R_L = 100\text{ k}\Omega$			± 0.025	± 0.1	%
		$V_O = 0.3\text{ V}$ to 3.75 V , $R_L = 10\text{ k}\Omega$			± 0.025	± 0.1	
	Gain error drift ⁽²⁾	$T_A = -40^\circ\text{C}$ to 85°C	$V_O = 0.25\text{ V}$ to 4 V , $R_L = 100\text{ k}\Omega$		± 1	± 10	ppm/ $^\circ\text{C}$
			$V_O = 0.5\text{ V}$ to 3.75 V , $R_L = 10\text{ k}\Omega$		± 1	± 10	
	Gain nonlinearity	$V_O = 0.3\text{ V}$ to 3.75 V			± 0.001	± 0.01	% of FSR
OUTPUT							
	Output voltage	$R_L = 100\text{ k}\Omega$		0.15		4	V
			$T_A = -40^\circ\text{C}$ to 85°C	0.25		4	
		$R_L = 10\text{ k}\Omega$		0.3		3.75	
			$T_A = -40^\circ\text{C}$ to 85°C	0.5		3.75	
C_L	Load capacitance	Stable operation			1		nF
I_{SC}	Short-circuit current	Continuous to $V_S / 2$			± 15		mA
FREQUENCY RESPONSE							
BW	Bandwidth, -3 dB	$G = 0.1$			550		kHz
		$G = 1$			50		
SR	Slew rate				0.3		V/ μs
t_s	Settling time	To 0.1%,	$V_O = 10\text{ V-step}$		40		μs
		To 0.01%	$V_O = 10\text{ V-step}$		80		
	Overload recovery	50% input overload			40		μs
POWER SUPPLY							
I_Q	Quiescent current	$V_{IN} = 0\text{ V}$			± 570	± 700	μA
		$T_A = -40^\circ\text{C}$ to 85°C				± 750	

(1) Input common-mode voltage varies with output voltage; see *Typical Characteristics*.

(2) Specified by wafer test.

5.7 Amplifier A1, A2 Performance

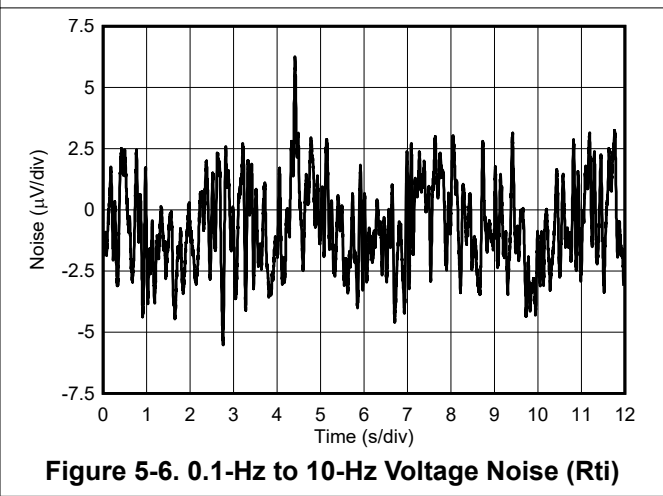
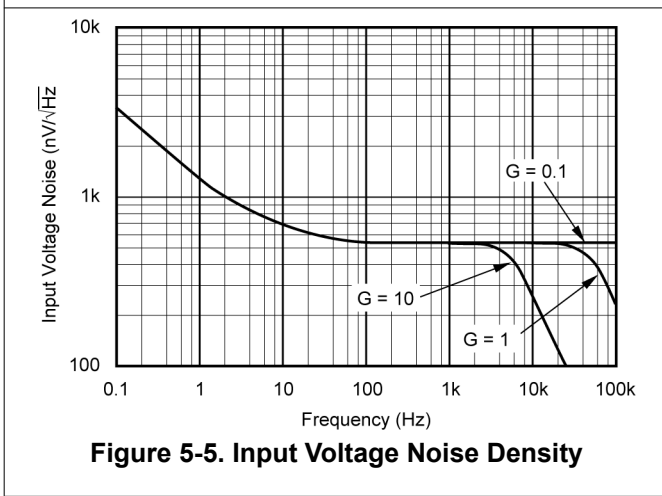
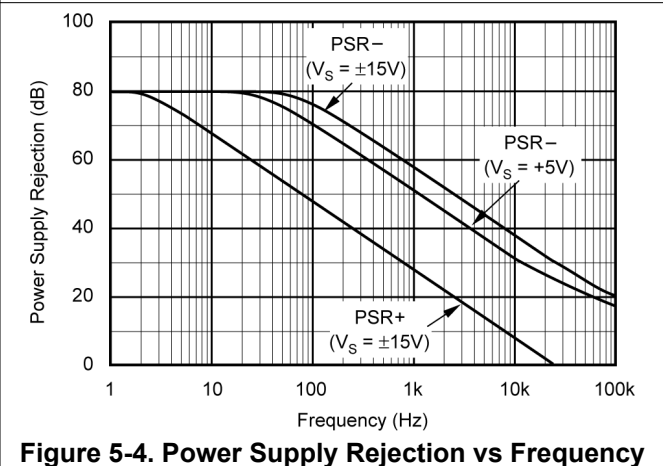
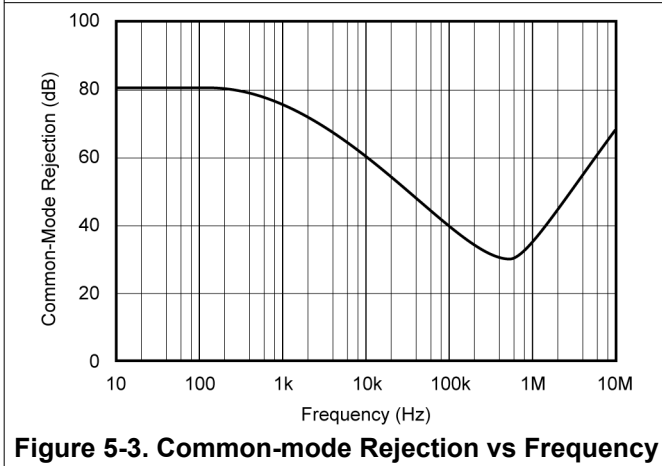
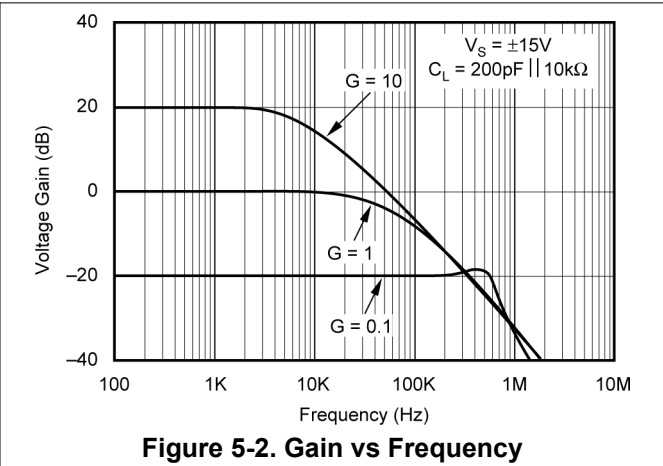
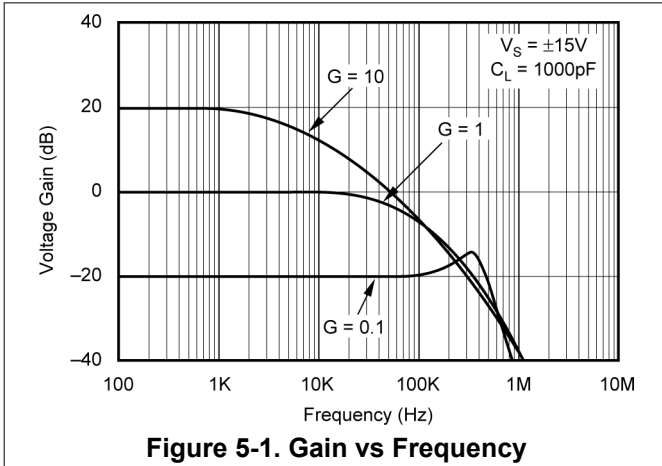
at $T_A = 25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$, $V_{REF} = 0\text{ V}$, $V_{CM} = V_S / 2$, and $G = 0.1$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT							
V_{OS}	Offset voltage, V_O	RTI, $V_S = \pm 15\text{ V}$, $V_{CM} = V_O = 0\text{ V}$			± 0.5		mV
	Offset voltage drift	RTI, $T_A = -40^\circ\text{C}$ to 85°C			± 1		$\mu\text{V}/^\circ\text{C}$
V_{CM}	Common-mode voltage ⁽¹⁾	$V_{IN} = V_O = 0\text{ V}$			V_{S-} to $(V_{S+}) - 1$		V
CMRR	Common-mode voltage rejection	$V_{CM} = V_{S-}$ to $(V_{S+}) - 1$			90		dB
GAIN							
A_{OL}	Open Loop Gain				110		dB
BIAS CURRENT							
I_B	Bias Current				± 50		nA
I_{OS}	Offset Current				± 5		nA
OUTPUT							
	Resistor at V_{O1}	Initial			10		k Ω
	Error at V_{O1}				± 1		%
	Error drift at V_{O1}				± 100		ppm/ $^\circ\text{C}$

(1) Input common-mode voltage varies with output voltage; see *Typical Characteristics*.

5.8 Typical Performance Curves

At $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, $G = 0.1$, $R_L = 10\text{ k}\Omega$ connected to ground and Ref pin connected to ground, unless otherwise noted.



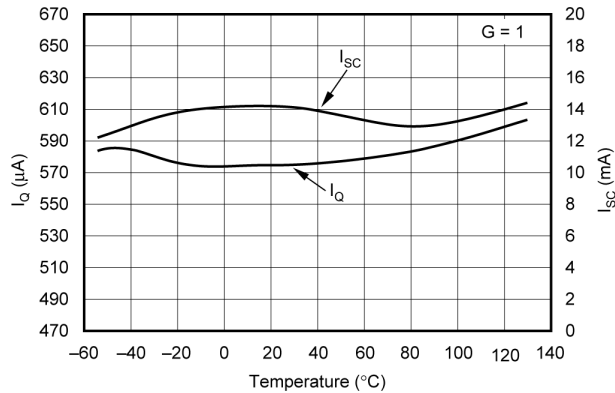


Figure 5-7. Quiescent Current and Short-circuit Current vs Temperature

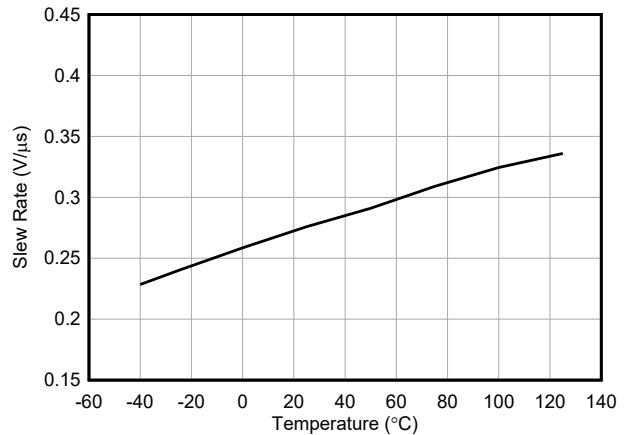


Figure 5-8. Slew Rate vs Temperature

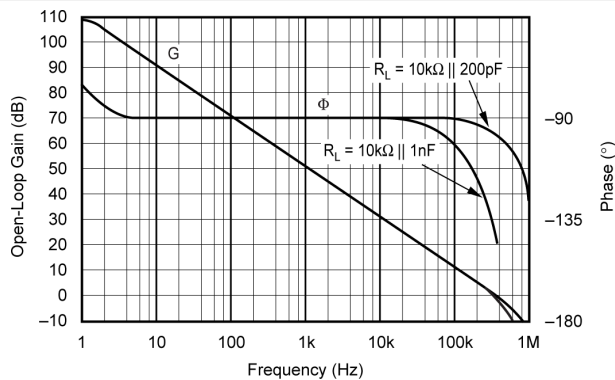


Figure 5-9. Gain and Phase vs Frequency Op Amp A1 and A2

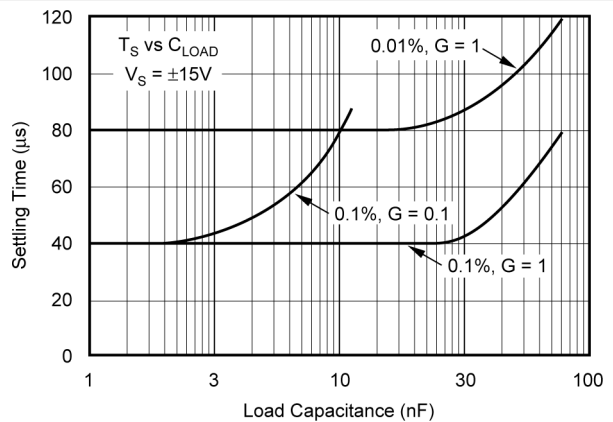


Figure 5-10. Settling Time vs Load Capacitance

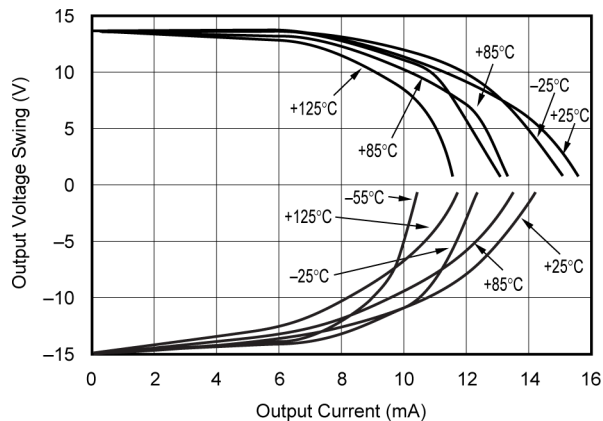


Figure 5-11. Maximum Output Voltage Swing vs Output Current

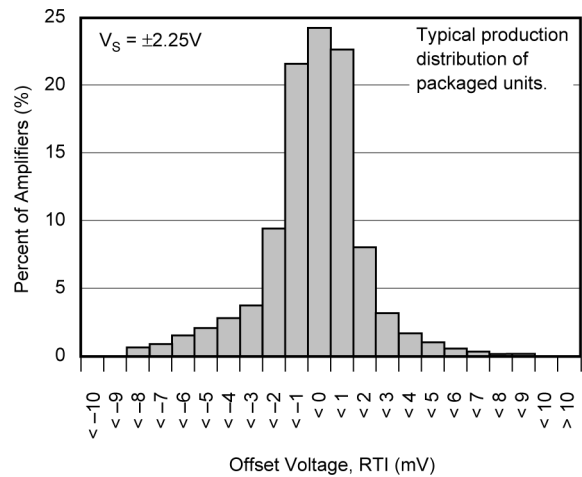


Figure 5-12. Offset Voltage Production Distribution

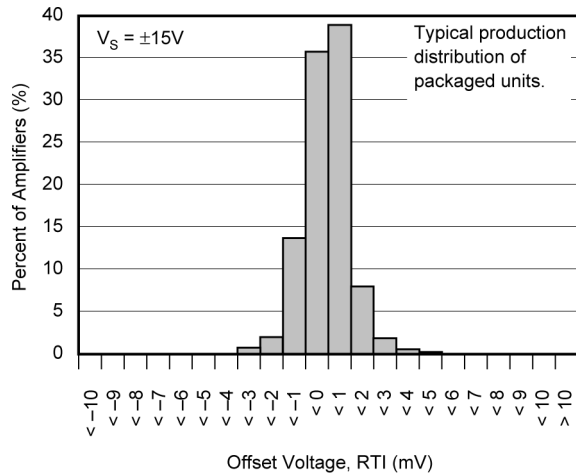


Figure 5-13. Offset Voltage Production Distribution

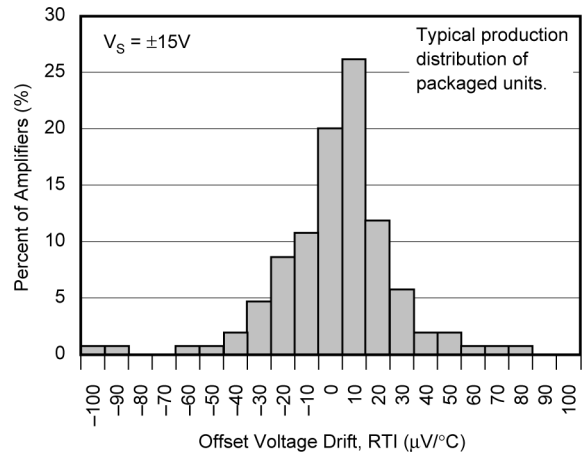


Figure 5-14. Offset Voltage Drift Production Distribution

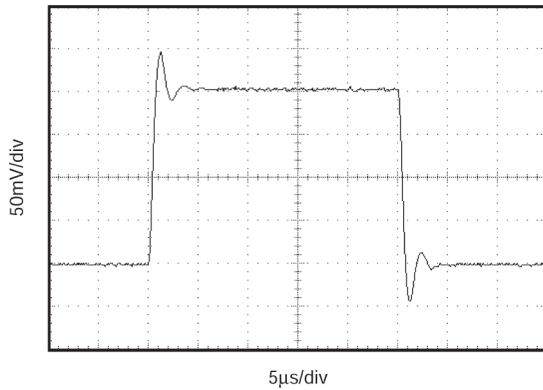


Figure 5-15. Small-signal Step Response (G = 0.1, RL = 10 kΩ, CL = 200 pF)

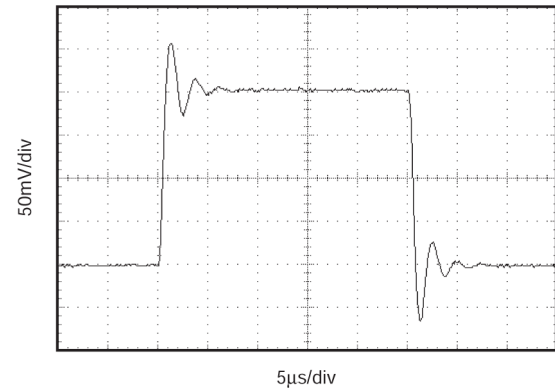


Figure 5-16. Small-signal Step Response (G = 0.1, CL = 1000 pF)

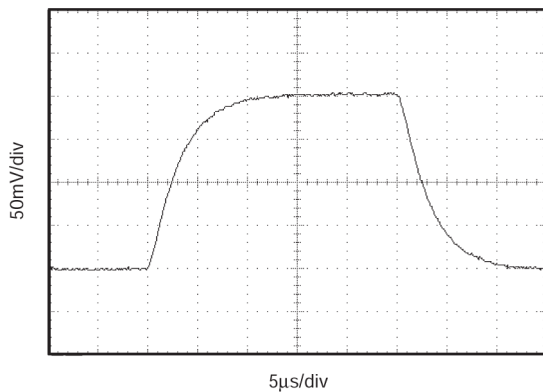


Figure 5-17. Small-signal Step Response (G = 1, CL = 1000 pF)

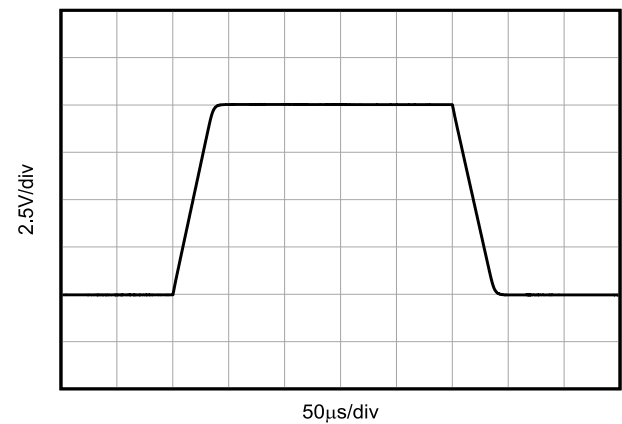


Figure 5-18. Large-signal Step Response (G = 1, RL = 10 kΩ, CL = 200pF)

6 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

6.1 Application Information

The INA146 is a programmable gain difference amplifier consisting of a gain of 0.1 difference amplifier and a programmable-gain output buffer stage. Basic circuit connections are shown in [Figure 6-1](#). Power supply bypass capacitors must be connected close to pins 4 and 7, as shown. The amplifier is programmable in the range of $G = 0.1$ to $G = 50$ with two external resistors.

The output of A1 is connected to the noninverting input of A2 through a 10-k Ω resistor which is trimmed to $\pm 1\%$ absolute accuracy. The A2 input is available for applications such as a filter or a precision current source. See application figures for examples.

6.1.1 Operating Voltage

The INA146 is fully specified for supply voltages from ± 2.25 V to ± 18 V with key parameters specified over the temperature range -40°C to 85°C . The INA146 can be operated with single or dual supplies with excellent performance. Parameters that vary significantly with operating voltage, load conditions or temperature are shown in the typical performance curves.

6.1.2 Setting the Gain

The gain of the INA146 is set by using two external resistors, R_{G1} and R_{G2} , according to the equation:

$$G = 0.1 \times (1 + R_{G2}/R_{G1})$$

For a total gain of 0.1, A2 is connected as a buffer amplifier with no R_{G1} . A feedback resistor, $R_{G2} = 10$ k Ω , must be used in the buffer connection. This provides bias current cancellation (in combination with internal R_5) to assure specified offset voltage performance. Commonly used values are shown in the table of [Figure 6-1](#). Resistor values for other gains must be chosen to provide a 10-k Ω parallel resistance.

6.1.3 Common-mode Range

The 10:1 input resistor ratio of the INA146 provides an input common-mode range that can extend well beyond the power supply rails. Exact range depends on the power supply voltage and the voltage applied to the Ref terminal (pin 1). For proper operation, the voltage at the non-inverting input of A1 (an internal node) must be within the linear operating range. The voltage is determined by the simple 10:1 voltage divider between pin 3 and pin 1. This voltage must be between V_- and $(V_+) - 1$ V.

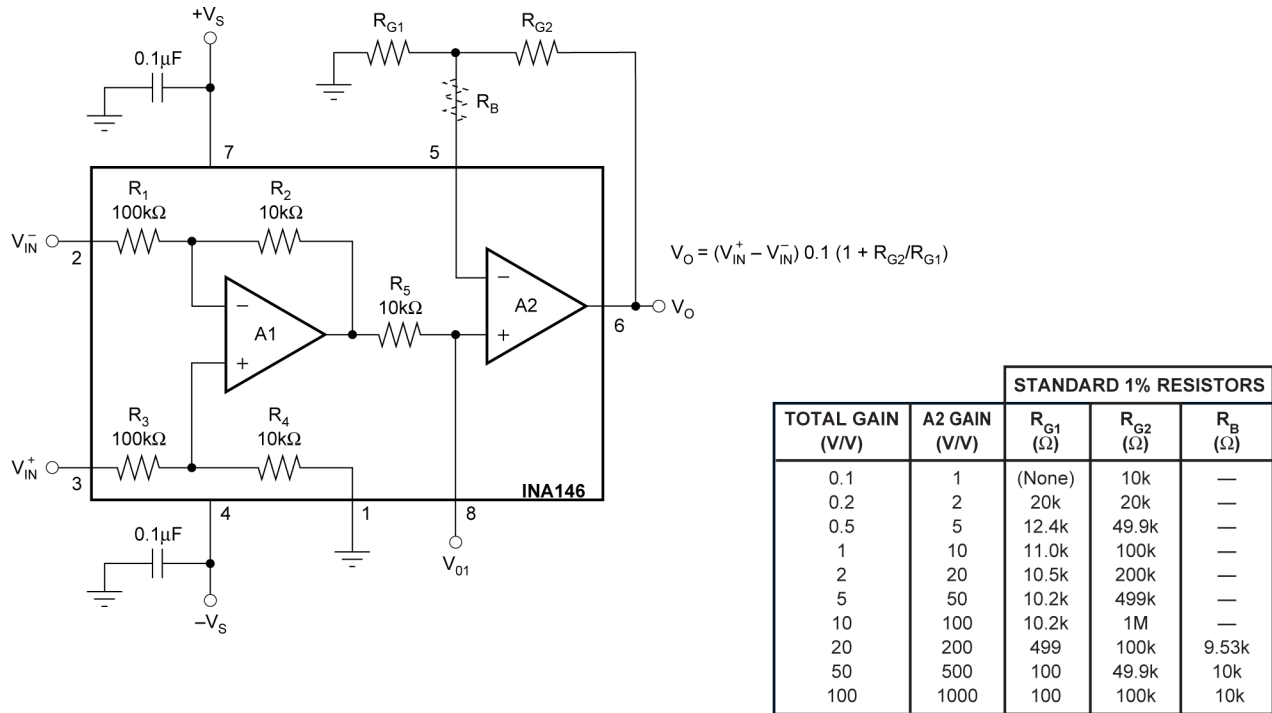


Figure 6-1. Basic Circuit Connections

6.1.4 Offset Trim

The INA146 is laser-trimmed for low offset voltage and drift. Most applications require no external offset adjustment. Figure 6-2 shows an optional circuit for trimming the offset voltage. A voltage applied to the Ref terminal is summed with the output signal. This feature can be used to null offset voltage. To maintain good common-mode rejection, the source impedance of a signal applied to the Ref terminal must be less than 10 Ω and a resistor added to the positive input terminal must be 10 times that, or 100 Ω. Alternatively, the trim voltage can be buffered with an operational amplifier such as the OPA277.

6.1.5 Input Impedance

The input impedance of the INA146 is determined by the input resistor network and is approximately 100 kΩ. The source impedance at the two input terminals must be nearly equal to maintain good common-mode rejection. A 12-Ω mismatch in impedance between the two inputs causes the typical common-mode rejection to be degraded to approximately 72 dB. Figure 6-7 shows a common application measuring power supply current through a shunt resistor. The source impedance of the shunt resistor, RS, is balanced by an equal compensation resistor, RC.

Source impedances greater than 800 Ω are not recommended, even if the source impedances are perfectly matched. Internal resistors are laser trimmed for accurate ratios, not to absolute values. Adding equal resistors greater than 800 Ω can cause a mismatch in the total resistor ratios, degrading CMR.

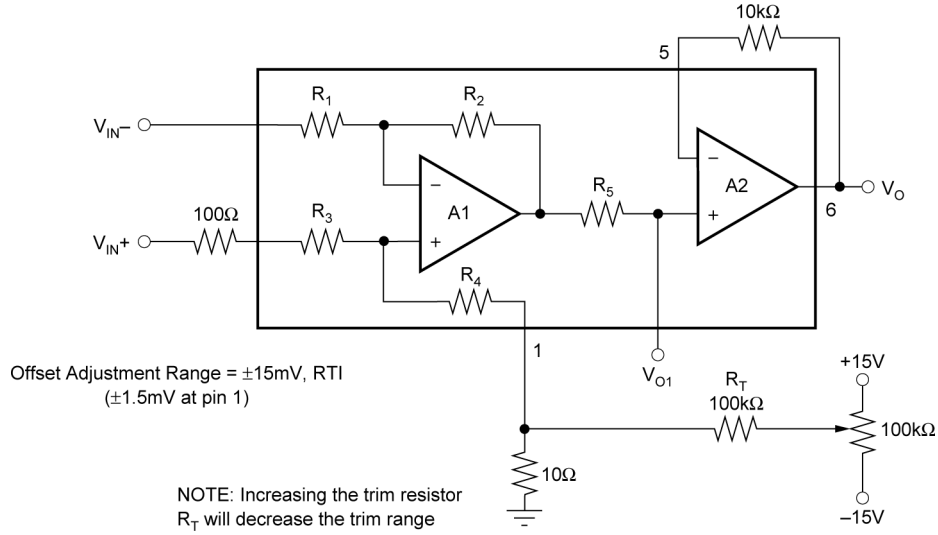


Figure 6-2. Optional Offset Trim Circuit

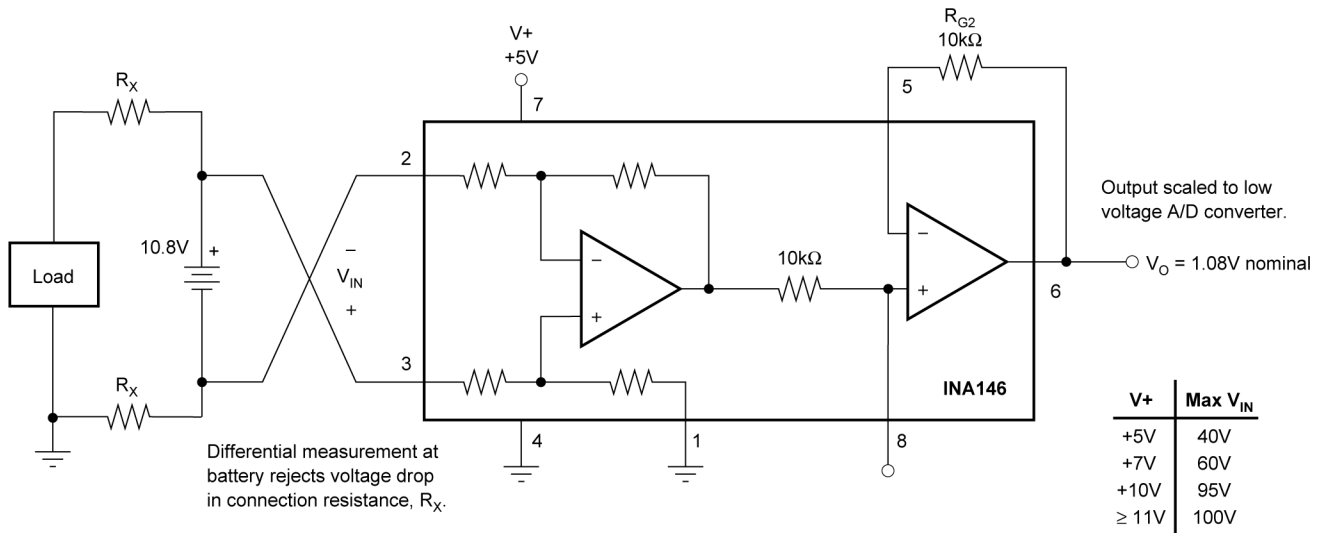


Figure 6-3. Measuring Voltages Greater Than Supply Voltage

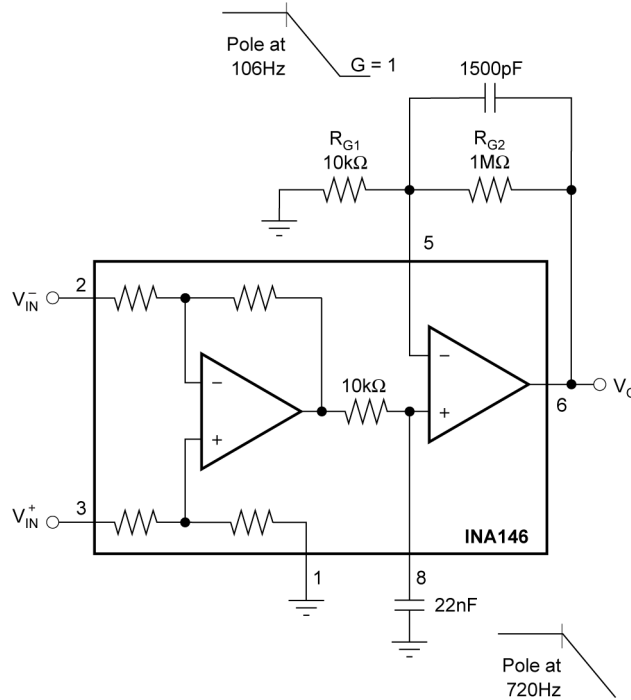


Figure 6-4. Noise Filtering

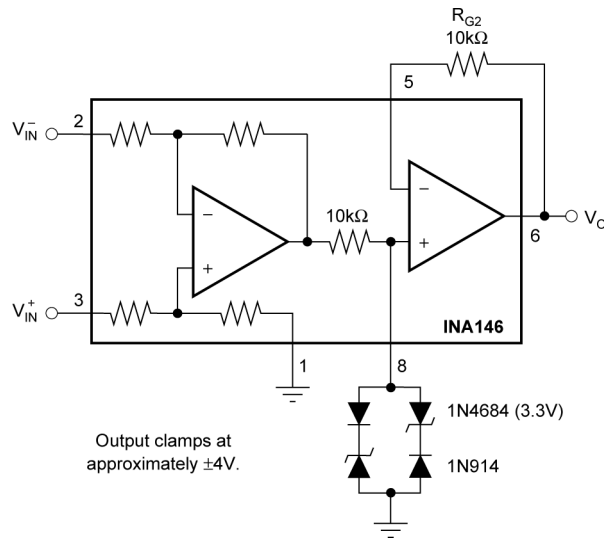
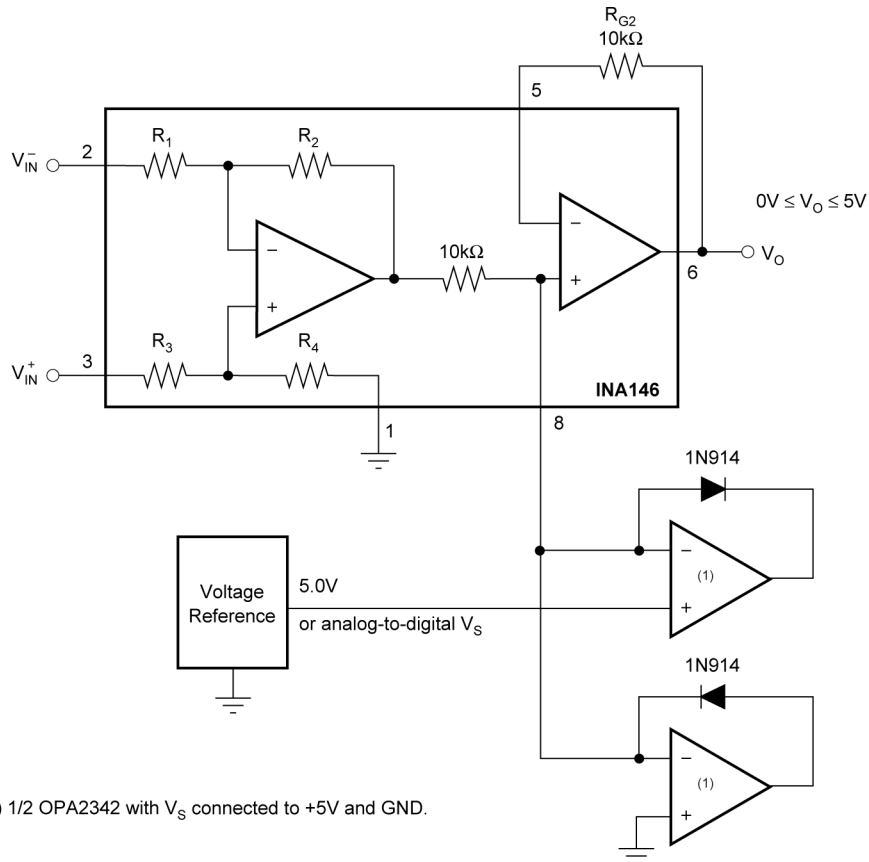
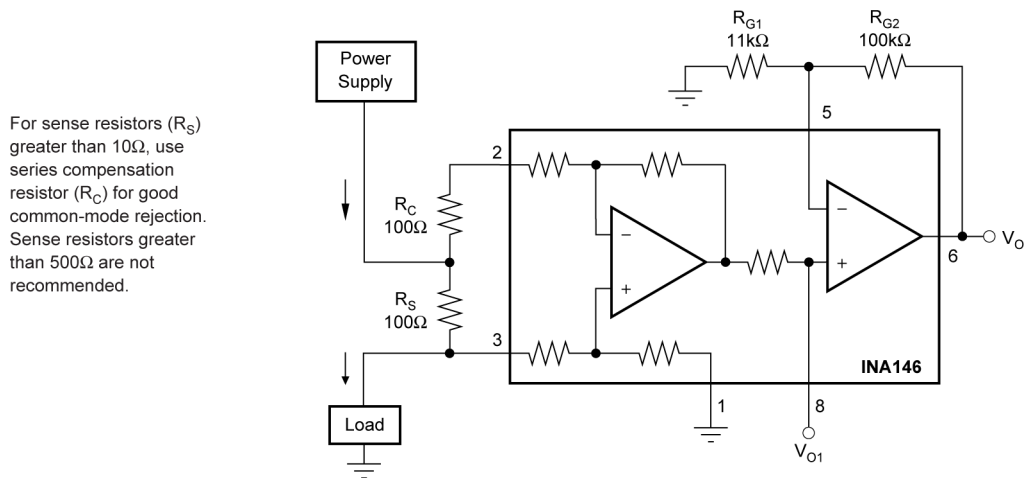


Figure 6-5. Output Clamp



NOTE: (1) 1/2 OPA2342 with V_S connected to +5V and GND.

Figure 6-6. Precision Clamp



For sense resistors (R_S) greater than 10Ω , use series compensation resistor (R_C) for good common-mode rejection. Sense resistors greater than 500Ω are not recommended.

Figure 6-7. Current Monitor, $G = 1$

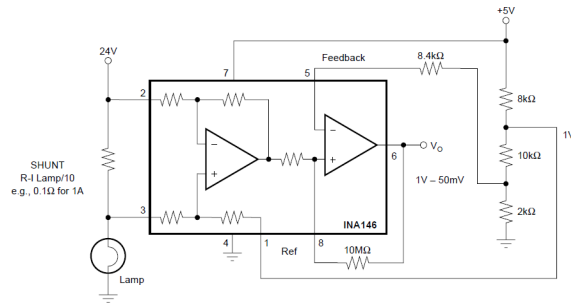


Figure 6-8. Comparator Output With Optional Hysteresis Application to Sense Lamp Burn-Out

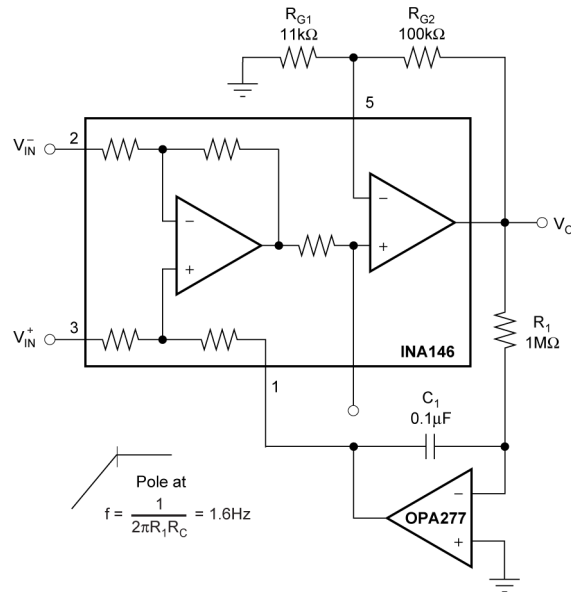


Figure 6-9. AC Coupling (DC Restoration)

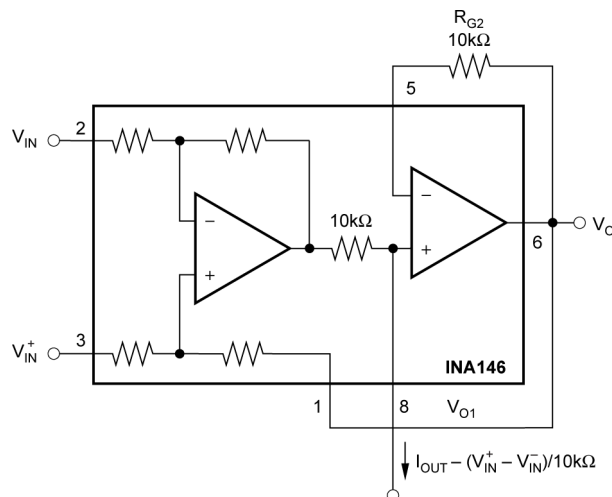


Figure 6-10. Precision Current Source

7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

7.1 Third-Party Products Disclaimer

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7.2 Documentation Support

7.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [Comprehensive Error Calculation for Instrumentation Amplifiers](#), application note
- Texas Instruments, [High-Voltage Signal Conditioning for Low Voltage ADCs](#), application note
- Texas Instruments, [Analog Engineer's Calculator](#), application

7.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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7.5 Trademarks

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7.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (September 1999) to Revision A (October 2023)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Changed pin 7 from V+ to V _{S+} and pin 4 from V- to V _{S-}	3
• Added V _{REF} = 0 V, V _{CM} = V _S / 2 "unless otherwise noted" conditions in <i>Electrical Characteristics</i> and <i>Typical Characteristics</i> for clarity.....	5
• Changed from Offset Voltage vs Power Supply to Power-supply rejection ratio for more clarity.....	5
• Change test condition V _{CM} formula for more clarity.....	5
• Added test condition "TA = –40°C to 85°C" for "Gain error vs temperature" in <i>Electrical Characteristics</i> and renamed to "Gain drift" for clarity.....	5
• Added test condition "TA = –40°C to 85°C" for Output over Temperature in <i>Electrical Characteristics</i>	5
• Added test condition "Continuous to V _S / 2" short-circuit current specification in <i>Electrical Characteristics</i> for clarity.....	5
• Deleted redundant voltage range, operating temperature range, and specification temperature range specifications from <i>Electrical Characteristics</i>	5
• Added V _{REF} = 0 V, V _{CM} = V _S / 2, to "unless otherwise noted" conditions in <i>Electrical Characteristics</i> and <i>Typical Characteristics</i> for clarity.....	6
• Changed from Offset Voltage vs Power Supply to Power-supply rejection ratio for more clarity.....	6
• Added test condition "TA = –40°C to 85°C" for "Gain error vs temperature" in <i>Electrical Characteristics</i> and renamed to "Gain drift" for clarity.....	6
• Added test condition "TA = –40°C to 85°C" to "Output voltage" in <i>Electrical Characteristics</i>	6
• Added test condition "Continuous to V _S / 2" short-circuit current specification in <i>Electrical Characteristics</i> for clarity.....	6
• Deleted redundant voltage range, operating temperature range, and specification temperature range specifications from <i>Electrical Characteristics</i>	6
• Added V _{REF} = 0 V, V _{CM} = V _S / 2 to "unless otherwise noted" conditions in <i>Electrical Characteristics</i> and <i>Typical Characteristics</i> for clarity.....	7

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA146UA	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	INA 146UA	
INA146UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	INA 146UA	Samples
INA146UAE4	NRND	SOIC	D	8	75	TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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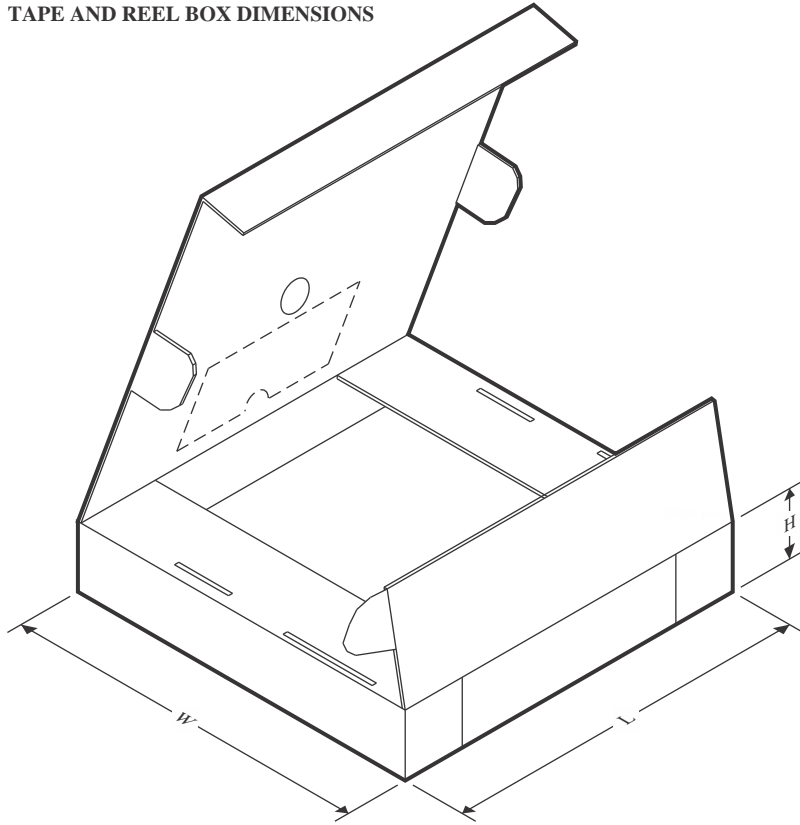
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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA146UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA146UA/2K5	SOIC	D	8	2500	367.0	367.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
INA146UA	D	SOIC	8	75	506.6	8	3940	4.32



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
 EXPOSED METAL SHOWN
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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