SN75ALS173 Quadruple Differential Line Receiver

1 Features

- Meets or exceeds the requirements of ANSI EIA/TIA-422-B, EIA/TIA-423-B, and RS-485
- Meets or exceeds the requirements of ITU recommendations V.10, V.11, X.26, and X.27
- Designed for multipoint bus transmission on long bus lines in noisy environments
- 3-State Outputs
- Common-mode input voltage range of –12 V to 12 V
- Input sensitivity: ±200 mV
- Input hysteresis: 50 mV typical
- High input impedance: 12 kΩ minimum
- Operates from single 5-V supply
- Low supply-current requirement 27 mA maximum

2 Applications

- Motor drives
- Factory automation and control

3 Description

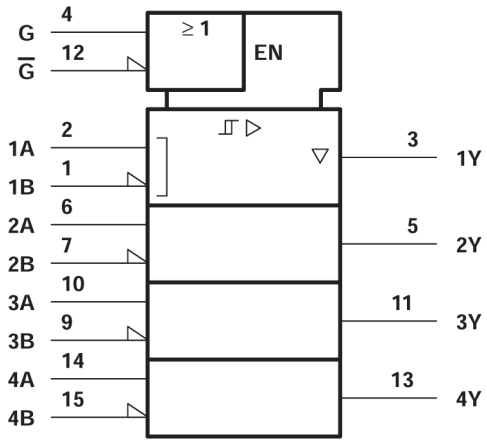
The SN75ALS173 is a monolithic quadruple differential line receiver with 3-state outputs. It is designed to meet the requirements of ANSI Standards EIA/TIA-422-B, EIA/TIA-423-B, RS-485, and several ITU recommendations. Advanced low-power Schottky technology provides high speed without the usual power penalty. The four receivers have an ORed pair of enables in common. Either G high or $\overline{G}$ low enables all of the receivers. The device features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ±200 mV over a common-mode input voltage range of –12 V to 12 V.

The SN75ALS173 is characterized for operation from 0°C to 70°C.

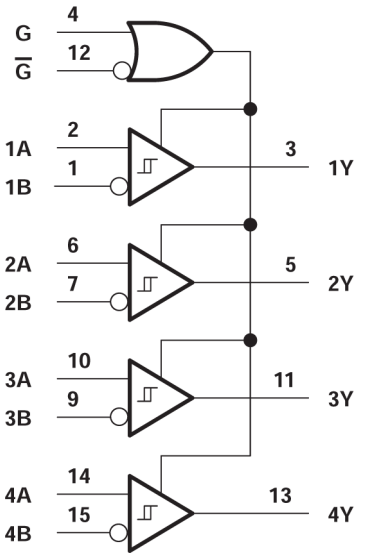
Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
SN75ALS173	N (PDIP, 16)	19.3 mm × 9.4 mm
	NS (SOP, 16)	10.2 mm × 7.8 mm

(1) For more Information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Logic Symbol†

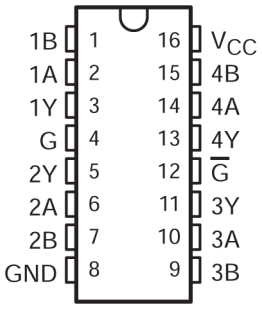


Logic Diagram (Positive Logic)

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Table of Contents

4 Pin Configuration and Functions



A. The NS package is only available left-end taped and reeled (order device SN75ALS173 NSLE).

Figure 4-1. N or NS Package (Top View)

Table 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
1B	1	I	Channel 1 Differential Receiver Inverting Input
1A	2	I	Channel 1 Differential Receiver Non-Inverting Input
1Y	3	O	Channel 1 Single Ended Output
G	4	I	Active High Enable
2Y	5	O	Channel 2 Single Ended Output
2A	6	I	Channel 2 Differential Receiver Non-Inverting Input
2B	7	I	Channel 2 Differential Receiver Inverting Input
GND	8	GND	Device GND
3B	9	I	Channel 3 Differential Receiver Inverting Input
3A	10	I	Channel 3 Differential Receiver Non-Inverting Input
3Y	11	O	Channel 3 Single Ended Output
$\overline{G}$	12	I	Active Low Enable
4Y	13	O	Channel 4 Single Ended Output
4A	14	I	Channel 4 Differential Receiver Non-Inverting Input
4B	15	I	Channel 4 Differential Receiver Inverting Input
V_{CC}	16	PWR	Device VCC (4.75 V to 5.25 V)

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage, (see (2))		7	V
V_I	Input voltage, (A or B inputs)		±14	V
V_{ID}	Differential input voltage, (see (3))		±14	V
V_I	Enable input voltage		7	V
I_{OL}	Low-level output current		50	mA
	Continuous total dissipation	See Dissipation Rating Table		
T_A	Operating free-air temperature range	0	70	°C
T_{stg}	Storage temperature range	–65	150	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential input voltage, are with respect to network ground terminal.
(3) Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

5.2 Dissipation Rating Table

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
N	1150 mW	9.2 mW/°C	736 mW
NS	625 mW	5.0 mW/°C	400 mW

5.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Common-mode input voltage, V_{IC}				±12	V
Differential input voltage, V_{ID}				±12	V
High-level input voltage, V_{IH}	G, $\overline{G}$	2			V
Low-level input voltage, V_{IL}	G, $\overline{G}$			0.8	V
High-level output current, I_{OH}				–400	µA
Low-level output current, I_{OL}				8	mA
Operating free-air temperature, T_A		0		70	°C

5.4 Thermal Information

THERMAL METRIC(1)		SN75ALS173		UNIT
		N (PDIP)	NS (SOP)	
		16 Pins	16 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	60.6	88.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	48.1	46.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	40.6	50.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	27.5	13.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	40.3	50.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.5 Electrical Characteristics

over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted) (see Note 3)

PARAMETER			TEST CONDITIONS			MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage							200	mV
V_{IT-}	Negative-going input threshold voltage						-200(2)		mV
V_{hys}	Hysteresis voltage (V_{IT+} - V_{IT-})						50		mV
V_{IK}	Input clamp voltage	G, $\overline{G}$	I_I = -18 mA					-1.5	V
V_{OH}	High-level output voltage		V_{ID} = 200 mV,	I_{OH} = -400 µA,	See Figure 6-1	2.7			v
V_{OL}	Low-level output voltage		V_{ID} = -200 mV,	I_{OL} = 8 mA,	See Figure 6-1			0.45	v
I_{OZ}	High-impedance-state output current		V_O = 0.4 V to 2.4 V					-20	µA
I_I	Line input current		Other input at 0 V		V_I = 12 V			1	mA
					V_I = -7 V			-0.8	
I_{IH}	High-level input current	G, $\overline{G}$	V_{IH} = 2.7 V					20	µA
I_{IL}	Low-level input current	G, $\overline{G}$	V_{IL} = 0.4 V					-100	µA
r_i	Input resistance						12		kΩ
I_{OS}	Short-circuit output current		See Note 4				-15	-85	mA
I_{CC}	Supply current (total package)		No load,	Outputs enabled			16	24	mA
			No load,	Outputs disabled			18	27	

(1) All typical values are at V_{CC} = 5 V and T_A = 25°C.
(2) The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold voltage levels only.
(3) Refer to ANSI Standard RS-485 for exact conditions.
(4) The duration of the short circuit should not cause the maximum package power dissipation to be exceeded.

5.6 Switching Characteristics

V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high- to low-level output	V_{ID} = –2.5 V to 2.5 V, See Figure 6-2	9	18	27	ns
t_{PLH}	Propagation delay time, low- to high-level output		9	18	27	ns
t_{PZH}	Output enable time to high level	See Figure 6-3	4	12	18	ns
t_{PZL}	Output enable time to low level	See Figure 6-4	6	13	21	ns
t_{PHZ}	Output disable time from high level	See Figure 6-3	10	21	27	ns
t_{PLZ}	Output disable time from low level	See Figure 6-4	8	15	25	ns

6 Parameter Measurement Information

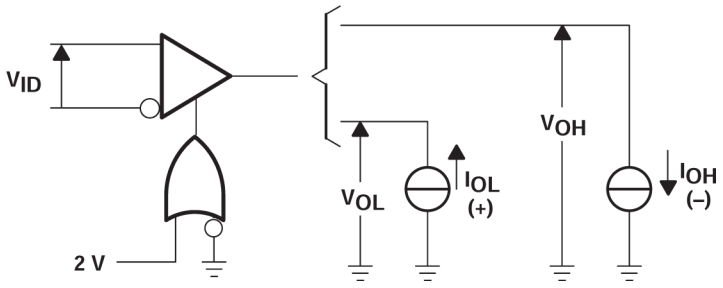


Figure 6-1. V_{OH}, V_{OL}

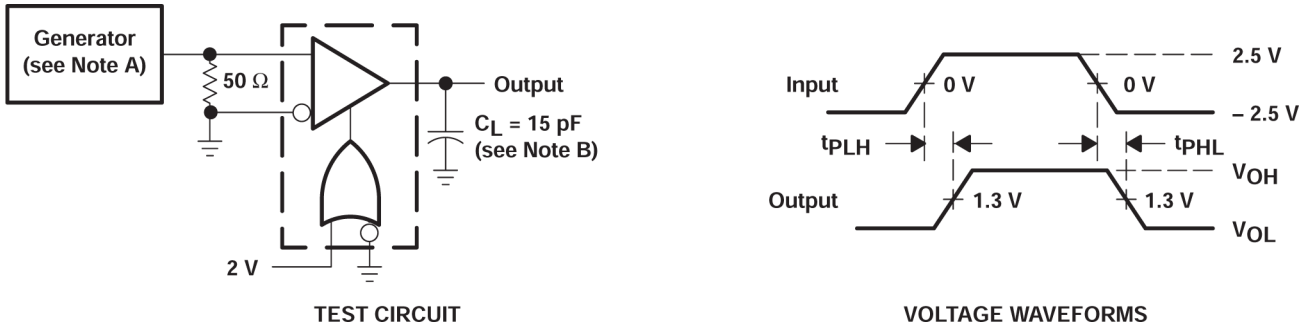
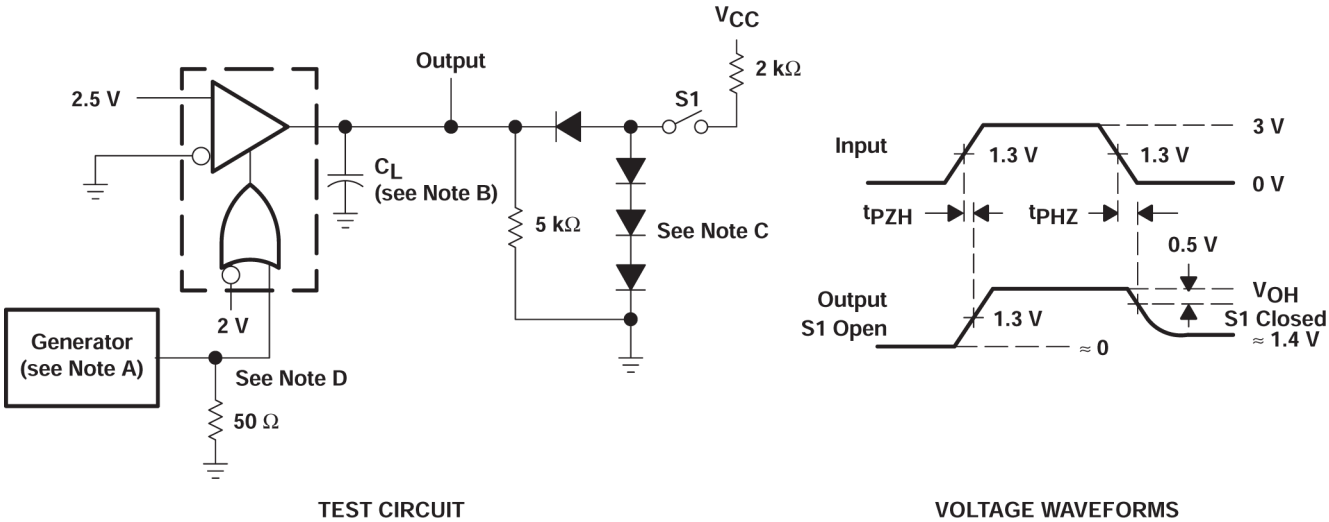
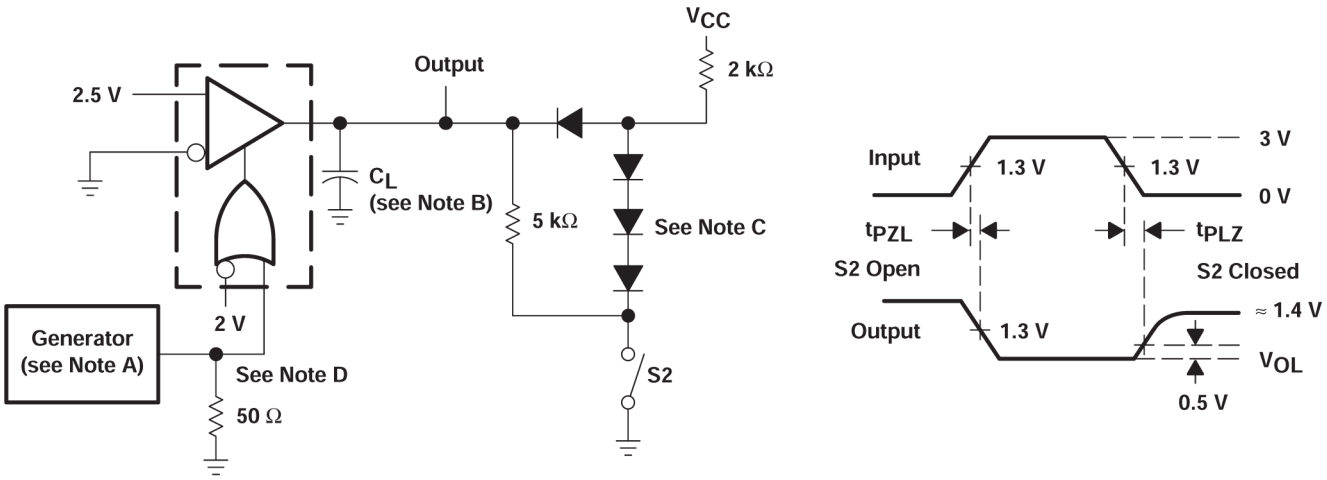


Figure 6-2. Test Circuit and Voltage Waveforms



A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r \le 6$ ns, $t_f \le 6$ ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.
D. To test the active-low enable $\overline{G}$, ground G and apply an inverted input waveform to $\overline{G}$.

Figure 6-3. Test Circuit and Voltage Waveforms



TEST CIRCUIT VOLTAGE WAVEFORMS

A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r \le 6$ ns, $t_f \le 6$ ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.
D. To test the active-low enable $\overline{G}$, ground G and apply an inverted input waveform to $\overline{G}$.

Figure 6-4. Test Circuit and Voltage Waveforms

7 Detailed Description

7.1 Device Functional Modes

Table 7-1. Function Table (Each Receiver)

DIFFERENTIAL A - B	ENABLES(1)		OUTPUT Y
	G	G	
$V_{ID} \geq 0.2$ V	H	X	H
	X	L	H
-0.2 V < V_{ID} < 0.2 V	H	X	?
	X	L	?
$V_{ID} \leq -0.2$ V	H	X	L
	X	L	L
X	L	H	Z
Open Circuit	H	X	H
	X	L	H

(1) H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

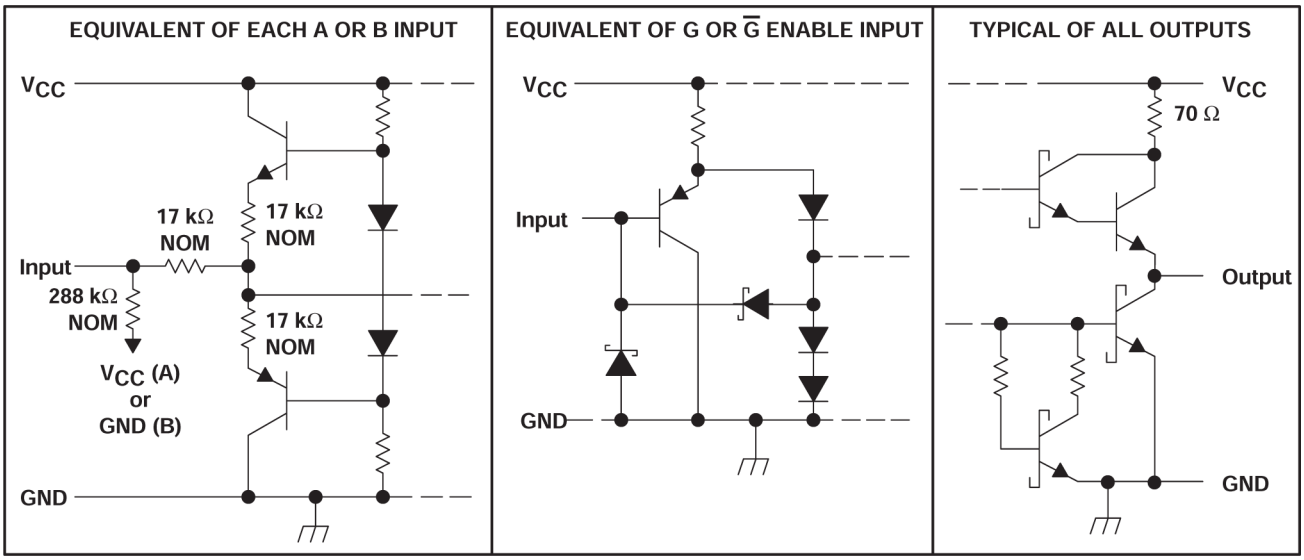


Figure 7-1. Schematics of Inputs and Outputs

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (May 1995) to Revision D (October 2023)	Page
• Changed the numbering format for tables, figures, and cross-references throughout the document	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75ALS173NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS173	Samples
SN75ALS173NSRG4	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS173	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

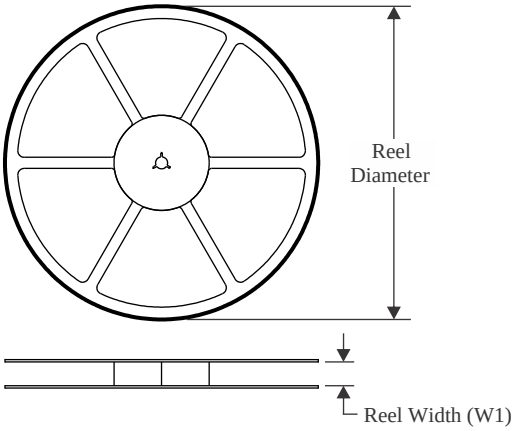
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

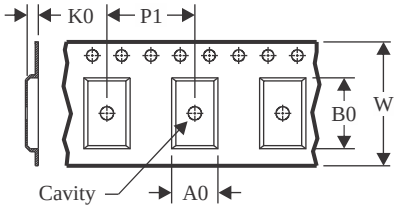
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

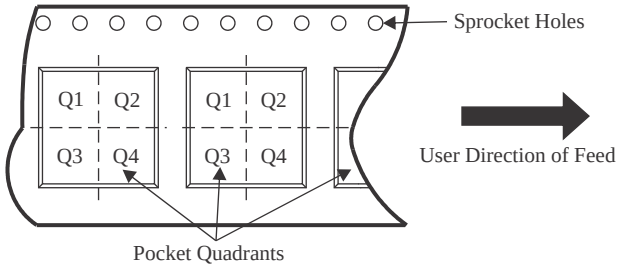


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

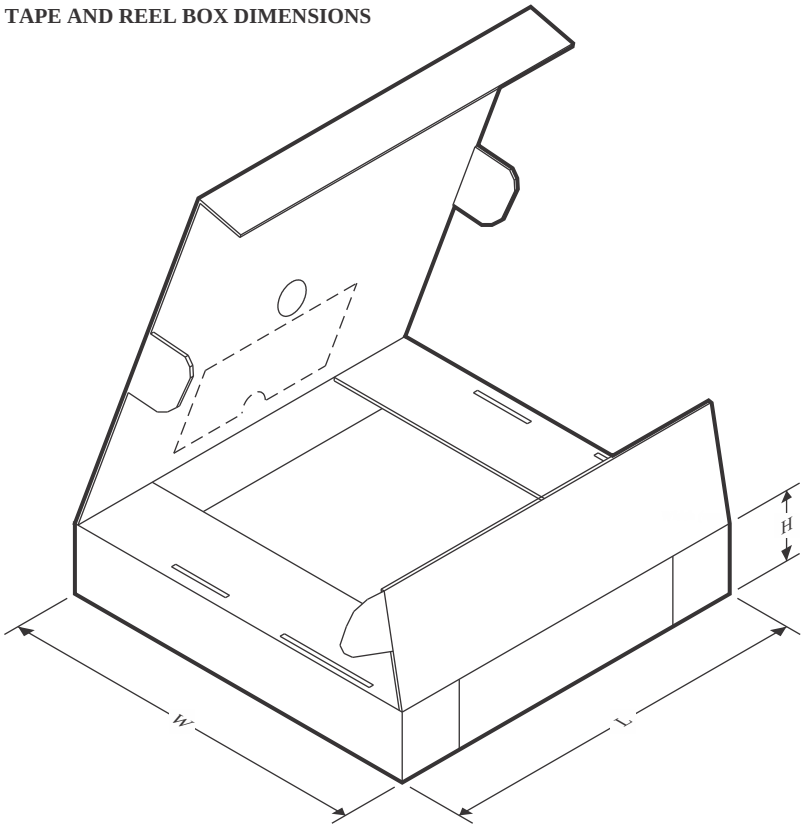
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

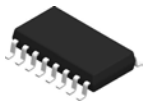
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75ALS173NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75ALS173NSR	SO	NS	16	2000	367.0	367.0	38.0

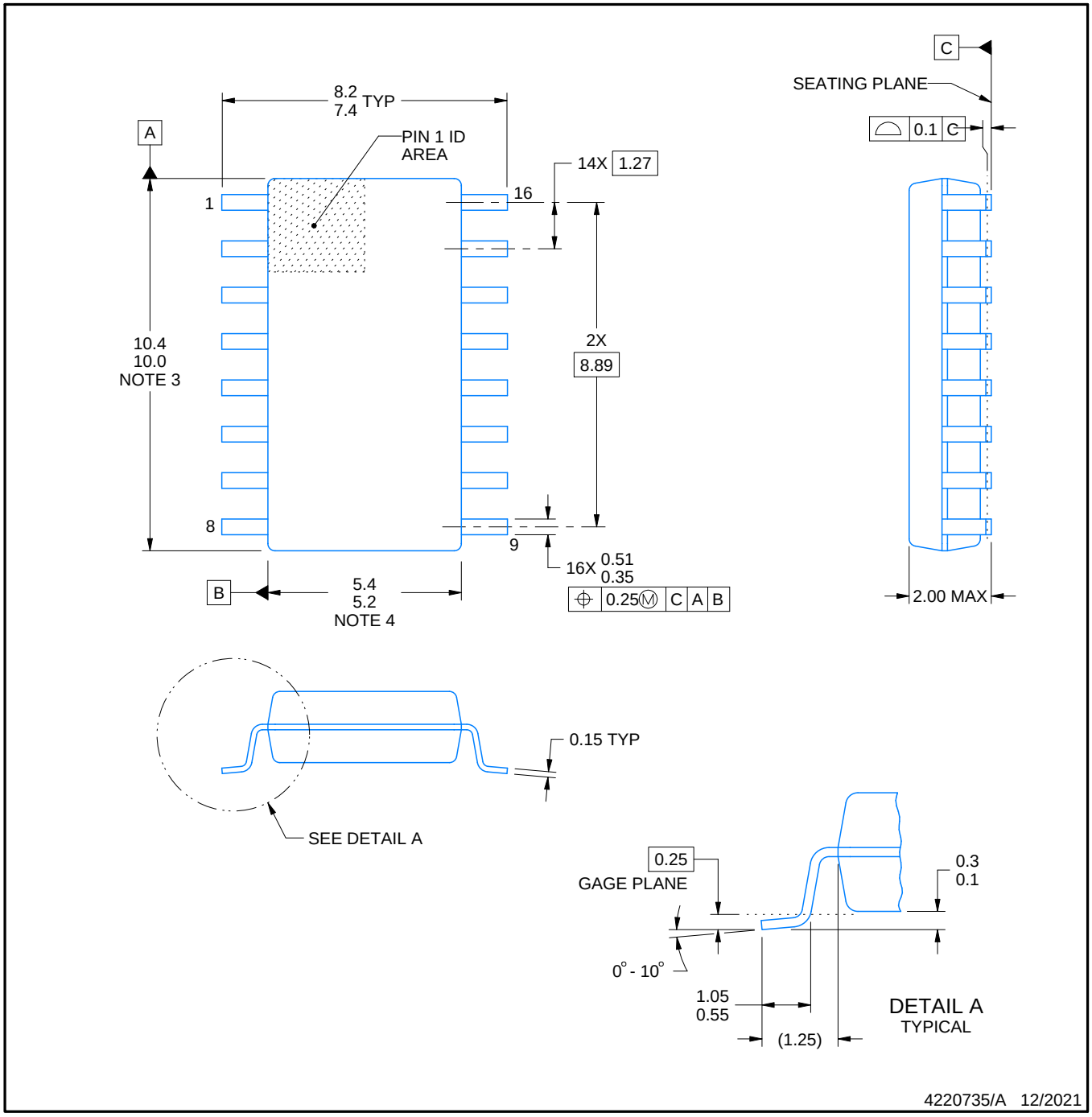


PACKAGE OUTLINE

NS0016A

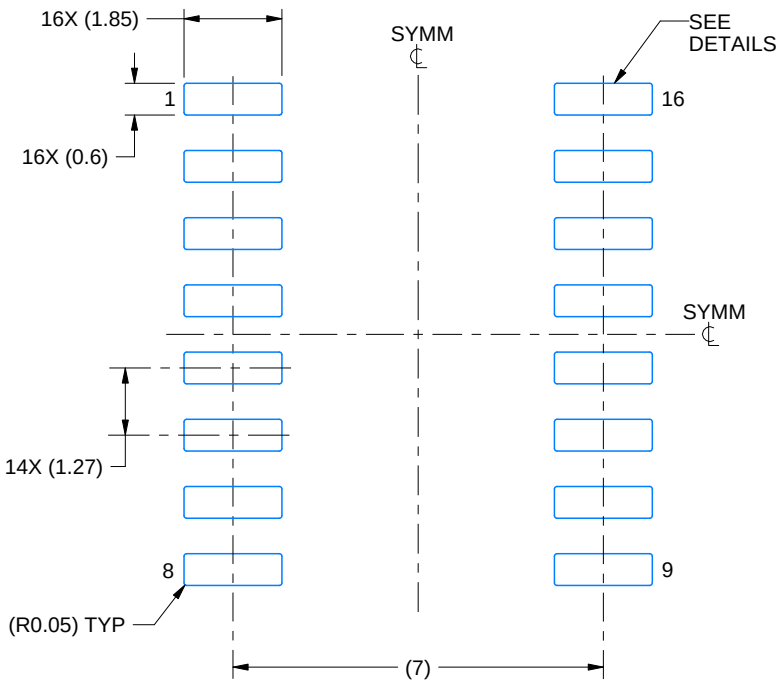
SOP - 2.00 mm max height

SOP

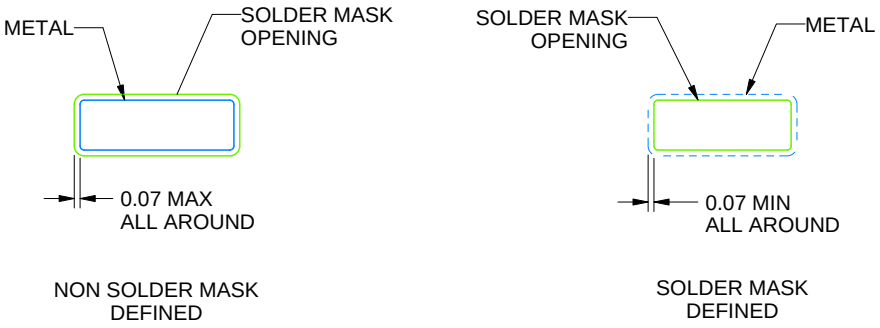


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK
DEFINED

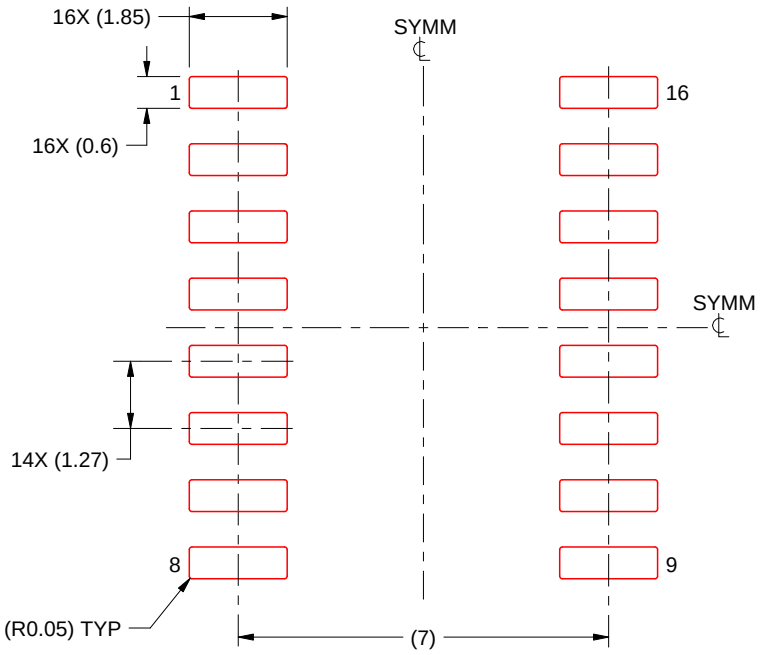
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

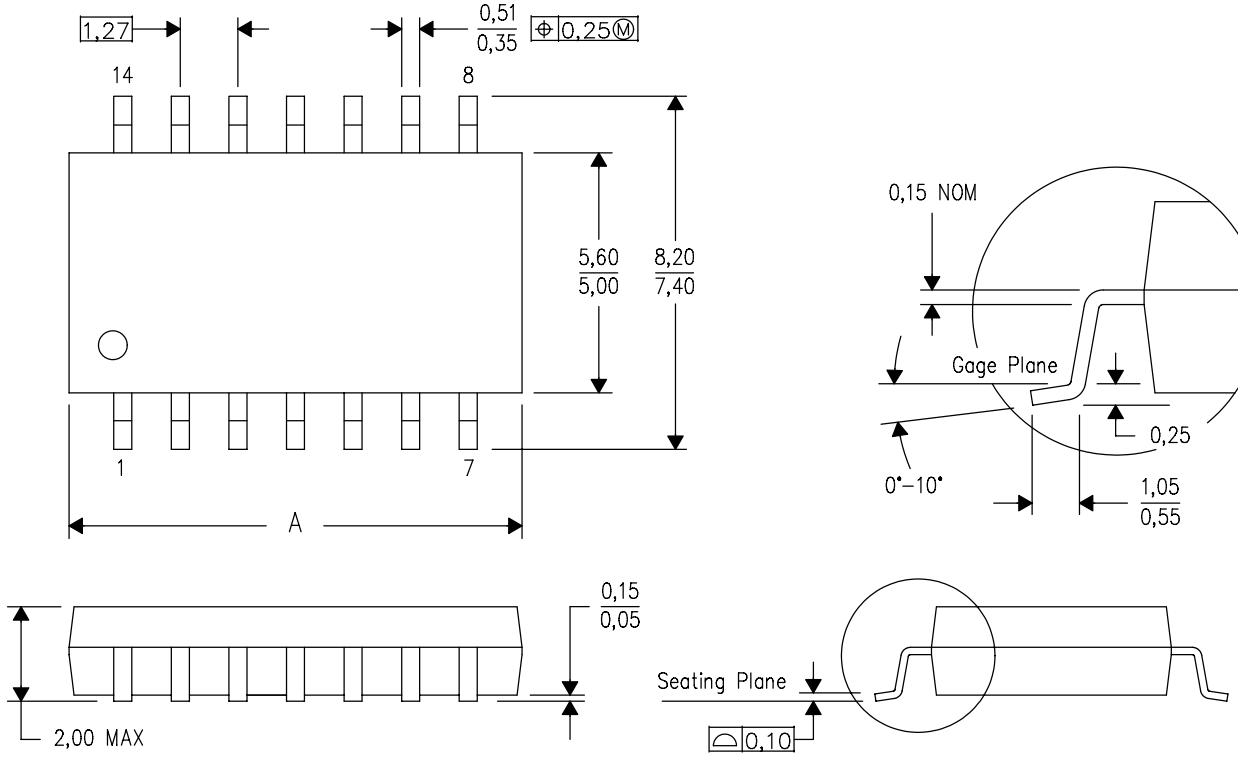
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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