HIGH SPEED, LOW POWER, OPERATIONAL AMPLIFIER

AD847

1.0 SCOPE

This specification documents the detail requirements for space qualified product manufactured on Analog Devices, Inc.'s QML certified line per MIL-PRF-38535 Level V except as modified herein. The manufacturing flow described in the STANDARD SPACE LEVEL PRODUCTS PROGRAM brochure is to be considered a part of this specification. http://www.analog.com/aerospace. This data sheet specifically details the space grade version of this product. A more detailed operational description and a complete data sheet for commercial product grades can be found at www.analog.com/AD847.

2.0 Part Number. The complete part number(s) of this specification follow:

Part Number	Description
AD847-703Q	High speed, low power, operational amplifier

2.1 Case Outline.

Letter	Descriptive designator	Case Outline (Lead Finish per MIL-PRF-38535)
Q	GDIP1-T8	8-Lead ceramic dual-in-line package (CERDIP)

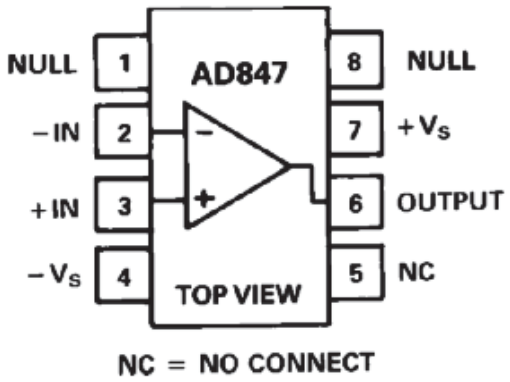

Figure 1 - Terminal connections.

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3.0 **Absolute Maximum Ratings**. (T_A = 25°C, unless otherwise noted)

Supply voltage ..... ±18V
Differential input voltage ..... ±6V
Input common mode voltage ..... $\pm V_S$
Operating temperature range ..... -55°C to +125°C
Storage temperature range ..... -65°C to +150°C
Power dissipation (P_D) 1.1W
Lead temperature (soldering, 10 seconds) ..... +300°C
Thermal resistance, junction-to-case (Θ_{JC}) ..... See MIL-STD-1835
Thermal resistance, junction-to-ambient (Θ_{JA}) ..... 110°C/W
Junction temperature (T_J) ..... +175°C

4.0 **Electrical Table**: See notes at end of table

Table I

Parameter	Symbol	Conditions 1/	Sub-group	2/ Min	2/ Max	Units
Input offset voltage	V_{IO}		1		±1.0	mV
			2, 3		±4.0	
Input bias current	I_B	V_S = ±5V, ±15V	1		5.0	µA
			2, 3		7.5	
Input offset current	I_{IO}		1		±300	nA
			2, 3		±400	
Common mode input voltage range 3/	IVR		1, 2, 3		±2.5	V
		V_S = ±15V	1, 2, 3		±12	
Open loop gain	AVO	V_{OUT} = ±2.5V, R_L = 500Ω	1	2.0		V/mV
			2, 3	1.0		
		V_{OUT}=±10V, R_L=1kΩ, V_S=±15V	1	3.0		
			2, 3	1.5		
Common mode rejection ratio	CMRR	V_{CM} = ±2.5V	1	80		dB
		V_{CM} = ±12V, V_S = ±15V	1	80		
			2, 3	75		
Output current 4/	I_{OUT}	V_{OUT} = ±2.5V	4	13		mA
		V_{OUT} = ±10V, V_S = ±15V	4	20		
Output voltage swing	$+V_{OUT}$	R_L = 500Ω	1	3.0		V
			2, 3	2.5		
		R_L = 150Ω	1	2.5		
		V_S = ±15V, R_L = 1kΩ	1, 2, 3	12		
		V_S = ±15V, R_L = 500Ω	1	10		
	$-V_{OUT}$	R_L = 500Ω	1	-3.0		
			2, 3	-2.5		
		R_L = 150Ω	1	-2.5		
		V_S = ±15V, R_L = 1kΩ	1, 2, 3	-12		
		V_S = ±15V, R_L = 500Ω	1	-10		
Quiescent power supply current	I_{CC}		1		5.7	mA
			2, 3		7.8	
		V_S = ±15V	1		6.3	
			2, 3		8.4	
Power supply rejection ratio	PSRR	V_S = ±5V to ±15V	1	75		dB
			2, 3	72		
Differential input resistance 4/	R_{IN}	V_S = ±5V, ±15V	4	80		kΩ
Slew rate 6/ 4/	+SR	V_{OUT} = -2.5V to +2.5V, R_L = 500KΩ, A_V = 1V/V	4	120		V/µS
		Measured from 10% to 90%	5, 6	90		
	-SR	V_{OUT} = +2.5V to -2.5V, R_L = 500KΩ, A_V = 1V/V	4	90		
		Measured from 10% to 90%	5, 6	65		

Table I						
Parameter	**Symbol**	**Conditions 1/**	**Sub-group**	**2/ Min**	**2/ Max**	**Units**
	+SR	V_{OUT} = -5V to +5V, R_L = 1KΩ, V_S = ±15V	4	200		
		Measured from 10% to 90%	5, 6	130		
	-SR	V_{OUT} = +5V to -5V, R_L = 1KΩ, V_S = ±15V	4	145		
		Measured from 10% to 90%	5, 6	120		
Gain bandwidth product 4/	GBWP	V_{OUT} = ±100mV, R_L - 500Ω	4	25		MHz
		V_{OUT} = ±100mV, R_L = 1KΩ, VS = ±15V		40		
Full power bandwidth 4/	FPBW	V_{PK} = 2.5V, R_L = 500Ω	4	5.7		
		V_{PK} = 10V, R_L = 1KΩ, V_S = ±15V		2.8		
Closed loop stable gain 4/	CLSG	R_L = 1KΩ, V_S = ±5V, ±15V	4, 5, 6	1.0		V/V
Rise time 4/ 8/	r_r	V_{OUT} = 0V to +200mV, A_V = +1, R_L =-1KΩ, V_S = ±15V	4, 5, 6		10	nS
	t_f	V_{OUT} = 0V to -200mV, A_V = +1, R_L =-1KΩ, V_S = ±15V	4, 5, 6		10	
Settling time 4/	t_s	A_V = -1V/V, 10V step at 0.1% of the fixed value, R_L = 1KΩ			150	
		A_V = -1V/V, 10V step at 0.01% of the fixed value, R_L = 1KΩ			200	
Overshoot 4/	+OS	V_{OUT} = 0V to +200mV, A_V = +1, R_L = 1KΩ, V_S = ±15V	4		30	%
	-OS	V_{OUT} = 0V to -200mV, A_V = +1, R_L = 1KΩ, V_S = ±15V	4		30	

TABLE I NOTES:

1/ Unless otherwise specified for dc tests, V_S = ±5V, R_S < 100Ω, R_L > 100kΩ, V_{OUT} = 0V, and $C_L \leq$ 10pF. Unless otherwise specified for ac tests, A_V = ±1 V/V, R_L = 1kΩ, and C_L = 10pF.

2/ The limiting terms "min" (minimum) and "max" (maximum) shall be considered to apply to magnitudes only. Negative current shall be defined as conventional current flow out of a device terminal.

3/ This parameter is guaranteed by CMRR test.

4/ If not tested, shall be guaranteed to the limits specified in table I herein.

5/ Quiescent power consumption is based on quiescent supply current test maximum (no load at the output).

6/ Slew rate test limits are guarantee after 5 minutes of warm-up.

7/ Full power bandwidth = $SR/(2\pi V_{PK})$.

8/ Rise and fall times measured between 10% and 90% point.

4.1 Electrical Test Requirements:

Table II	
Test Requirements	Subgroups (in accordance with MIL-PRF-38535, Table III)
Interim Electrical Parameters	1
Final Electrical Parameters	1, 2, 3, 4, 5, 6 1/ 2/
Group A Test Requirements	1, 2, 3, 4, 5, 6
Group C end-point electrical parameters	1 2/
Group D end-point electrical parameters	1
Group E end-point electrical parameters	1

1/ PDA applies to Subgroup 1. Delta's excluded from PDA.
2/ See Table III for delta parameters. See table I for conditions.

4.1 Table III. Burn-in test delta limits.

Table III				
TEST TITLE	BURN-IN ENDPOINT	LIFETEST ENDPOINT	DELTA LIMIT	UNITS
V_{OS}	±1	±1.5	±0.5	mV
$\pm I_B$	5	7.5	2.5	uA
I_{IO}	±300	±500	±200	nA

5.0 Life Test/Burn-In Circuit:

5.1 HTRB is not applicable for this drawing.
5.2 Burn-in is per MIL-STD-883 Method 1015 test condition B.
5.3 Steady state life test is per MIL-STD-883 Method 1005.

Rev	Description of Change	Date
A	Initiate	7/20/2000
B	Update web address	2/7/2002
C	Update web address. Delete Burn-In circuit.	6/20/2003
D	Update header/footer & add to 1.0 scope description.	2/25/2008
E	Remove obsolete product and update ASD to Analog Standard	11/30/2011
F	Correct typo in Table 3 section 4.1 *A to uA.	06/29/2012

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