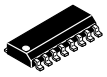
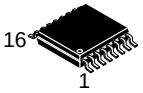
# 3-to-8 Line Decoder

# MM74HCT138



**SOIC−16**
**CASE 751B−05/751BG−01**




**TSSOP−16**
**CASE 948F−01**

## General Description

The MM74HCT138 decoder utilizes advanced silicon−gate CMOS technology, and are well suited to memory address decoding or data routing applications. Both circuits feature high noise immunity and low power consumption usually associated with CMOS circuitry, yet have speeds comparable to low power Schottky TTL logic.

The MM74HCT138 have 3 binary select inputs (A, B, and C). If the device is enabled these inputs determine which one of the eight normally HIGH outputs will go LOW. Two active LOW and one active HIGH enables (G1, G2A and G2B) are provided to ease the cascading decoders.

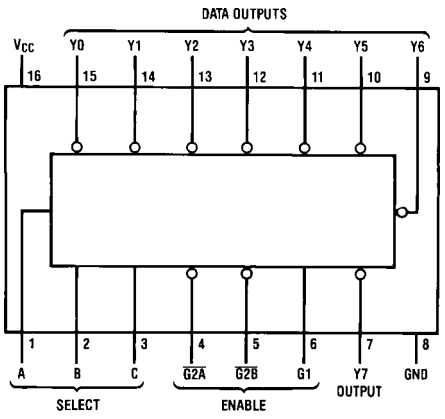
The decoders' output can drive 10 low power Schottky TTL equivalent loads and are functionally and pin equivalent to the 74LS138. All inputs are protected from damage due to static discharge by diodes to VCC and ground.

MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug−in replacements for LS−TTL devices and can be used to reduce power consumption in existing designs.

## Features

- TTL Input Compatible
- Typical Propagation Delay: 20 ns
- Low Quiescent Current: 160 μA Maximum (74HCT Series)
- Low Input Current: 1 μA Maximum
- Fanout of 10 LS−TTL Loads
- These are Pb−Free Devices

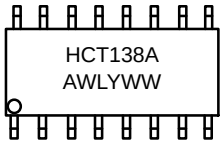
## Connection Diagram



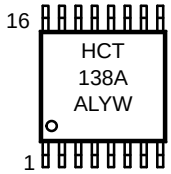

Top View

**Figure 1. Pin Assignments for SOIC and TSSOP**

## MARKING DIAGRAM




SOIC−16




TSSOP−16

HCT138A = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
Y = Year
WW, W = Work Week

## ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

**TRUTH TABLE**

| Inputs | | | | | Outputs | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Enable | | Select | | | | | | | | | | |
| G1 | $\overline{G2}$ (Note 1) | C | B | A | Y0 | Y01 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
| X | H | X | X | X | H | H | H | H | H | H | H | H |
| L | X | X | X | X | H | H | H | H | H | H | H | H |
| H | L | L | L | L | L | H | H | H | H | H | H | H |
| H | L | L | L | H | H | L | H | H | H | H | H | H |
| H | L | L | H | L | H | H | L | H | H | H | H | H |
| H | L | L | H | H | H | H | H | L | H | H | H | H |
| H | L | H | L | L | H | H | H | H | L | H | H | H |
| H | L | H | L | H | H | H | H | H | H | L | H | H |
| H | L | H | H | L | H | H | H | H | H | H | L | H |
| H | L | H | H | H | H | H | H | H | H | H | H | L |

H = HIGH Level
L = LOW Level
X = Don't Care

1. $\overline{G2} = \overline{G2A} + \overline{G2B}$

**Logic Diagram**

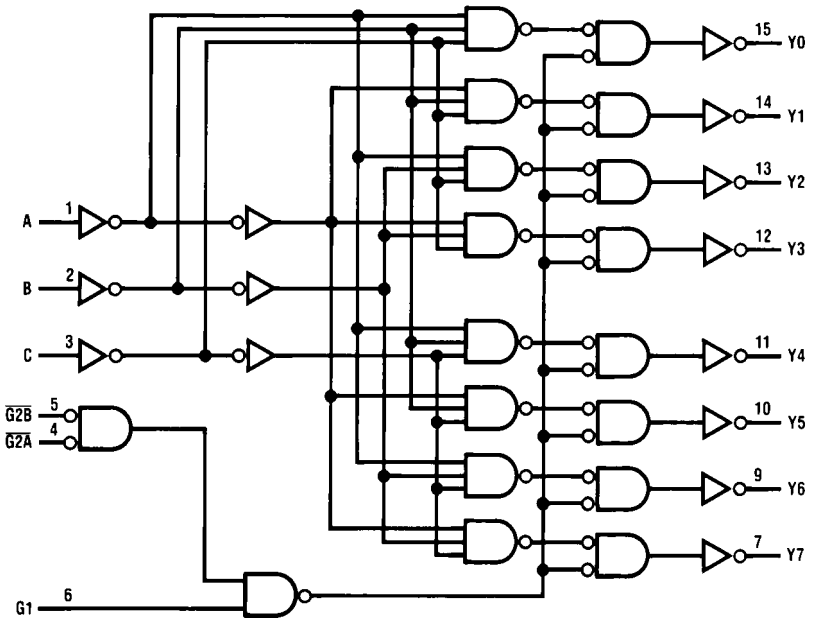



**Figure 2. Logic Diagram**

**ABSOLUTE MAXIMUM RATINGS** (Note 2)

| Symbol | Parameter | | Rating |
|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | –0.5 to +7.0 V |
| $V_{IN}$ | DC Input Voltage | | –0.5 to $V_{CC}$ + 0.5 V |
| $V_{OUT}$ | DC Output Voltage | | –0.5 to $V_{CC}$ + 0.5 V |
| $I_{IK}$, $I_{OK}$ | Clamp Diode Current | | ±20 mA |
| $I_{OUT}$ | DC Output Current, per Pin | | ±25 mA |
| $I_{CC}$ | DC $V_{CC}$ or GND Current, per Pin | | ±50 mA |
| $T_{STG}$ | Storage Temperature Range | | –65°C to +150°C |
| $P_D$ | Power Dissipation | S.O. Package Only | 500 mW |
| $T_L$ | Lead Temperature (Soldering 10 Seconds) | | 260°C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Unless otherwise specified all voltages are referenced to ground.

**RECOMMENDED OPERATING CONDITIONS**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 4.5 | 5.5 | V |
| $V_{IN}$, $V_{OUT}$ | DC Input or Output Voltage | 0 | $V_{CC}$ | V |
| $T_A$ | Operating Temperature Range | –55 | +125 | °C |
| $t_r$, $t_f$ | Input Rise or Fall Times | – | 500 | ns |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

**DC ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 5 V ±10% (unless otherwise specified))

| Symbol | Parameter | Conditions | $T_A$ = 25°C | $T_A$ = −40°C to 85°C | $T_A$ = −55°C to 125°C | Unit |
|---|---|---|---|---|---|---|
| | | | Typ | Guaranteed Limits | | |
| $V_{IH}$ | Minimum HIGH Level Input Voltage | | – | 2.0 | 2.0 | 2.0 | V |
| $V_{IL}$ | Maximum LOW Level Input Voltage | | – | 0.8 | 0.8 | 0.8 | V |
| $V_{OH}$ | Minimum HIGH Level Output Voltage | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | | |
| | | $\|I_{OUT}\|$ = 20 μA | $V_{CC}$ | $V_{CC}$ − 0.1 | $V_{CC}$ − 0.1 | $V_{CC}$ − 0.1 | V |
| | | $\|I_{OUT}\|$ = 4.0 mA, $V_{CC}$ = 4.5 V | 4.2 | 3.98 | 3.84 | 3.7 | V |
| | | $\|I_{OUT}\|$ = 4.8 mA, $V_{CC}$ = 5.5 V | 5.2 | 4.98 | 4.84 | 4.7 | V |
| $V_{OL}$ | Maximum LOW Level Voltage | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | | |
| | | $\|I_{OUT}\|$ = 20 μA | 0 | 0.1 | 0.1 | 0.1 | V |
| | | $\|I_{OUT}\|$ = 4.0 mA, $V_{CC}$ = 4.5 V | 0.2 | 0.26 | 0.33 | 0.4 | V |
| | | $\|I_{OUT}\|$ = 4.8 mA, $V_{CC}$ = 5.5 V | 0.2 | 0.26 | 0.33 | 0.4 | V |
| $I_{IN}$ | Maximum Input Current | $V_{IN}$ = $V_{CC}$ or GND, $V_{IH}$ or $V_{IL}$ | – | ±0.1 | ±1.0 | ±1.0 | μA |
| $I_{CC}$ | Maximum Quiescent Supply Current | $V_{IN}$ = $V_{CC}$ or GND, $I_{OUT}$ = 0 μA | – | 8.0 | 80 | 160 | μA |
| | | $V_{IN}$ = 2.4 V or 0.5 V (Note 3) | – | 0.3 | 0.4 | 0.5 | mA |

3. This is measured per input pin. All other inputs are held at $V_{CC}$ or ground.

**AC ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C, $V_{CC}$ = 5.0 V, $t_r = t_f$ = 6 ns, $C_L$ = 15 pF (unless otherwise specified))

| Symbol | Parameter | Conditions | Typ | Guaranteed Limit | Unit |
|---|---|---|---|---|---|
| $t_{PHL}$ | Maximum Propagation Delay, A, B, or C to Output | | 20 | 35 | ns |
| $t_{PLH}$ | Maximum Propagation Delay, A, B, or C to Output | | 13 | 25 | ns |
| $t_{PHL}$ | Maximum Propagation Delay, G1 to Y Output | | 14 | 25 | ns |
| $t_{PLH}$ | Maximum Propagation Delay, G1 to Y Output | | 13 | 25 | ns |
| $t_{PHL}$ | Maximum Propagation Delay, $\overline{G2A}$ or $\overline{G2B}$ to Y Output | | 17 | 30 | ns |
| $t_{PLH}$ | Maximum Propagation Delay, $\overline{G2A}$ or $\overline{G2B}$ to Y Output | | 13 | 25 | ns |

**AC ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 5 V ±10%, $C_L$ = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified))

| Symbol | Parameter | Conditions | $T_A$ = 25°C | $T_A$ = −40°C to 85°C | $T_A$ = −55°C to 125°C | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Typ | Guaranteed Limits | | | |
| $t_{PHL}$ | Maximum Propagation Delay A, B, or C to Output | | 24 | 40 | 50 | 60 | ns |
| $t_{PLH}$ | Maximum Propagation Delay A, B, or C to Output | | 18 | 30 | 38 | 45 | ns |
| $t_{PHL}$ | Maximum Propagation Delay G1 to Y Output | | 17 | 30 | 38 | 45 | ns |
| $t_{PLH}$ | Maximum Propagation Delay G1 to Y Output | | 20 | 30 | 38 | 45 | ns |
| $t_{PHL}$ | Maximum Propagation Delay $\overline{G2A}$ or $\overline{G2B}$ to Y Output | | 23 | 35 | 43 | 52 | ns |
| $t_{PLH}$ | Maximum Propagation Delay $\overline{G2A}$ or $\overline{G2B}$ to Y Output | | 18 | 30 | 38 | 45 | ns |
| $t_{THL}$, $t_{TLH}$ | Maximum Output Rise and Fall Time | | − | 15 | 19 | 22 | ns |
| $C_{IN}$ | Input Capacitance | | − | 5 | 10 | 10 | pF |
| $C_{PD}$ | Power Dissipation Capacitance | (Note 4) | 55 | − | − | − | pF |

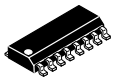
4. $C_{PD}$ determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

## ORDERING INFORMATION

| Part Number | Package | Shipping† |
|---|---|---|
| MM74HCT138M | SOIC−16, Case 751B−05 (Pb−Free) | 48 Units / Tube |
| MM74HCT138MTC | TSSOP−16, Case 948F−01 (Pb−Free) | 96 Units / Tube |
| MM74HCT138MX | SOIC−16, Case 751BG−01 (Pb−Free) | 2500 Units / Tape & Reel |
| MM74HCT138MTCX | TSSOP−16, Case 948F−01 (Pb−Free) | 2500 Units / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

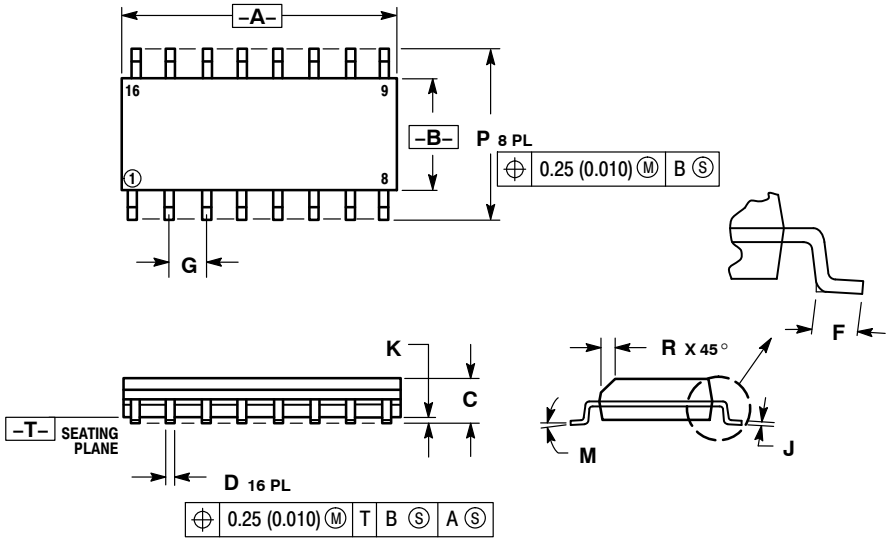
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS



SCALE 1:1

**SOIC−16**
CASE 751B−05
ISSUE K

DATE 29 DEC 2006



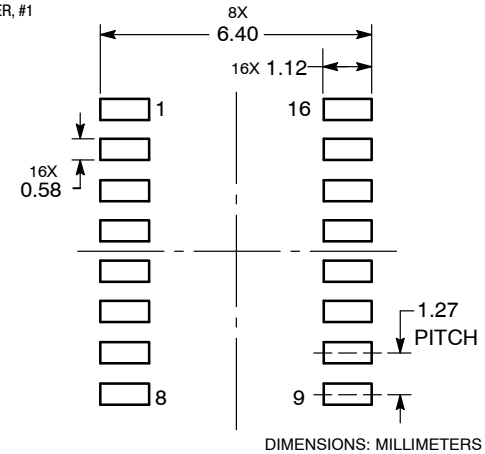

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

| STYLE 1: | | STYLE 2: | | STYLE 3: | | STYLE 4: | |
|---|---|---|---|---|---|---|---|
| PIN 1. | COLLECTOR | PIN 1. | CATHODE | PIN 1. | COLLECTOR, DYE #1 | PIN 1. | COLLECTOR, DYE #1 |
| 2. | BASE | 2. | ANODE | 2. | BASE, #1 | 2. | COLLECTOR, #1 |
| 3. | EMITTER | 3. | NO CONNECTION | 3. | EMITTER, #1 | 3. | COLLECTOR, #2 |
| 4. | NO CONNECTION | 4. | CATHODE | 4. | COLLECTOR, #1 | 4. | COLLECTOR, #2 |
| 5. | EMITTER | 5. | CATHODE | 5. | COLLECTOR, #2 | 5. | COLLECTOR, #3 |
| 6. | BASE | 6. | NO CONNECTION | 6. | BASE, #2 | 6. | COLLECTOR, #3 |
| 7. | COLLECTOR | 7. | ANODE | 7. | EMITTER, #2 | 7. | COLLECTOR, #4 |
| 8. | COLLECTOR | 8. | CATHODE | 8. | COLLECTOR, #2 | 8. | COLLECTOR, #4 |
| 9. | BASE | 9. | CATHODE | 9. | COLLECTOR, #3 | 9. | BASE, #4 |
| 10. | EMITTER | 10. | ANODE | 10. | BASE, #3 | 10. | EMITTER, #4 |
| 11. | NO CONNECTION | 11. | NO CONNECTION | 11. | EMITTER, #3 | 11. | BASE, #3 |
| 12. | EMITTER | 12. | CATHODE | 12. | COLLECTOR, #3 | 12. | EMITTER, #3 |
| 13. | BASE | 13. | CATHODE | 13. | COLLECTOR, #4 | 13. | BASE, #2 |
| 14. | COLLECTOR | 14. | NO CONNECTION | 14. | BASE, #4 | 14. | EMITTER, #2 |
| 15. | EMITTER | 15. | ANODE | 15. | EMITTER, #4 | 15. | BASE, #1 |
| 16. | COLLECTOR | 16. | CATHODE | 16. | COLLECTOR, #4 | 16. | EMITTER, #1 |

| STYLE 5: | | STYLE 6: | | STYLE 7: | |
|---|---|---|---|---|---|
| PIN 1. | DRAIN, DYE #1 | PIN 1. | CATHODE | PIN 1. | SOURCE N-CH |
| 2. | DRAIN, #1 | 2. | CATHODE | 2. | COMMON DRAIN (OUTPUT) |
| 3. | DRAIN, #2 | 3. | CATHODE | 3. | COMMON DRAIN (OUTPUT) |
| 4. | DRAIN, #2 | 4. | CATHODE | 4. | GATE P-CH |
| 5. | DRAIN, #3 | 5. | CATHODE | 5. | COMMON DRAIN (OUTPUT) |
| 6. | DRAIN, #3 | 6. | CATHODE | 6. | COMMON DRAIN (OUTPUT) |
| 7. | DRAIN, #4 | 7. | CATHODE | 7. | COMMON DRAIN (OUTPUT) |
| 8. | DRAIN, #4 | 8. | CATHODE | 8. | SOURCE P-CH |
| 9. | GATE, #4 | 9. | ANODE | 9. | SOURCE P-CH |
| 10. | SOURCE, #4 | 10. | ANODE | 10. | COMMON DRAIN (OUTPUT) |
| 11. | GATE, #3 | 11. | ANODE | 11. | COMMON DRAIN (OUTPUT) |
| 12. | SOURCE, #3 | 12. | ANODE | 12. | COMMON DRAIN (OUTPUT) |
| 13. | GATE, #2 | 13. | ANODE | 13. | GATE N-CH |
| 14. | SOURCE, #2 | 14. | ANODE | 14. | COMMON DRAIN (OUTPUT) |
| 15. | GATE, #1 | 15. | ANODE | 15. | COMMON DRAIN (OUTPUT) |
| 16. | SOURCE, #1 | 16. | ANODE | 16. | SOURCE N-CH |

**RECOMMENDED SOLDERING FOOTPRINT***




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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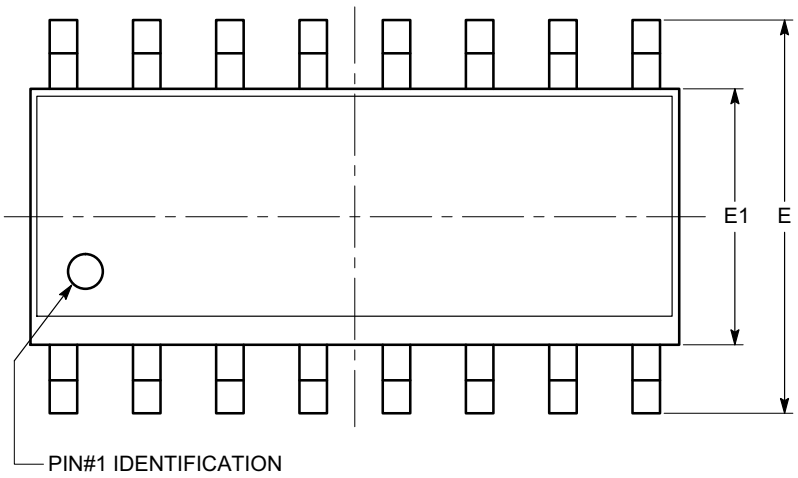
|---|---|---|
| DESCRIPTION: | SOIC−16 | PAGE 1 OF 1 |

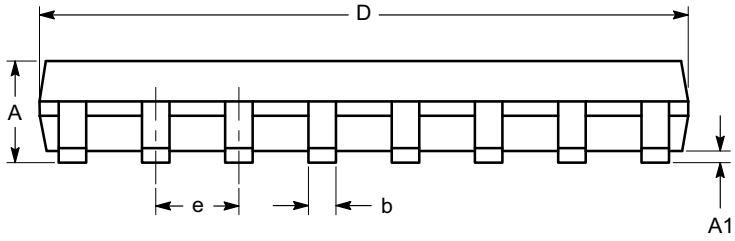
**SOIC−16, 150 mils**
CASE 751BG−01
ISSUE O

DATE 19 DEC 2008

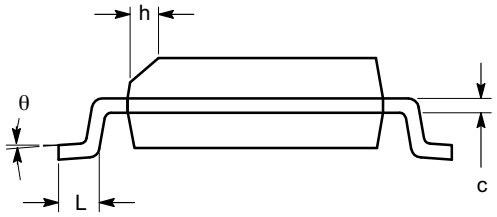



**TOP VIEW**

| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | 1.35 | | 1.75 |
| A1 | 0.10 | | 0.25 |
| b | 0.33 | | 0.51 |
| c | 0.19 | | 0.25 |
| D | 9.80 | 9.90 | 10.00 |
| E | 5.80 | 6.00 | 6.20 |
| E1 | 3.80 | 3.90 | 4.00 |
| e | | 1.27 BSC | |
| h | 0.25 | | 0.50 |
| L | 0.40 | | 1.27 |
| θ | 0º | | 8º |




**SIDE VIEW**




**END VIEW**

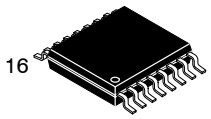
**Notes:**
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

| | | |
|---|---|---|
| **DOCUMENT NUMBER:** | **98AON34275E** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| **DESCRIPTION:** | **SOIC−16, 150 MILS** | **PAGE 1 OF 1** |

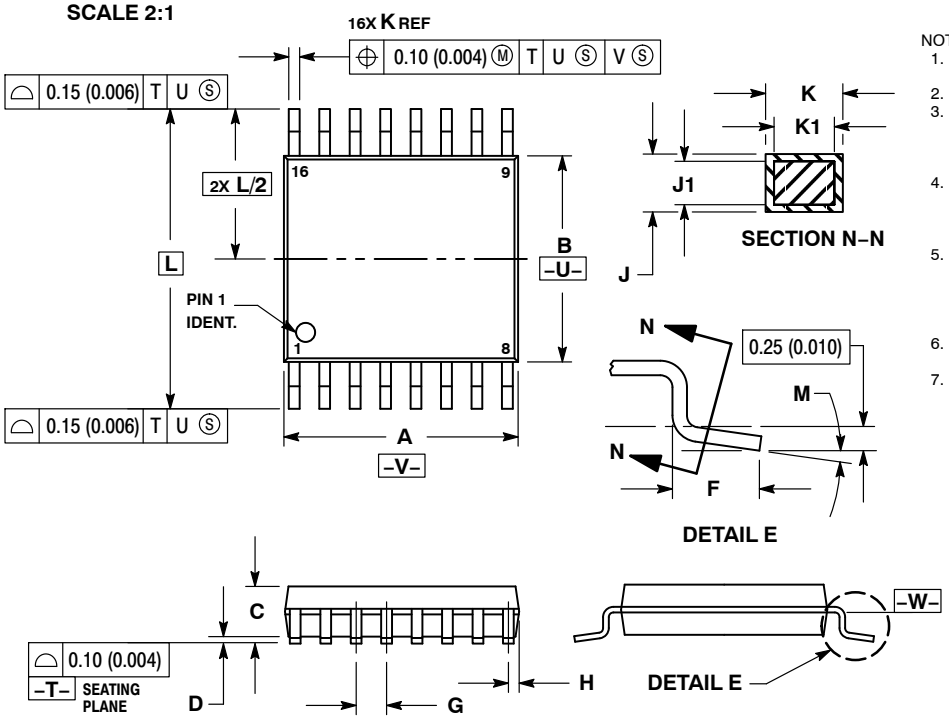
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

**TSSOP−16 WB**
CASE 948F
ISSUE B

DATE 19 OCT 2006



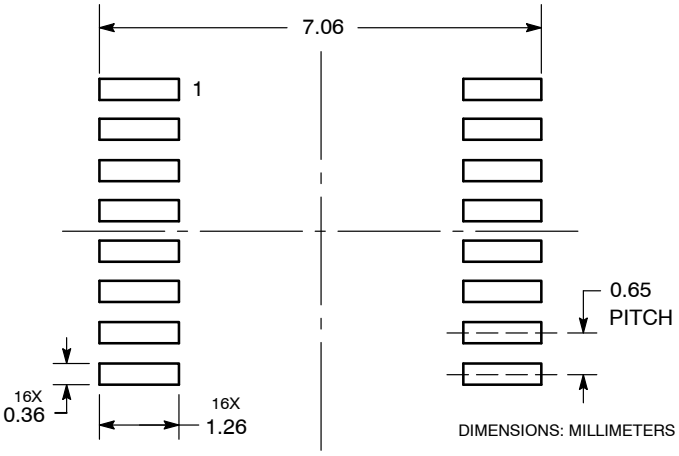

**SCALE 2:1**




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

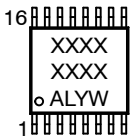
| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | −−− | 1.20 | −−− | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.18 | 0.28 | 0.007 | 0.011 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0 ° | 8 ° | 0 ° | 8 ° |

### RECOMMENDED SOLDERING FOOTPRINT*




*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM*




| | |
|---|---|
| XXXX | = Specific Device Code |
| A | = Assembly Location |
| L | = Wafer Lot |
| Y | = Year |
| W | = Work Week |
| G or ▪ | = Pb−Free Package |

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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| **DESCRIPTION:** | **TSSOP−16** | | **PAGE 1 OF 1** |

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