# 74ALVCH16952

## 16-bit registered transceiver; 3-state

Rev. 3 — 9 January 2018 Product data sheet

## 1 General description

The 74ALVCH16952 consists of two sections, each containing a dual octal non-inverting registered transceiver. Two 8-bit back to back registers store data flowing in both directions between two bidirectional buses. Data applied to the inputs is entered and stored on the rising edge of the clock (nCPAB and nCPBA) provided that the clock enable ($n\overline{CEAB}$ and $n\overline{CEBA}$) is LOW. The data is then present at the output buffers, but is only accessible when the output enable input ($n\overline{OEAB}$ and $n\overline{OEBA}$) is LOW. Data flow from A inputs to B outputs is the same as for B inputs to A outputs.

## 2 Features and benefits

- CMOS low-power consumption
- Multibyte flow-through pinout architecture
- Low inductance, multiple center power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- Output drive capability 50 Ω transmission lines at 85 °C
- Complies with JEDEC standard JESD8-B

## 3 Ordering information

**Table 1. Ordering information**

| Type number | Package | | | |
|---|---|---|---|---|
| | Temperature range | Name | Description | Version |
| 74ALVCH16952DGG | -40 °C to +85 °C | TSSOP56 | plastic thin shrink small outline package; 56 leads; body width 6.1 mm | SOT364-1 |

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# 4 Functional diagram

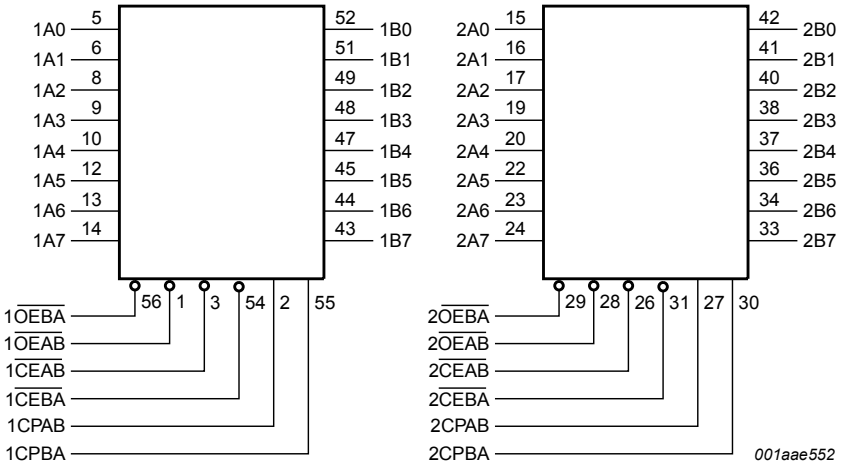



**Figure 1. Logic symbol**

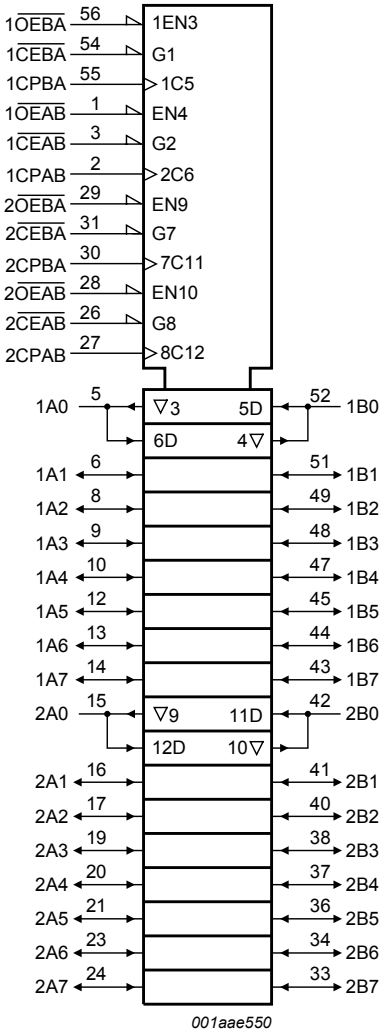



**Figure 2. IEC logic symbol**

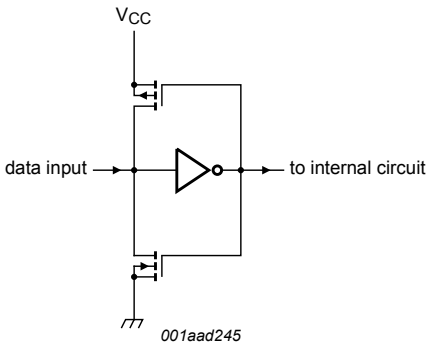



**Figure 3. Bus hold circuit**

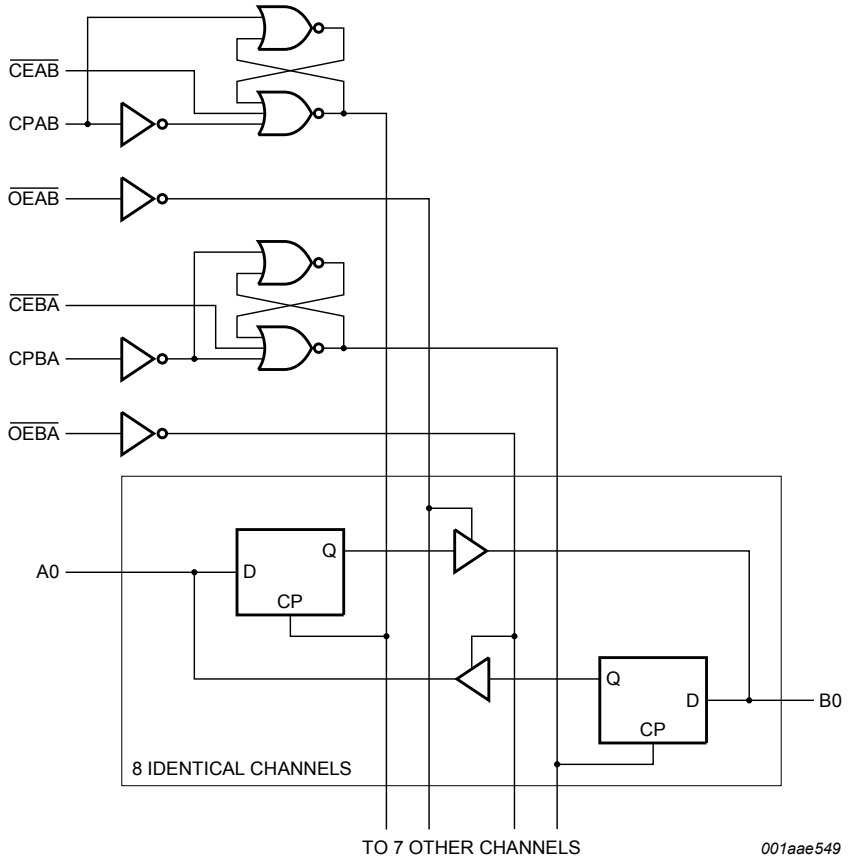



**Figure 4. Schematic diagram (one section)**

# 5 Pinning information

## 5.1 Pinning

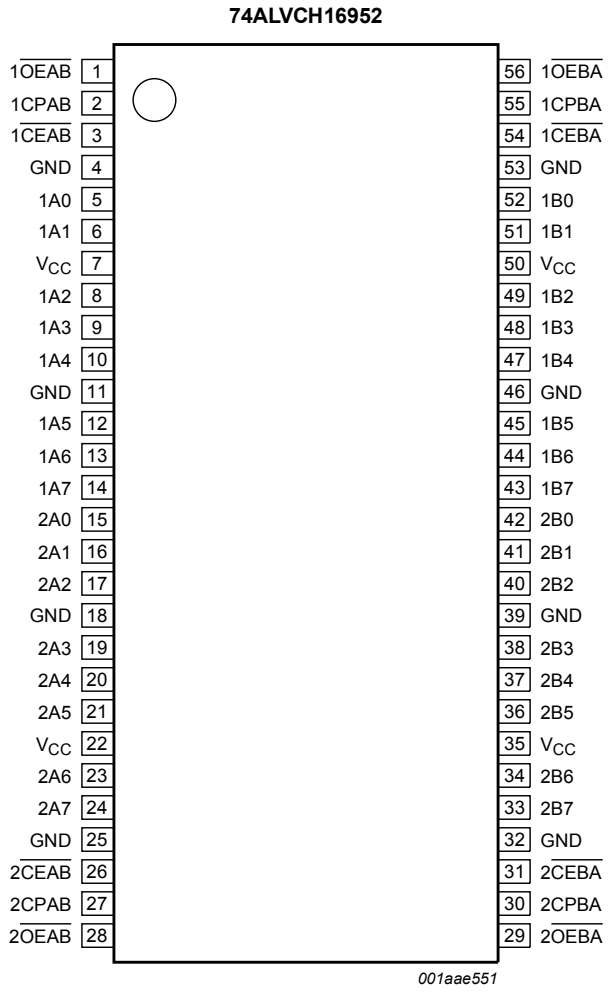



**Figure 5. Pin configuration**

### 5.2 Pin description

**Table 2. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| 1A0, 1A1, 1A2, 1A3, 1A4, 1A5, 1A6, 1A7 | 5, 6, 8, 9, 10, 12, 13, 14 | data inputs or outputs |
| 1B0, 1B1, 1B2, 1B3, 1B4, 1B5, 1B6, 1B7 | 52, 51, 49, 48, 47, 45, 44, 43 | data inputs or outputs |
| 2A0, 2A1, 2A2, 2A3, 2A4, 2A5, 2A6, 2A7 | 15, 16, 17, 19, 20, 21, 23, 24 | data inputs or outputs |
| 2B0, 2B1, 2B2, 2B3, 2B4, 2B5, 2B6, 2B7 | 42, 41, 40, 38, 37, 36, 34, 33 | data inputs or outputs |
| 1$\overline{OEAB}$, 1$\overline{OEBA}$, 2$\overline{OEAB}$, 2$\overline{OEBA}$ | 1, 56, 28, 29 | output enable input (active LOW) |
| 1$\overline{CEAB}$, 1$\overline{CEBA}$, 2$\overline{CEAB}$, 2$\overline{CEBA}$ | 3, 54, 26, 31 | clock enable input (active LOW) |
| 1CPAB, 1CPBA, 2CPAB, 2CPBA | 2, 55, 27, 30 | clock pulse input (LOW-to-HIGH, edge-triggered) |
| GND | 4, 11, 18, 25, 32, 39, 46, 53 | ground (0 V) |
| $V_{CC}$ | 7, 22, 35, 50 | supply voltage |

## 6 Functional description

**Table 3. Function table [1]**

| Operating mode | Control | | | Input | Internal | Output |
|---|---|---|---|---|---|---|
| **A to B, B to A** | **n$\overline{OEAB}$, n$\overline{OEBA}$** | **n$\overline{CEAB}$, n$\overline{CEBA}$** | **nCPAB, nCPBA** | **nAn, nBn** | **nQn** | **nBn, nAn** |
| Hold | L | H | X | X | NC | NC |
| Load and output enable | L | L | ↑ | L | L | L |
| | | | | H | H | H |
| Load and output disable | H | L | ↑ | L | L | Z |
| | | | | H | H | Z |

[1] H = HIGH voltage level;
L = LOW voltage level;
↑ = LOW-to-HIGH clock transition;
X = don't care;
Z = high impedance OFF-state;
NC = no change.

# 7 Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | | -0.5 | +4.6 | V |
| $V_I$ | input voltage | control pins | [1] | -0.5 | +4.6 | V |
| | | data inputs | [1] | -0.5 | $V_{CC}$ + 0.5 | V |
| $V_O$ | output voltage | | [1] | -0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | input clamping current | $V_I$ < 0 V | | - | -50 | mA |
| $I_{OK}$ | output clamping current | $V_O$ > $V_{CC}$ or $V_O$ < 0 V | | - | ±50 | mA |
| $I_O$ | output current | $V_O$ = 0 V to $V_{CC}$ | | - | ±50 | mA |
| $I_{CC}$ | supply current | | | - | 100 | mA |
| $I_{GND}$ | ground current | | | -100 | - | mA |
| $T_{stg}$ | storage temperature | | | -65 | +150 | °C |
| $P_{tot}$ | total power dissipation | $T_{amb}$ = -40 °C to +125 °C | [2] | - | 600 | mW |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] For TSSOP56 package: $P_{tot}$ derates linearly with 8 mW/K above 55 °C.

# 8 Recommended operating conditions

**Table 5. Recommended operating conditions**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | maximum speed performance | | | | |
| | | $C_L$ = 30 pF | 2.3 | - | 2.7 | V |
| | | $C_L$ = 50 pF | 3.0 | - | 3.6 | V |
| $V_I$ | input voltage | | 0 | - | $V_{CC}$ | V |
| $V_O$ | output voltage | | 0 | - | $V_{CC}$ | V |
| $T_{amb}$ | ambient temperature | operating in free-air | -40 | - | +85 | °C |
| Δt/ΔV | input transition rise and fall rate | $V_{CC}$ = 2.3 V to 3.0 V | 0 | - | 20 | ns/V |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 0 | - | 10 | ns/V |

# 9 Static characteristics

**Table 6. Static characteristics**

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | $T_{amb}$ = -40 °C to +85 °C | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ [1] | Max | |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | 1.2 | - | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 2.0 | 1.5 | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 2.3 V to 2.7 V | - | 1.2 | 0.7 | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | - | 1.5 | 0.8 | V |
| $V_{OH}$ | HIGH-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | |
| | | $V_{CC}$ = 2.3 V to 3.6 V; $I_O$ = -100 µA | $V_{CC}$ - 0.2 | $V_{CC}$ | - | V |
| | | $V_{CC}$ = 2.3 V; $I_O$ = -6 mA | $V_{CC}$ - 0.3 | $V_{CC}$ - 0.08 | - | V |
| | | $V_{CC}$ = 2.3 V; $I_O$ = -12 mA | $V_{CC}$ - 0.6 | $V_{CC}$ - 0.26 | - | V |
| | | $V_{CC}$ = 2.7 V; $I_O$ = -12 mA | $V_{CC}$ - 0.5 | $V_{CC}$ - 0.14 | - | V |
| | | $V_{CC}$ = 3.0 V; $I_O$ = -12 mA | $V_{CC}$ - 0.6 | $V_{CC}$ - 0.09 | - | V |
| | | $V_{CC}$ = 3.0 V; $I_O$ = -24 mA | $V_{CC}$ - 1.0 | $V_{CC}$ - 0.28 | - | V |
| $V_{OL}$ | LOW-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | |
| | | $V_{CC}$ = 2.3 V to 3.6 V; $I_O$ = 100 µA | - | GND | 0.20 | V |
| | | $V_{CC}$ = 2.3 V; $I_O$ = 6 mA | - | 0.07 | 0.40 | V |
| | | $V_{CC}$ = 2.3 V; $I_O$ = 12 mA | - | 0.15 | 0.70 | V |
| | | $V_{CC}$ = 2.7 V; $I_O$ = 12 mA | - | 0.14 | 0.40 | V |
| | | $V_{CC}$ = 3.0 V; $I_O$ = 24 mA | - | 0.27 | 0.55 | V |
| $I_I$ | input leakage current | $V_{CC}$ = 2.3 V to 3.6 V; $V_I$ = $V_{CC}$ or GND | - | 0.1 | 5 | µA |
| $I_{OZ}$ | OFF-state output current | $V_{CC}$ = 2.7 V to 3.6 V; $V_I$ = $V_{IH}$ or $V_{IL}$; $V_O$ = $V_{CC}$ or GND | - | 0.1 | 10 | µA |
| $I_{CC}$ | supply current | $V_{CC}$ = 2.3 V to 3.6 V; $V_I$ = $V_{CC}$ or GND; $I_O$ = 0 A | - | 0.2 | 40 | µA |
| $\Delta I_{CC}$ | additional supply current | $V_{CC}$ = 2.3 V to 3.6 V; $V_I$ = $V_{CC}$ - 0.6 V; $I_O$ = 0 A | - | 150 | 750 | µA |
| $I_{BHL}$ | bus hold LOW sustaining current | $V_{CC}$ = 2.3 V; $V_I$ = 0.7 V | 45 | - | - | µA |
| | | $V_{CC}$ = 3.0 V; $V_I$ = 0.8 V | 75 | 150 | - | µA |
| $I_{BHH}$ | bus hold HIGH sustaining current | $V_{CC}$ = 2.3 V; $V_I$ = 1.7 V | -45 | - | - | µA |
| | | $V_{CC}$ = 3.0 V; $V_I$ = 2.0 V | -75 | -175 | - | µA |
| $I_{BHLO}$ | bus hold LOW overdrive current | $V_{CC}$ = 3.6 V | 500 | - | - | µA |
| $I_{BHHO}$ | bus hold HIGH overdrive current | $V_{CC}$ = 3.6 V | -500 | - | - | µA |
| $C_i$ | input capacitance | | - | 3.0 | - | pF |

[1] Typical values are measured at $T_{amb}$ = 25 °C
Typical values for $V_{CC}$ = 2.3 V to 2.7 V are measured at $V_{CC}$ = 2.5 V
Typical values for $V_{CC}$ = 3.0 V to 3.6 V are measured at $V_{CC}$ = 3.3 V

## 10 Dynamic characteristics

**Table 7. Dynamic characteristics**

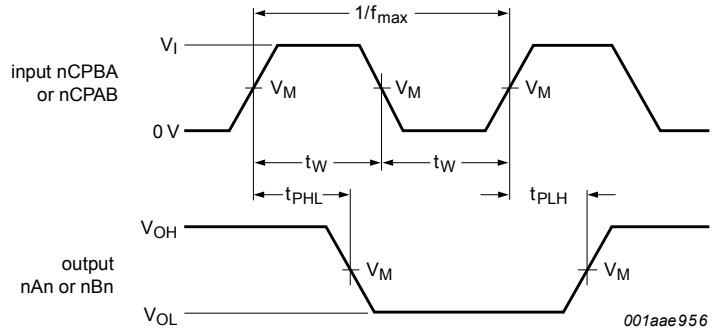
*Voltages are referenced to GND (ground = 0 V). $T_{amb}$ = −40 °C to +85 °C; For test circuit, see Figure 9.*

| Symbol | Parameter | Conditions | Min | Typ [1] | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{pd}$ | propagation delay | nCPBA to nAn; nCPAB to nBn; see Figure 6 [2] | | | | |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.0 | 3.2 | 4.1 | ns |
| | | $V_{CC}$ = 2.7 V | 1.0 | - | 4.6 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1.0 | 3.2 | 3.9 | ns |
| $t_{en}$ | enable time | $n\overline{OEBA}$ to nAn; $n\overline{OEAB}$ to nBn; see Figure 8 [3] | | | | |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.0 | - | 5.4 | ns |
| | | $V_{CC}$ = 2.7 V | 1.0 | - | 5.3 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1.0 | - | 4.4 | ns |
| $t_{dis}$ | disable time | $n\overline{OEBA}$ to nAn; $n\overline{OEAB}$ to nBn; see Figure 8 [4] | | | | |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.0 | - | 5.3 | ns |
| | | $V_{CC}$ = 2.7 V | 1.4 | - | 4.4 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1.1 | - | 4.0 | ns |
| $t_w$ | pulse width | nCPAB; nCPBA; HIGH or LOW; see Figure 6 | | | | |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 3.3 | - | - | ns |
| | | $V_{CC}$ = 2.7 V | 3.3 | - | - | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 3.3 | - | - | ns |
| $t_{su}$ | set-up time | nAn to nCPAB or nBn to nCPBA; see Figure 7 | | | | |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | - | - | ns |
| | | $V_{CC}$ = 2.7 V | 1.9 | - | - | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1.5 | - | - | ns |
| | | $n\overline{CEAB}$ to nCPAB or $n\overline{CEBA}$ to nCPBA; see Figure 7 | | | | |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.2 | - | - | ns |
| | | $V_{CC}$ = 2.7 V | 1.0 | - | - | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1.0 | - | - | ns |
| $t_h$ | hold time | nAn to nCPAB or nBn to nCPBA; see Figure 7 | | | | |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 0.6 | - | - | ns |
| | | $V_{CC}$ = 2.7 V | 0.6 | - | - | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 0.8 | - | - | ns |
| | | $n\overline{CEAB}$ to nCPAB or $n\overline{CEBA}$ to nCPBA; see Figure 7 | | | | |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.1 | - | - | ns |
| | | $V_{CC}$ = 2.7 V | 0.9 | - | - | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1.1 | - | - | ns |

| Symbol | Parameter | Conditions | Min | Typ [1] | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{max}$ | maximum frequency | CP; see Figure 6 | | | | |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 150 | 350 | - | MHz |
| | | $V_{CC}$ = 2.7 V | 150 | 350 | - | MHz |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 150 | 350 | - | MHz |
| $C_{PD}$ | power dissipation capacitance | per driver; $V_I$ = GND to $V_{CC}$ [5] | - | 30 | - | pF |

[1] Typical values are measured at $T_{amb}$ = 25 °C
Typical values for $V_{CC}$ = 2.3 V to 2.7 V are measured at $V_{CC}$ = 2.5 V
Typical values for $V_{CC}$ = 3.0 V to 3.6 V are measured at $V_{CC}$ = 3.3 V
[2] $t_{pd}$ is the same as $t_{PHL}$ and $t_{PLH}$.
[3] $t_{en}$ is the same as $t_{PZH}$ and $t_{PZL}$.
[4] $t_{dis}$ is the same as $t_{PHZ}$ and $t_{PLZ}$.
[5] $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in µW):
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
$f_i$ = input frequency in MHz;
$f_o$ = output frequency in MHz;
$C_L$ = output load capacitance in pF;
$V_{CC}$ = supply voltage in V;
N = number of inputs switching;
$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

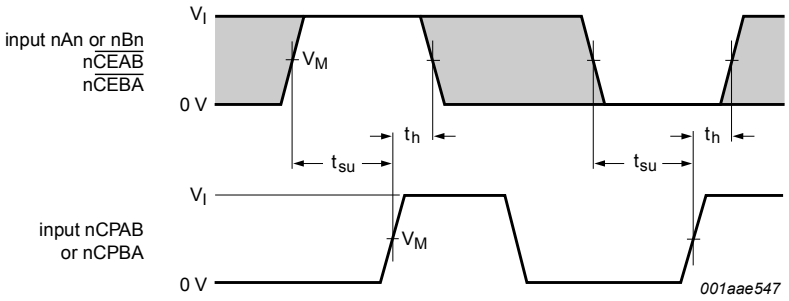
## 10.1 Waveforms and test circuit




Measurements points are given in Table 8.

$V_{OL}$ and $V_{OH}$ are typical voltage output levels that occur with the output load.

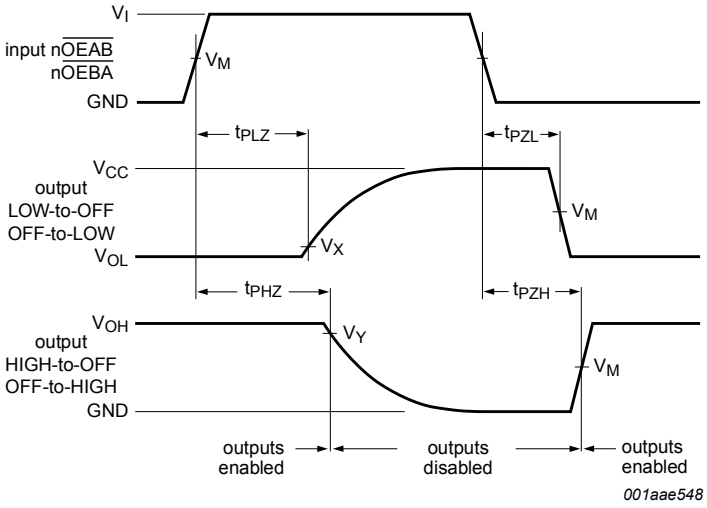
**Figure 6. Propagation delay clock input (nCPAB, nCPBA) to output (nBn, nAn), clock pulse width and maximum clock pulse frequency**




Measurements points are given in Table 8.

The shaded areas indicate when the input is permitted to change for predictable output performance.

**Figure 7. Setup and hold times**



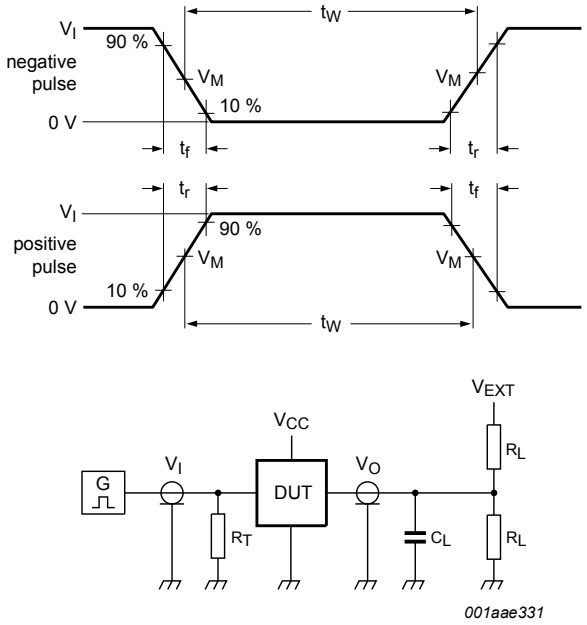

Measurements points are given in Table 8.

$V_{OL}$ and $V_{OH}$ are typical voltage output levels that occur with the output load.

**Figure 8. 3-state enable and disable time**

**Table 8. Measurement points**

| Supply voltage | Input | | Output | | |
|---|---|---|---|---|---|
| $V_{CC}$ | $V_I$ | $V_M$ | $V_M$ | $V_X$ | $V_Y$ |
| 2.3 V to 2.7 V | $V_{CC}$ | 0.5 V | 0.5 V | $V_{OL}$ + 0.15 V | $V_{OH}$ - 0.15 V |
| 2.7 V | 2.7 V | 1.5 V | 1.5 V | $V_{OL}$ + 0.3 V | $V_{OH}$ - 0.3 V |
| 3.0 V to 3.6 V | 2.7 V | 1.5 V | 1.5 V | $V_{OL}$ + 0.3 V | $V_{OH}$ - 0.3 V |




Test data is given in Table 9.

Definitions for test circuit:

$R_T$ = Termination resistance should be equal to output impedance $Z_o$ of the pulse generator.

$C_L$ = Load capacitance including jig and probe capacitance.

$R_L$ = Load resistance.

$V_{EXT}$ = External voltage for measuring switching times.

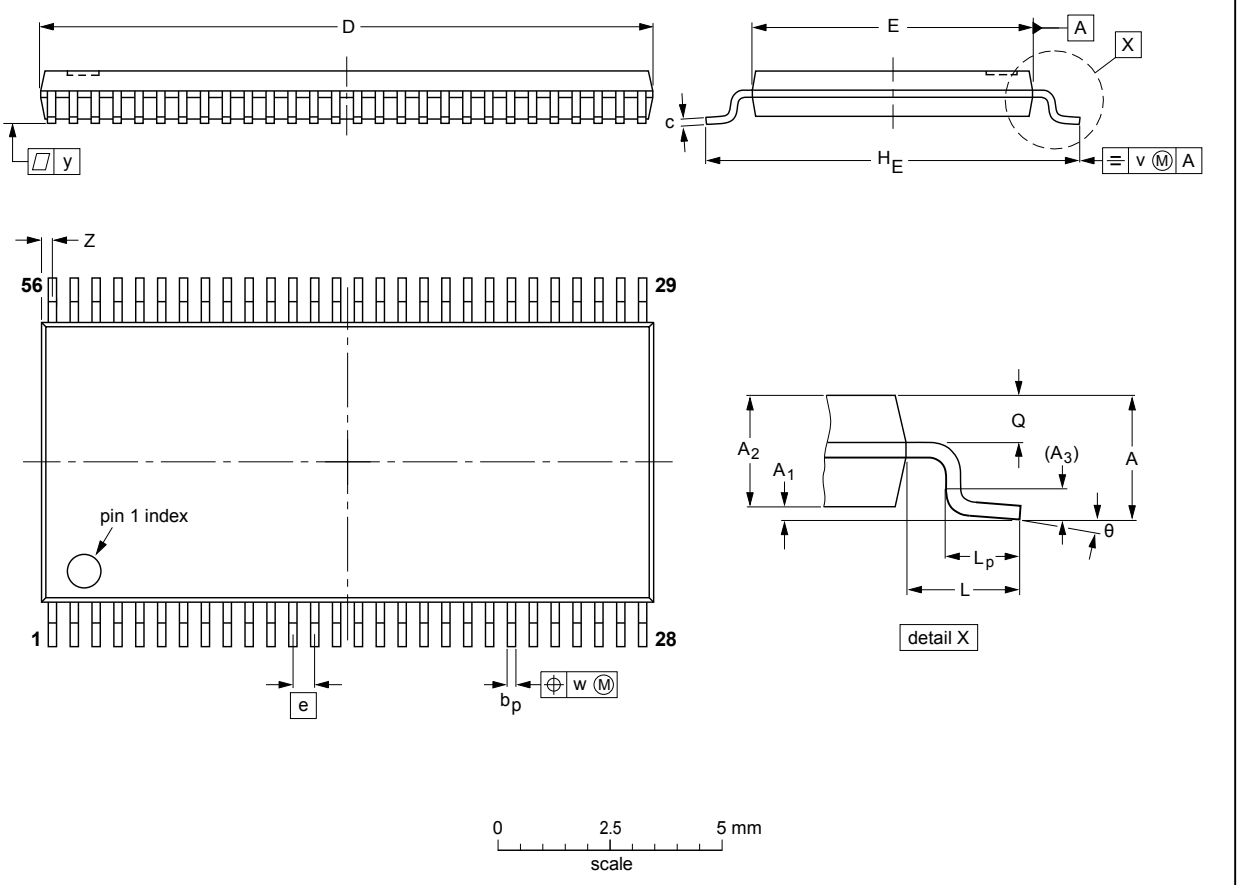
**Figure 9. Test circuit for measuring switching times**

**Table 9. Test data**

| Supply voltage | Input | | Load | | $V_{EXT}$ | | |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | $V_I$ | $t_r$, $t_f$ | $C_L$ | $R_L$ | $t_{PLH}$, $t_{PHL}$ | $t_{PLZ}$, $t_{PZL}$ | $t_{PHZ}$, $t_{PZH}$ |
| 2.3 V to 2.7 V | $V_{CC}$ | ≤ 2.0 ns | 30 pF | 500 Ω | open | 2 × $V_{CC}$ | GND |
| 2.7 V | 2.7 V | 2.5 ns | 50 pF | 500 Ω | open | 2 × $V_{CC}$ | GND |
| 3.0 V to 3.6 V | 2.7 V | 2.5 ns | 50 pF | 500 Ω | open | 2 × $V_{CC}$ | GND |

## 11 Package outline

**TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm** **SOT364-1**




**DIMENSIONS (mm are the original dimensions).**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(2)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.2 | 0.15<br>0.05 | 1.05<br>0.85 | 0.25 | 0.28<br>0.17 | **0.2**<br>**0.1** | 14.1<br>13.9 | 6.2<br>6.0 | 0.5 | 8.3<br>7.9 | 1 | 0.8<br>0.4 | 0.50<br>0.35 | 0.25 | 0.08 | 0.1 | 0.5<br>0.1 | $8^o$<br>$0^o$ |

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT364-1 | | MO-153 | | | | ~~99-12-27~~<br>03-02-19 |

**Figure 10. Package outline SOT364-1 (TSSOP56)**

## 12 Abbreviations

**Table 10. Abbreviations**

| Acronym | Description |
|---|---|
| CMOS | Complementary Metal-Oxide Semiconductor |
| DUT | Device Under Test |
| TTL | Transistor-Transistor Logic |

## 13 Revision history

**Table 11. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| 74ALVCH16952 v.3 | 20180109 | Product data sheet | - | 74ALVCH16952 v.2 |
| Modifications: | • The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.<br>• Legal texts have been adapted to the new company name where appropriate. | | | |
| 74ALVCH16952 v.2 | 20060427 | Product data sheet | - | 74ALVCH16952 v.1 |
| Modifications: | • The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors<br>• The symbol of pin numbers 15, 16, 17, 19, 20, 21, 23 and 24 is rectified | | | |
| 74ALVCH16952 v.1 | 19980901 | Preliminary specification | - | - |

## Contents





For more information, please visit: http://www.nexperia.com
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**Document identifier: 74ALVCH16952**