

# 74AHC2G125; 74AHCT2G125

Dual buffer/line driver; 3-state

Rev. 5 — 1 September 2023

Product data sheet

## 1. General description

The 74AHC2G125; 74AHCT2G125 is a dual buffer/line driver with 3-state outputs controlled by the output enable inputs ( $\overline{nOE}$ ). Inputs are overvoltage tolerant. This feature allows the use of these devices as translators in mixed voltage environments.

## 2. Features and benefits

- Symmetrical output impedance
- Balanced propagation delays
- Wide supply voltage range from 2.0 to 5.5 V
- Overvoltage tolerant inputs to 5.5 V
- Input levels:
  - For 74AHC2G125: CMOS level
  - For 74AHCT2G125: TTL level
- High noise immunity
- CMOS low power dissipation
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level A
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +125 °C

## 3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
<a href="#">74AHC2G125DP</a> <a href="#">74AHCT2G125DP</a>	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	<a href="#">SOT505-2</a>
<a href="#">74AHC2G125DC</a> <a href="#">74AHCT2G125DC</a>	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	<a href="#">SOT765-1</a>

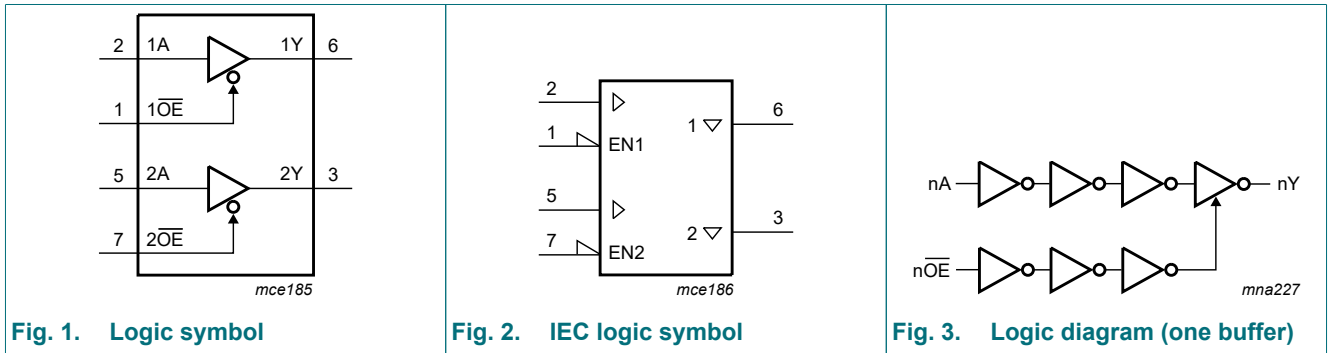
## 4. Marking

Table 2. Marking codes

Type number	Marking <sup>[1]</sup>
74AHC2G125DP	A25
74AHCT2G125DP	C25
74AHC2G125DC	A25
74AHCT2G125DC	C25

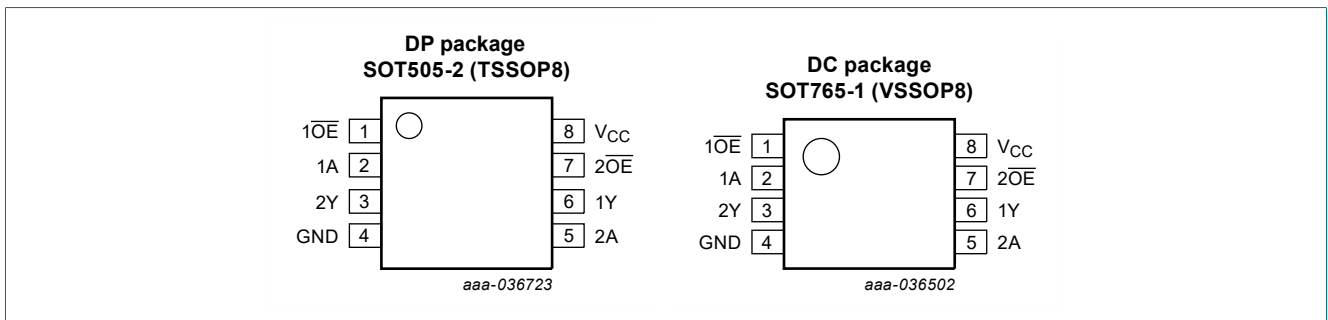
[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

## 5. Functional diagram



## 6. Pinning information

### 6.1. Pinning



### 6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
1OE, 2OE	1, 7	output enable input (active LOW)
1A, 2A	2, 5	data input
GND	4	ground (0 V)
1Y, 2Y	6, 3	data output
V <sub>CC</sub>	8	supply voltage

## 7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Control	Input	Output
nOE	nA	nY
L	L	L
L	H	H
H	X	Z

## 8. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$V_I$	input voltage		-0.5	+7.0	V
$I_{IK}$	input clamping current	$V_I < -0.5$ V [1]	-20	-	mA
$I_{OK}$	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V [1]	-	±20	mA
$I_O$	output current	$-0.5$ V < $V_O$ < $V_{CC} + 0.5$ V	-	±25	mA
$I_{CC}$	supply current		-	75	mA
$I_{GND}$	ground current		-75	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C [2]	-	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT505-2 (TSSOP8) package:  $P_{tot}$  derates linearly with 4.6 mW/K above 96 °C.

For SOT765-1 (VSSOP8) package:  $P_{tot}$  derates linearly with 4.9 mW/K above 99 °C.

## 9. Recommended operating conditions

**Table 6. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74AHC2G125			74AHCT2G125			Unit
			Min	Typ	Max	Min	Typ	Max	
$V_{CC}$	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
$V_I$	input voltage		0	-	5.5	0	-	5.5	V
$V_O$	output voltage		0	-	$V_{CC}$	0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 3.3$ V ± 0.3 V	-	-	100	-	-	-	ns/V
		$V_{CC} = 5.0$ V ± 0.5 V	-	-	20	-	-	20	ns/V

## 10. Static characteristics

**Table 7. Static characteristics**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74AHC2G125</b>										
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 2.0$ V	1.5	-	-	1.5	-	1.5	-	V
		$V_{CC} = 3.0$ V	2.1	-	-	2.1	-	2.1	-	V
		$V_{CC} = 5.5$ V	3.85	-	-	3.85	-	3.85	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 2.0$ V	-	-	0.5	-	0.5	-	0.5	V
		$V_{CC} = 3.0$ V	-	-	0.9	-	0.9	-	0.9	V
		$V_{CC} = 5.5$ V	-	-	1.65	-	1.65	-	1.65	V

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = -50 µA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I <sub>O</sub> = -50 µA; V <sub>CC</sub> = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I <sub>O</sub> = -50 µA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 3.0 V	2.58	-	-	2.48	-	2.40	-	V
		I <sub>O</sub> = -8.0 mA; V <sub>CC</sub> = 4.5 V	3.94	-	-	3.8	-	3.70	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = 50 µA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 50 µA; V <sub>CC</sub> = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 50 µA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
		I <sub>O</sub> = 8.0 mA; V <sub>CC</sub> = 4.5 V	-	-	0.36	-	0.44	-	0.55	V
I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	-	-	0.25	-	2.5	-	10	µA
I <sub>I</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	µA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	1.0	-	10	-	40	µA
C <sub>I</sub>	input capacitance		-	1.5	10	-	10	-	10	pF
<b>74AHCT2G125</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = -50 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -8.0 mA	3.94	-	-	3.8	-	3.70	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = 50 µA	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 8.0 mA	-	-	0.36	-	0.44	-	0.55	V
I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	-	-	0.25	-	2.5	-	10	µA
I <sub>I</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	µA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	1.0	-	10	-	40	µA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>I</sub> = 3.4 V; other inputs at V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
C <sub>I</sub>	input capacitance		-	1.5	10	-	10	-	10	pF

## 11. Dynamic characteristics

**Table 8. Dynamic characteristics**

$GND = 0\text{ V}$ ; for test circuit see Fig. 6.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	Min	Max	
<b>74AHC2G125</b>										
$t_{pd}$	propagation delay	nA to nY; see Fig. 4 [2]								
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}; C_L = 15\text{ pF}$	-	4.7	8.0	1.0	9.5	1.0	11.5	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}; C_L = 50\text{ pF}$	-	6.6	11.5	1.0	13.0	1.0	14.5	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}; C_L = 15\text{ pF}$	-	3.4	5.5	1.0	6.5	1.0	7.0	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}; C_L = 50\text{ pF}$	-	4.8	7.5	1.0	8.5	1.0	9.5	ns
$t_{en}$	enable time	n $\overline{OE}$ to nY; see Fig. 5 [2]								
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}; C_L = 15\text{ pF}$	-	5.0	8.0	1.0	9.5	1.0	11.5	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}; C_L = 50\text{ pF}$	-	6.9	11.5	1.0	13.0	1.0	14.5	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}; C_L = 15\text{ pF}$	-	3.6	5.1	1.0	6.0	1.0	6.5	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}; C_L = 50\text{ pF}$	-	4.9	7.5	1.0	8.5	1.0	9.5	ns
$t_{dis}$	disable time	n $\overline{OE}$ to nY; see Fig. 5 [2]								
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}; C_L = 15\text{ pF}$	-	6.0	9.7	1.0	11.5	1.0	12.5	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}; C_L = 50\text{ pF}$	-	8.3	13.2	1.0	15.0	1.0	16.5	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}; C_L = 15\text{ pF}$	-	4.1	6.8	1.0	8.0	1.0	8.5	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}; C_L = 50\text{ pF}$	-	5.7	8.8	1.0	10.0	1.0	11.0	ns
$C_{PD}$	power dissipation capacitance	per buffer; $C_L = 50\text{ pF}; f_i = 1\text{ MHz}; [3]$ $V_i = GND\text{ to }V_{CC}$	-	9	-	-	-	-	-	pF
<b>74AHCT2G125</b>										
$t_{pd}$	propagation delay	nA to nY; see Fig. 4 [2]								
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}; C_L = 15\text{ pF}$	-	3.4	5.5	1.0	6.5	1.0	6.5	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}; C_L = 50\text{ pF}$	-	4.8	7.5	1.0	8.5	1.0	8.5	ns
$t_{en}$	enable time	n $\overline{OE}$ to nY; see Fig. 5 [2]								
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}; C_L = 15\text{ pF}$	-	3.9	5.1	1.0	6.0	1.0	6.0	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}; C_L = 50\text{ pF}$	-	5.1	7.5	1.0	8.5	1.0	8.5	ns
$t_{dis}$	disable time	n $\overline{OE}$ to nY; see Fig. 5 [2]								
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}; C_L = 15\text{ pF}$	-	4.5	6.8	1.0	8.0	1.0	8.0	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}; C_L = 50\text{ pF}$	-	6.1	8.8	1.0	10.0	1.0	10.0	ns
$C_{PD}$	power dissipation capacitance	per buffer; $C_L = 50\text{ pF}; f_i = 1\text{ MHz}; [3]$ $V_i = GND\text{ to }V_{CC}$	-	11	-	-	-	-	-	pF

[1] Typical values are measured at  $T_{amb} = 25\text{ °C}$  and  $V_{CC} = 3.3\text{ V}$  and  $5.0\text{ V}$  respectively.

[2]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ ;  $t_{en}$  is the same as  $t_{PZL}$  and  $t_{PZH}$ ;  $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ .

[3]  $C_{PD}$  is used to determine the dynamic power dissipation  $P_D$  ( $\mu\text{W}$ ).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in Volts.

11.1. Waveforms and test circuit

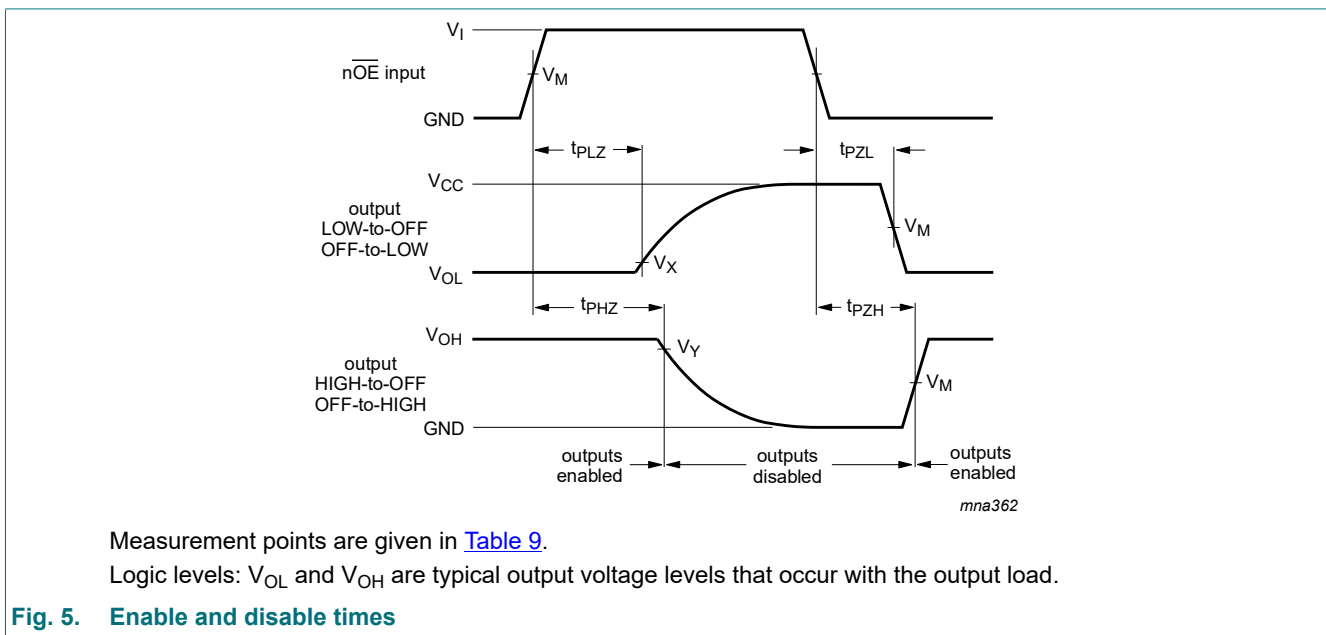
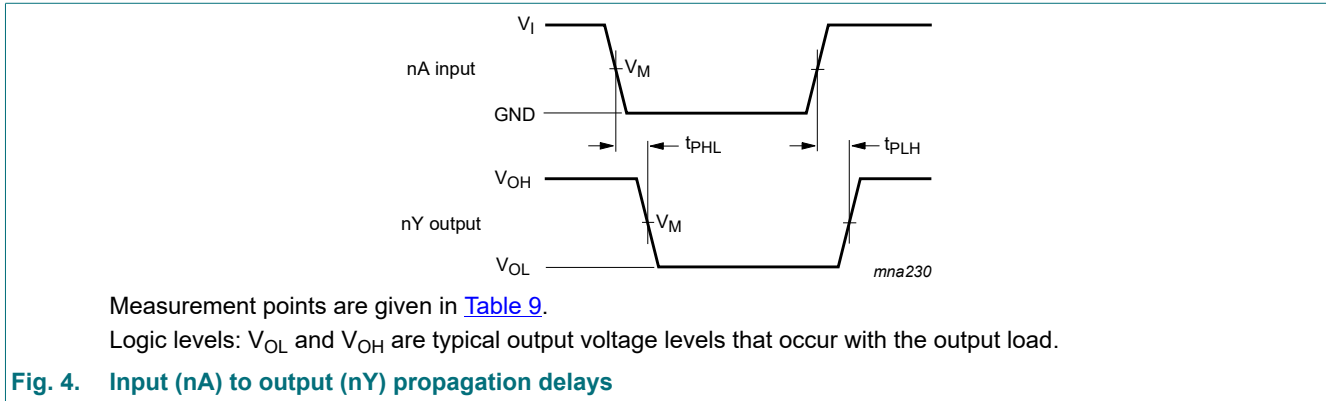


Table 9. Measurement points

Type	Input	Output		
	$V_M$	$V_M$	$V_X$	$V_Y$
74AHC2G125	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$
74AHCT2G125	1.5 V	$0.5V_{CC}$	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$

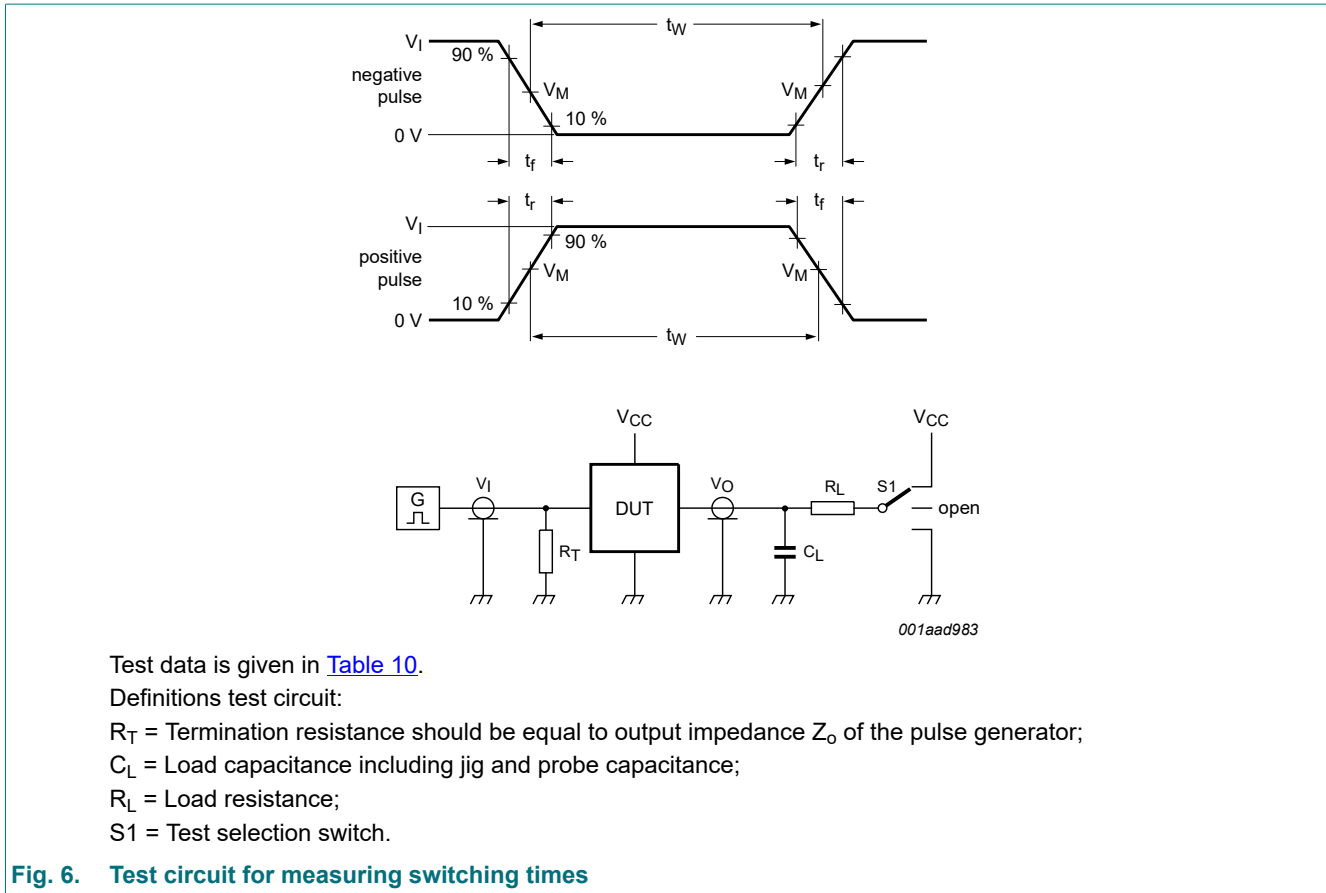


Table 10. Test data

Type	Input		Load		S1 position		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$
74AHC2G125	$V_{CC}$	$\leq 3$ ns	15 pF, 50 pF	1 k $\Omega$	open	GND	$V_{CC}$
74AHCT2G125	3 V	$\leq 3$ ns	15 pF, 50 pF	1 k $\Omega$	open	GND	$V_{CC}$

12. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2

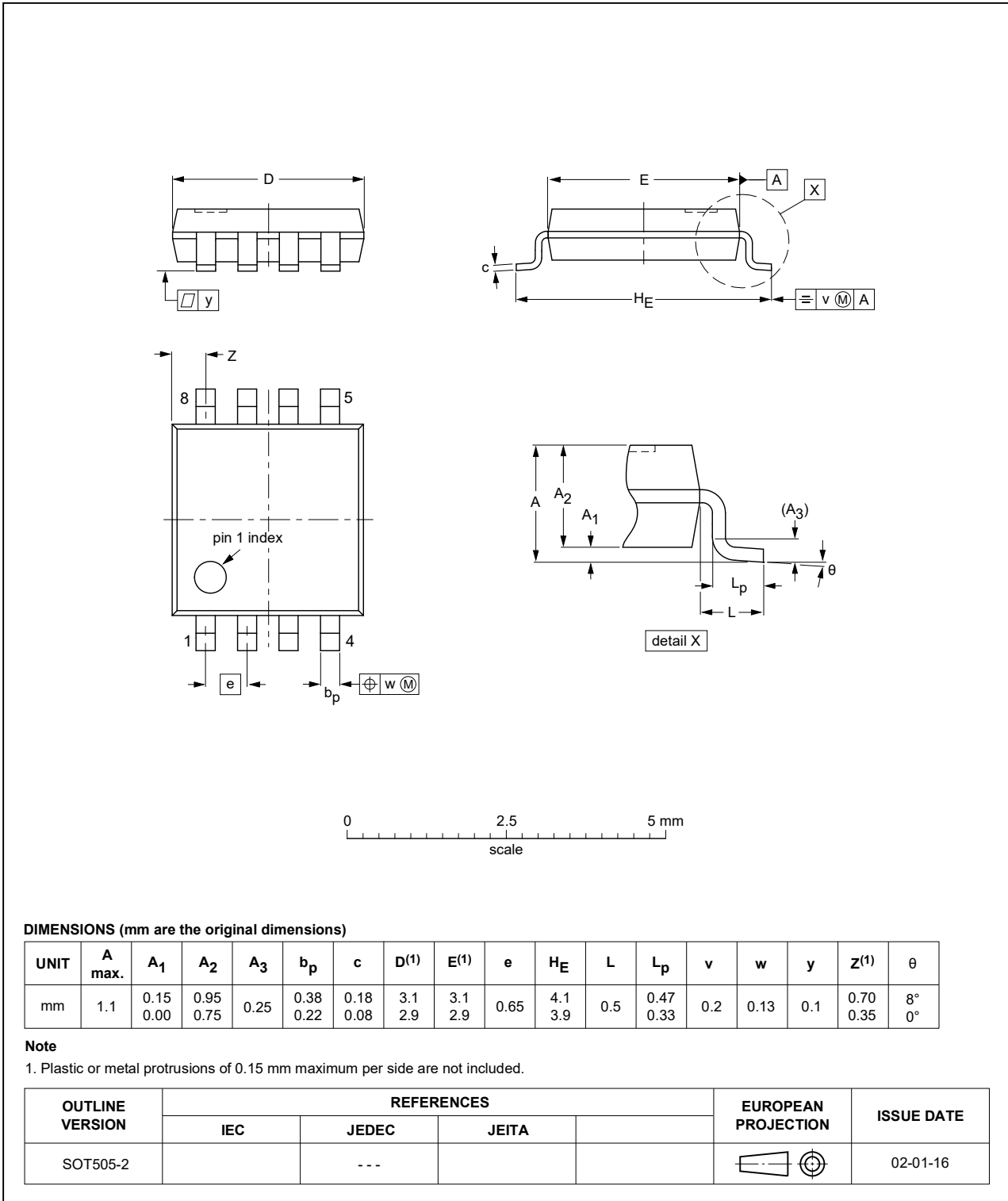


Fig. 7. Package outline SOT505-2 (TSSOP8)



VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1

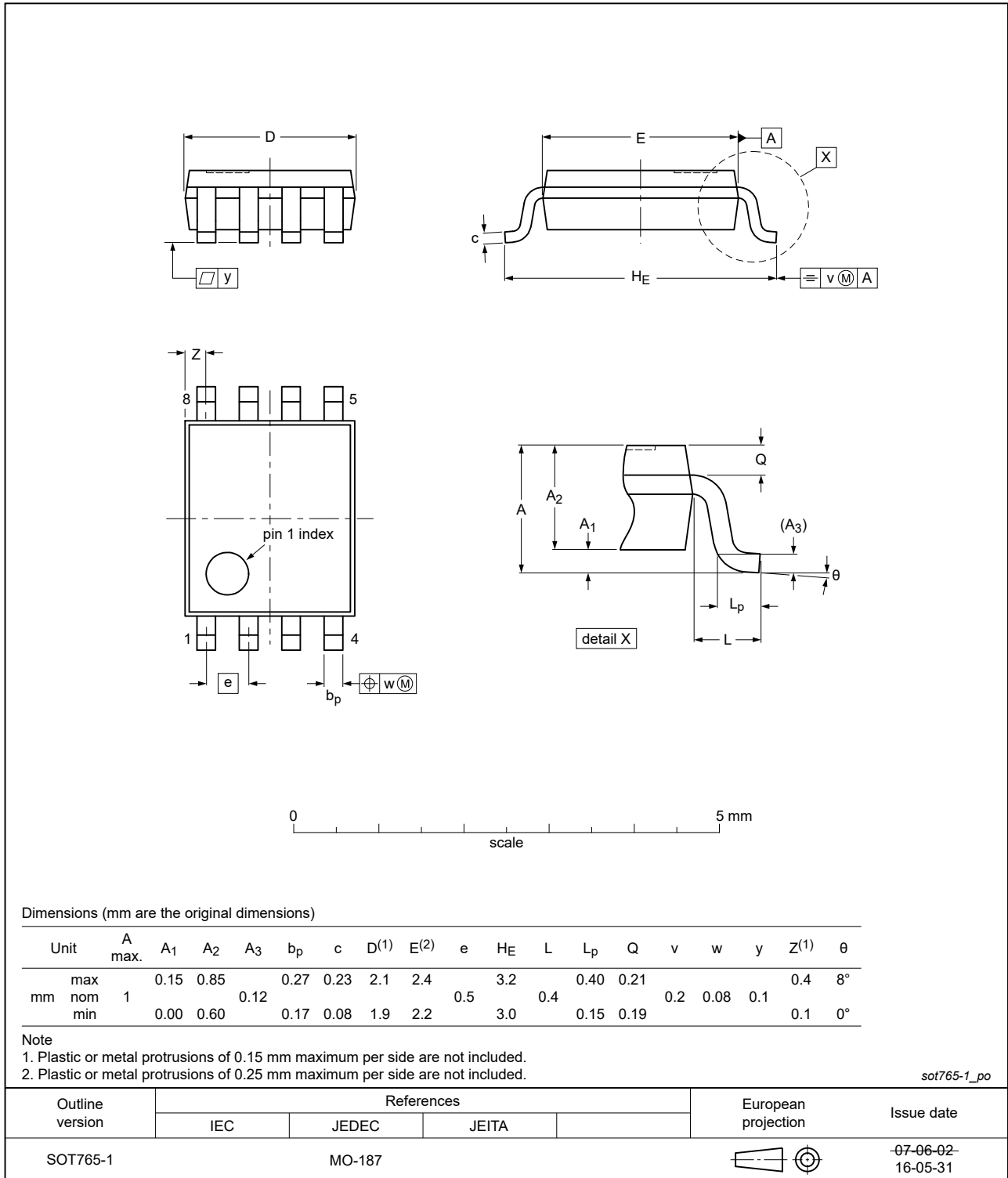


Fig. 8. Package outline SOT765-1 (VSSOP8)

## 13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT2G125 v.5	20230901	Product data sheet	-	74AHC_AHCT2G125 v.4
Modifications:	<ul style="list-style-type: none"> <li>• <a href="#">Section 1</a> and <a href="#">Section 2</a> updated.</li> <li>• <a href="#">Section 2</a>: ESD specification updated according to the latest JEDEC standard.</li> <li>• <a href="#">Section 8</a>: Derating values for <math>P_{tot}</math> total power dissipation updated.</li> </ul>			
74AHC_AHCT2G125 v.4	20190102	Product data sheet	-	74AHC_AHCT2G125 v.3
Modifications:	<ul style="list-style-type: none"> <li>• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>• Legal texts have been adapted to the new company name where appropriate.</li> <li>• Type numbers 74AHC2G125GD and 74AHCT2G125GD (SOT996-2) removed.</li> <li>• Package outline drawing <a href="#">SOT765-1</a> (VSSOP8) updated.</li> </ul>			
74AHC_AHCT2G125 v.3	20130506	Product data sheet	-	74AHC_AHCT2G125 v.2
Modifications:	<ul style="list-style-type: none"> <li>• For type number 74AHC2G125GD and 74AHCT2G125GD XSON8U has changed to XSON8.</li> </ul>			
74AHC_AHCT2G125 v.2	20081222	Product data sheet	-	74AHC_AHCT2G125 v.1
Modifications:	<ul style="list-style-type: none"> <li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>• Legal texts have been adapted to the new company name where appropriate.</li> <li>• Added type number 74AHC2G125GD and 74AHCT2G125GD (XSON8U package).</li> </ul>			
74AHC_AHCT2G125 v.1	20040113	Product specification	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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