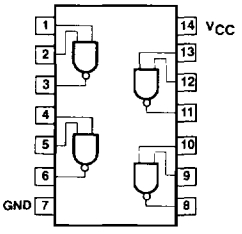
Quad two-input NAND gate — 54F00

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	PACKAGE DESIGNATOR*
14-Pin Ceramic DIP	54F00/BCA	GDIP1-T14
14-Pin Ceramic Flat Pack	54F00/BDA	GDFP1-F14
20-Pin Ceramic LLCC	54F00/B2A	CQCC2-N20

* MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

PIN CONFIGURATION

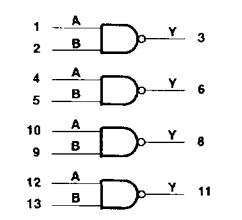


ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

LOGIC SYMBOL



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A, B	Inputs	1.0/1.0	20μA/0.6mA
$\overline{Y}$	Output	50/33	1.0mA/20mA

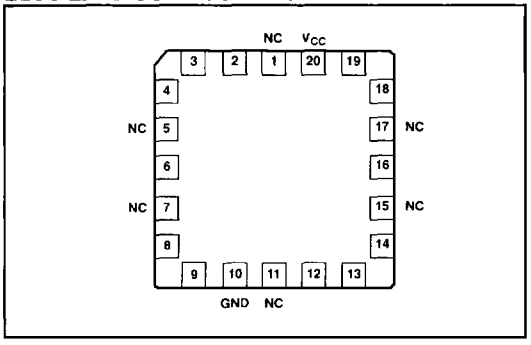
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

FUNCTION TABLE

INPUTS		OUTPUT
A	B	$\overline{Y}$
L	L	H
L	H	H
H	L	H
H	H	L

H = High voltage level
L = Low voltage level

LLCC LEAD CONFIGURATION



DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OH} = Max, V_{IH} = Min		2.5			V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OL} = Max, V_{IH} = Min			0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage		V_{CC} = Max, V_I = 7.0V				100	µA
I_{IH1}	High-level input current		V_{CC} = Max, V_I = 2.7V			1	20	µA
I_{IL}	Low-level input current		V_{CC} = Max, V_I = 0.5V			-0.4	-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = Max, V_O = 0.0V		-60	-80	-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = Max	V_I = GND		1.9	2.8	mA
		I_{CCL}		$V_I \geq$ 4.0V		6.8	10.2	mA

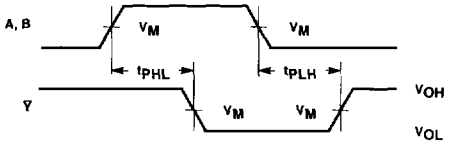
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay A, B to $\overline{Y}$	Waveform 1	2.4 2.0	3.7 3.2	5.0 4.3	2.0 1.2	7.0 6.5	ns ns

NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

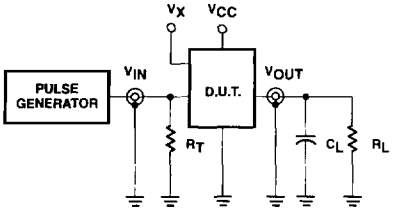
AC WAVEFORMS



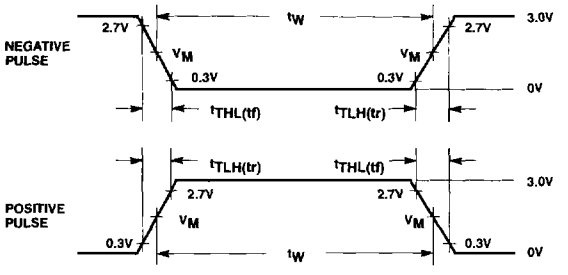
NOTE: For all waveforms, $V_M = 1.5V$.

Waveform 1. For Inverting Outputs

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per FunctionTable.

INPUT PULSE CHARACTERISTICS				
Family	**Rep. Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
54F	1MHz	500ns	≤2.5ns	≤2.5ns