# Signetics

Military Logic Products

# 54LS273, 54S273
## Flip-Flops

**Octal D Flip-Flops**

***Product Specification***

### FEATURES

- **Ideal buffer for MOS microprocessor or memory**
- **Eight edge-triggered D flip-flops**
- **High-speed Schottky version available**
- **Buffered common clock**
- **Buffered, asynchronous Master Reset**
- **Slim 20-pin plastic and ceramic DIP packages**
- **See '377 for Clock Enable version**
- **See '373 for transparent latch version**
- **See '374 for 3-State version**

### DESCRIPTION

The '273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge triggered. The state of each D input, one setup time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced Low independently of Clock or Data inputs by a Low voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

### ORDERING INFORMATION

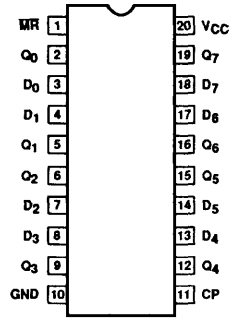
| DESCRIPTION | ORDER CODE |
|---|---|
| 20-Pin Ceramic DIP | 54LS273/BRA<br>54S273/BRA |
| 20-Pin Ceramic FlatPack | 54LS273/BSA<br>54S273/BSA |
| 20-Pin Ceramic LLCC | 54LS273/B2A<br>54S273/B2A |

### INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 54S | 54LS |
|---|---|---|---|
| All | Inputs | 1SUL | 1LSUL |
| All | Outputs | 10SUL | 10LSUL |

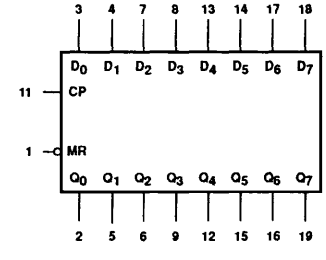
**NOTE:** A 54S Unit Load (SUL) is 50μA $I_{IH}$ and -2.0mA $I_{IL}$ and a 54LS Unit Load (LSUL) is 20μA $I_{IH}$ and -0.4mA $I_{IL}$.

### PIN CONFIGURATION




For LLCC Pin Assignments, see JEDEC Standard No. 2

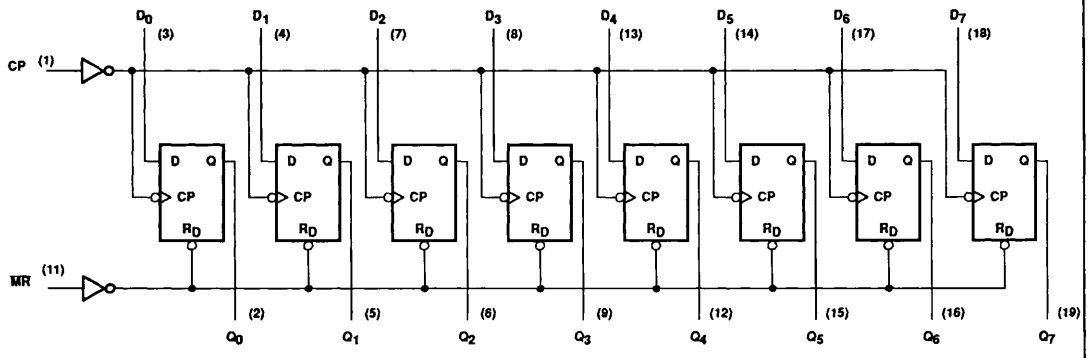
### LOGIC SYMBOL




VCC = Pin 20
GND = Pin 10

For LLCC Pin Assignments, see JEDEC Standard No. 2

## LOGIC DIAGRAM




$V_{CC}$ = Pin 20
GND = Pin 10
( ) = Pin number

For LLCC pin assignments, see JEDEC Standard No. 2

## MODE SELECT — FUNCTION TABLE

| OPERATING MODE | INPUTS | | | OUTPUTS |
|---|---|---|---|---|
| | $\overline{MR}$ | CP | $D_n$ | $Q_n$ |
| Reset (clear) | L | X | X | L |
| Load "1" | H | ↑ | h | H |
| Load "0" | H | ↑ | l | L |

H = High voltage level steady state.
h = High voltage level one setup time prior to the Low-to-High Clock transition.
L = Low voltage level steady state.
l = Low voltage level one setup time prior to the Low-to-High Clock transition.
X = Don't Care.
↑ = Low-to-High clock transition.

## ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

| SYMBOL | PARAMETER | 54LS | 54S | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 7.0 | 7.0 | V |
| $V_I$ | Input voltage range | -0.5 to +7.0 | -0.5 to +5.5 | V |
| $I_I$ | Input current range | -30 to +1 | -30 to +5 | mA |
| $V_O$ | Voltage applied to output in High output state range | -0.5 to +$V_{CC}$ | -0.5 to +$V_{CC}$ | V |
| $T_{STG}$ | Storage temperature range | -65 to +150 | -65 to +150 | °C |

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | | 54LS | | | 54S | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5.0 | 5.5 | 4.5 | 5.0 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2.0 | | | 2.0 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | +0.7 | | | +0.8 | V |
| | | +125°C | | | +0.7 | | | +0.7 | V |
| $I_{IK}$ | Input clamp current | | | | -18 | | | -18 | mA |
| $I_{OH}$ | High-level output current | | | | -400 | | | -1000 | µA |
| $I_{OL}$ | Low-level output current | | | | 4 | | | 20 | mA |
| $T_A$ | Operating free-air temperature range | | -55 | | +125 | -55 | | +125 | °C |

## DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

| SYMBOL | PARAMETER | TEST CONDITIONS[1] | | 54LS273 | | | 54S273 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ[2] | Max | Min | Typ[2] | Max | |
| $V_{OH}$ | High-level output voltage | $V_{CC}$ = Min, $V_{IH}$ = Min, $V_{IL}$ = Max, $I_{OH}$ = Max | | 2.5 | 3.4 | | 2.5 | | | V |
| $V_O$ | Low-level output voltage | $V_{CC}$ = Min, $V_{IH}$ = Min, $V_{IL}$ = Max, | | | 0.25 | 0.4 | | | 0.5 | V |
| | | $I_{OL}$ = Max | +125°C | | | 0.4 | | | 0.45 | V |
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = Min, $I_I$ = $I_{IK}$ | | | | -1.5 | | | -1.2 | V |
| $I_{IH2}$ | Input current at maximum | $V_{CC}$ = Max | $V_I$ = 5.5V | | | | | | 1.0 | mA |
| | input voltage | | $V_I$ = 7.0V | | | 0.1 | | | | mA |
| $I_{IH1}$ | High-level input current | $V_{CC}$ = Max, $V_I$ = 2.7V | | | | 20 | | | 50 | µA |
| $I_{IL}$ | Low-level input current | $V_{CC}$ = Max | $V_I$ = 0.4V | | | -0.4 | | | | mA |
| | | | $V_I$ = 0.5V | | | | | | -2.0 | mA |
| $I_{OS}$ | Short-circuit output current[3] | $V_{CC}$ = Max | | -20 | | -100 | -40 | | -100 | mA |
| $I_{CC}$ | Supply current[4] (total) | $V_{CC}$ = Max | | | 17 | 27 | | 109 | 150 | mA |

## AC ELECTRICAL CHARACTERISTICS $T_A$ = 25°C, $V_{CC}$ = 5.0V[5]

| SYMBOL | PARAMETER | TEST CONDITIONS | 54LS | | 54S | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | $C_L$ = 15pF | | $C_L$ = 15pF | | |
| | | | Min | Max | Min | Max | |
| $f_{MAX}$ | Maximum clock frequency | Waveform 1 | 30 | | 75 | | MHz |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>Clock to output | Waveform 1 | | 27<br>27 | | 15<br>15 | ns<br>ns |
| $t_{PHL}$ | Propagation delay, $\overline{MR}$ to output | Waveform 2 | | 27 | | 15 | ns |

## AC SETUP REQUIREMENTS $T_A$ = 25°C, $V_{CC}$ = 5.0V

| SYMBOL | PARAMETER | TEST CONDITIONS | 54LS | | 54S | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $t_W(L)$ | Clock pulse width (Low) | Waveform 1 | 20 | | 7.0 | | ns |
| $t_W$ | Master Reset pulse width | Waveform 2 | 20 | | 10 | | ns |
| $t_s(H)$ | Setup time, High data to CP | Waveform 3 | 20 | | 5.0 | | ns |
| $t_h(H)$ | Hold time, High data to CP | Waveform 3 | 5.0 | | 3.0 | | ns |
| $t_s(L)$ | Setup time, Low data to CP | Waveform 3 | 20 | | 5.0 | | ns |
| $t_h(L)$ | Hold time, Low data to CP | Waveform 3 | 5.0 | | 3.0 | | ns |
| $t_{rec}$ | Recovery time, MR to CP | Waveform 2 | 25 | | 5.0 | | ns |

## AC ELECTRICAL CHARACTERISTICS $T_A$ = 25°C, $V_{CC}$ = 5.0V

| SYMBOL | PARAMETER | TEST CONDITIONS | 54LS | | 54S | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | $C_L$ = 50pF | | $C_L$ = 50pF | | |
| | | | Min | Max | Min | Max | |
| $f_{MAX}$ | Maximum clock frequency | Waveform 1 | 30 | | 75 | | MHz |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>Clock to output | Waveform 1 | | 32<br>32 | | 17.5<br>17.5 | ns<br>ns |
| $t_{PHL}$ | Propagation delay, $\overline{MR}$ to output | Waveform 2 | | 32 | | 17.5 | ns |

## AC ELECTRICAL CHARACTERISTICS $T_A$ = -55°C and +125°C, $V_{CC}$ = 5.0V[5]

| SYMBOL | PARAMETER | TEST CONDITIONS | 54LS | | 54S | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | $C_L$ = 50pF | | $C_L$ = 50pF | | |
| | | | Min | Max | Min | Max | |
| $f_{MAX}$ | Maximum clock frequency | Waveform 1 | 30 | | 75 | | MHz |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>Clock to output | Waveform 1 | | 42<br>42 | | 23<br>23 | ns<br>ns |
| $t_{PLH}$ | Propagation delay $\overline{MR}$ to output | Waveform 2 | | 42 | | 23 | ns |

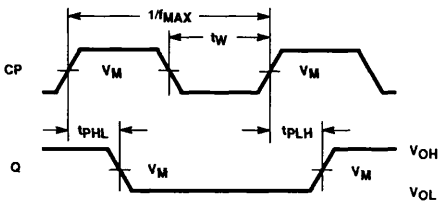
## AC SETUP REQUIREMENTS $T_A$ = -55°C and +125°C, $V_{CC}$ = 5.0V[5]

| SYMBOL | PARAMETER | TEST CONDITIONS | 54LS | | 54S | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $t_W(L)$ | Clock pulse width (Low) | Waveform 1 | 20 | | 7.0 | | ns |
| $t_W$ | Master Reset pulse width | Waveform 2 | 20 | | 10 | | ns |
| $t_s(H)$ | Setup time, High data to CP | Waveform 3 | 20 | | 5.0 | | ns |
| $t_h(H)$ | Hold time, High data to CP | Waveform 3 | 5.0 | | 3.0 | | ns |
| $t_s(L)$ | Setup time, Low data to CP | Waveform 3 | 20 | | 5.0 | | ns |
| $t_h(L)$ | Hold time, Low data to CP | Waveform 3 | 5.0 | | 3.0 | | ns |
| $t_{rec}$ | Recovery time, MR to CP | Waveform 2 | 25 | | 5.0 | | ns |

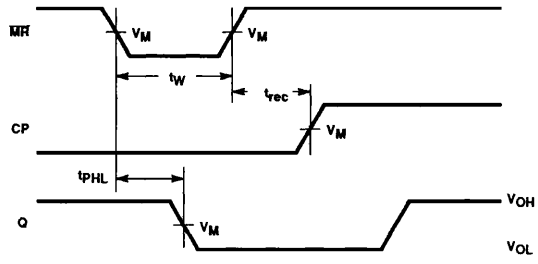
**NOTES:**

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at $V_{CC}$ = 5V, $T_A$ = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure $I_{CC}$ after a momentary ground, then ≥4.0V is applied to clock with all outputs open and ≥4.0V applied to all Data inputs and the Master Reset input.
5. These parameters are guaranteed, but not tested.

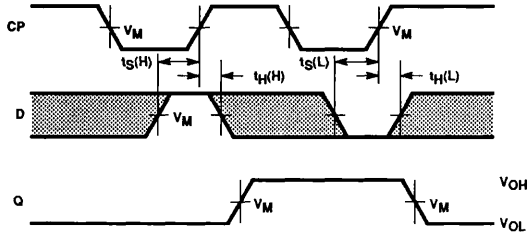
## AC WAVEFORMS




**Waveform 1. Clock to Output Delays and Clock Pulse Width**



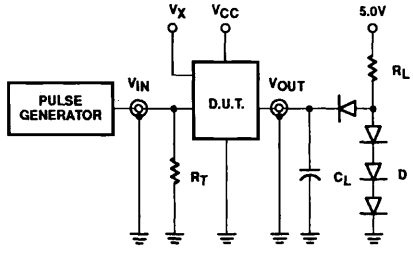

**Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time**



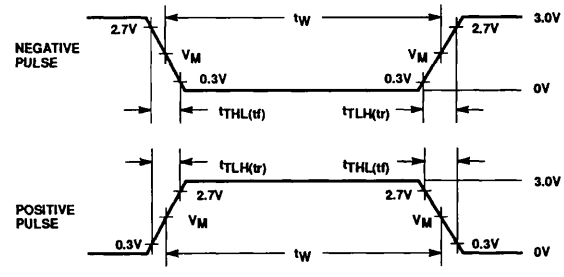

**Waveform 3. Data Setup and Hold Times**

NOTE: $V_M$ = 1.5V for 54S; $V_M$ = 1.3V for 54LS
The shaded areas indicate when the input is permitted to change for predictable output performance.

## TEST CIRCUIT AND WAVEFORM




Test Circuit for 54 Totem-Pole Outputs




Input Pulse Definition

| FAMILY | INPUT PULSE CHARACTERISTICS | | | | | |
|---|---|---|---|---|---|---|
| | $R_L$ | $V_M$ | Rep. Rate | $T_W$ | $T_{TLH}$ | $T_{THL}$ |
| 54LSXXX | 2.0kΩ | 1.3V | 1MHz | 500ns | ≤15ns | ≤6ns |
| 54SXXX | 280Ω | 1.5V | 1MHz | 500ns | ≤2.5ns | ≤2.5ns |

**DEFINITIONS:**
$C_L$ = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
$R_T$ = Termination resistance should be equal to $Z_{OUT}$ of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
$V_X$ = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.