

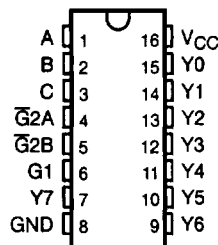
SN74LVC137

3-LINE TO 8-LINE DECODER/DEMULTIPLEXER WITH ADDRESS LATCHES

SCAS340A – MARCH 1994 – REVISED JULY 1995

- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Inputs Accept Voltages to 5.5 V
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This 3-line to 8-line decoder/demultiplexer with latches on three address inputs is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC137 is designed for high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, this decoder can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

When the latch-enable ($\overline{G2A}$) input is low, the SN74LVC137 acts as a decoder/demultiplexer. When $\overline{G2A}$ transitions from low to high, the address present at the inputs (A, B, and C) is stored in the latches. Further address changes are ignored provided $\overline{G2A}$ remains high. The output-enable (G1 and $\overline{G2B}$) inputs control the outputs independently of the select or latch-enable inputs. All of the outputs are forced high if G1 is low or $\overline{G2B}$ is high.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices in a mixed 3.3-V/5-V system environment.

The SN74LVC137 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

LATCH ENABLE	OUTPUT- ENABLE		SELECT INPUTS			OUTPUTS								
	$\overline{G2A}$	G1	$\overline{G2B}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H	H
L	H	L	L	H	L	H	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	Outputs corresponding to stored address = L; all other outputs = H								

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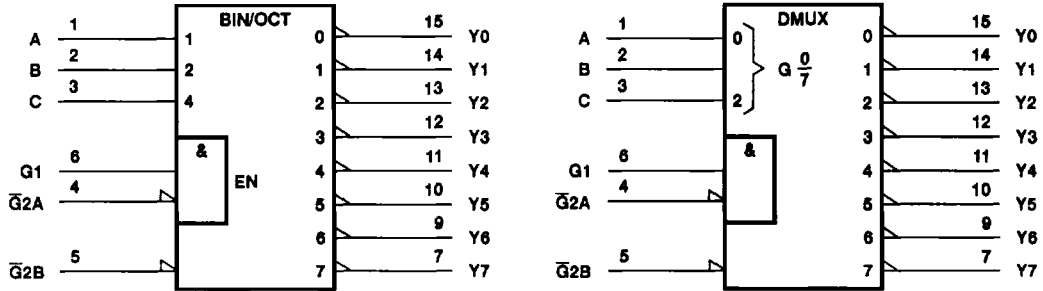
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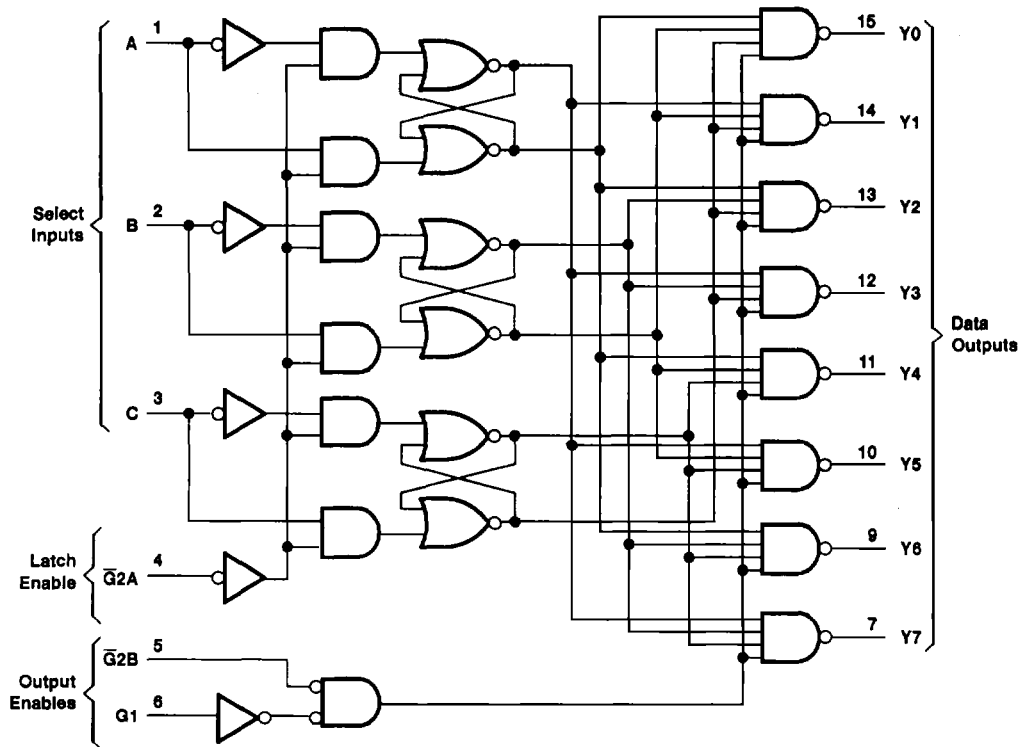
logic symbols (alternatives)†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	-0.5 V to 6.5 V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3): D package	1.3 W
DB package	0.55 W
PW package	0.5 W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.
 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_I	Input voltage	0	5.5	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7$ V		-12
		$V_{CC} = 3$ V		-24
I_{OL}	Low-level output current	$V_{CC} = 2.7$ V		12
		$V_{CC} = 3$ V		24
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	-40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} †	MIN	TYP‡	MAX	UNIT
V _{OH}	I _{OH} = -100 µA	MIN to MAX	V _{CC} -0.2			V
	I _{OH} = -12 mA	2.7 V	2.2			
		3 V	2.4			
	I _{OH} = -24 mA	3 V	2.2			
V _{OL}	I _{OL} = 100 µA	MIN to MAX			0.2	V
	I _{OL} = 12 mA	2.7 V			0.4	
	I _{OL} = 24 mA	3 V			0.55	
I _I	V _I = 5.5 V or GND	3.6 V			±5	µA
I _{OZ}	V _O = V _{CC} or GND	3.6 V			±10	µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V			10	µA
ΔI _{CC}	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V			500	µA
C _i	V _I = V _{CC} or GND	3.3 V				pF
C _o	V _O = V _{CC} or GND	3.3 V				pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

‡ Typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.

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