# 8-Bit Dual Supply Bus Transceiver with Configurable Output Voltage and 3-State Outputs

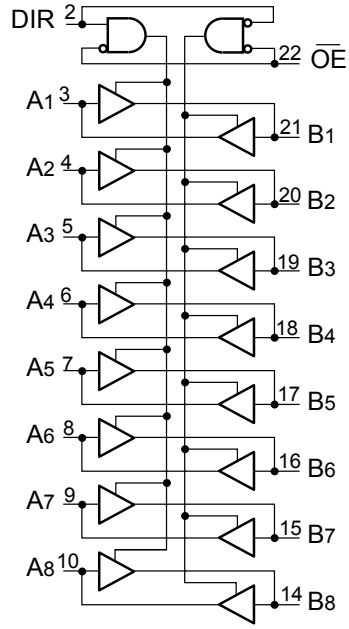
## Product Features

- 4.5V to 5.5V on A-port and 2.7V to 5.5V on B-port
- Latch-up performance exceeds 200mA Per JESD78
- ESD protection exceeds JESD 22
  - 2000V Human-Body Model (A114-B)
  - 200V Machine Model (A115-A)
- Industrial Temperature: –40°C to +85°C
- Packages (Pb-free & Green available):
  - 24-pin 173-mil wide plastic TSSOP (L)
  - 24-pin 150-mil wide plastic QSOP (Q)
  - 24-pin 300-mil wide plastic SOIC (S)

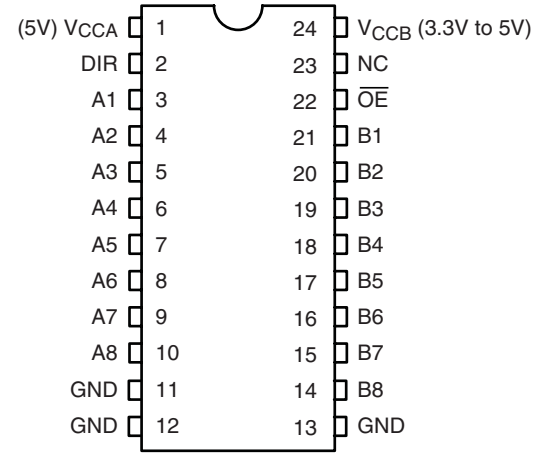
## Product Description

The PI74LVCC4245A is a non-inverting 8-bit Bidirectional Transceiver that uses two separate power supply rails. A-port ($V_{CCA}$) is set to operate at 5V and B-port ($V_{CCB}$) is set to operate from 3.3V to 5V. This allows for translation from a 3.3V to a 5V environment and vice-versa. This tranceiver is designed for asynchronous two-way communication between data buses. The direction control input pin (DIR) determines the dataflow from the A bus to the B bus or from the B bus to the A bus. The output enable ($\overline{OE}$) input, when HIGH, disables both A and B ports by placing them in HIGH Z condition.

## Logic Block Diagram




## Product Pin Configuration




## Truth Table[1]

| Inputs | | Outputs |
|---|---|---|
| $\overline{OE}$ | DIR | |
| L | L | Bus B Data to Bus A |
| L | H | Bus A Data to Bus B |
| H | X | Z (Isolation |

**Notes:**

1. H = High Signal Level, L = Low Signal Level
   X = Don't Care or Irrelevant, Z = High Impedance

## Product Pin Description

| Pin Name | Description |
|---|---|
| $\overline{OE}$ | 3-State Output Enable Inputs (Active LOW) |
| DIR | Direction Control Input |
| Ax | Side A Inputs or 3-State Outputs |
| Bx | Side B Inputs or 3-State Outputs |
| NC | No Internal Connect |
| GND | Ground |
| $V_{CCA}$,$V_{CCB}$ | Power |

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

| | |
|---|---|
| Supply voltage range, $V_{CCA}$ and $V_{CCB}$ | –0.5V to +7V |
| Input voltage range, $V_I$(1) : I/O ports (A-port) | –0.5V to $V_{CCA}$ +0.5V |
| I/O ports (B-port) | –0.5V to $V_{CCB}$+0.5V |
| Control Pins | –0.5V to $V_{CCA}$ +0.5V |
| Input clamp current, $I_{IK}$ ($V_I$ <0) | –50mA |
| Output clamp current, $I_{OK}$ ($V_O$ <0) | –50mA |
| Continous Output Current $I_O$ | ±50mA |
| Continous Current through each $V_{CC}$ or GND pin | ±100mA |
| Package thermal impedance, $\theta_{JA}$(2): package L | 84°C/W |
| package Q | 98°C/W |
| package S | 79°C/W |
| Storage Temperature range, $T_{stg}$ | –65°C to 150°C |

**Notes:**
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

1. This value is limited to 7V maximum.
2. The package thermal impedance is calculated in accordance with JESD 51.

## Recommended Operating Conditions(1)

| Parameters | Descritption | | $V_{CCA}$ | $V_{CCB}$ | Min. | Nom. | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{CCA}$ | Supply Voltage | | | | 4.5 | 5 | 5.5 | V |
| $V_{CCB}$ | Supply Voltage | | | | 2.7 | 3.3 | 5.5 | |
| $V_{IHA}$ | High-Level Input Voltage | $V_{OB} < 0.1V$ or $V_{OB} > V_{CCB} - 0.1V$ | 4.5V | 2.7V | 2 | | | |
| | | | | 3.6V | 2 | | | |
| | | | 5.5V | 5.5V | 2 | | | |
| $V_{IHB}$ | High-Level Input Voltage | $V_{OA} < 0.1V$ or $V_{OA} > V_{CCA} - 0.1V$ | 4.5V | 2.7V | 2 | | | |
| | | | | 3.6V | 2 | | | |
| | | | 5.5V | 5.5V | 3.85 | | | |
| $V_{ILA}$ | Low-Level Input Voltage | $V_{OB} < 0.1V$ or $V_{OB} > V_{CCB} - 0.1V$ | 4.5V | 2.7V | | | 0.8 | |
| | | | | 3.6V | | | 0.8 | |
| | | | 5.5V | 5.5V | | | 0.8 | |
| $V_{ILB}$ | Low-Level Input Voltage | $V_{OA} < 0.1V$ or $V_{OA} > V_{CCA} - 0.1V$ | 4.5V | 2.7V | | | 0.8 | |
| | | | | 3.6V | | | 0.8 | |
| | | | 5.5V | 5.5V | | | 1.65 | |
| $V_{IH}$ | High-Level Input Voltage (Control Pins) | $V_{OA} < 0.1V$ or $V_{OA} > V_{CCA} - 0.1V$, or $V_{OB} < 0.1V$ or $V_{OB} > V_{CCB} - 0.1V$ | 4.5V | 2.7V | 2 | | | |
| | | | | 3.6V | 2 | | | |
| | | | 5.5V | 5.5V | 2 | | | |
| $V_{IL}$ | Low-Level Input Voltage (Control Pins) | $V_{OA} < 0.1V$ or $V_{OA} > V_{CCA} - 0.1V$, or $V_{OB} < 0.1V$ or $V_{OB} > V_{CCB} - 0.1V$ | 4.5V | 2.7V | | | 0.8 | |
| | | | | 3.6V | | | 0.8 | |
| | | | 5.5V | 5.5V | | | 0.8 | |
| $V_{IA}$ | Input Voltage | | | | 0 | | $V_{CCA}$ | |
| $V_{IB}$ | Input Voltage | | | | 0 | | $V_{CCB}$ | |
| $V_{OA}$ | Output Voltage | | | | 0 | | $V_{CCA}$ | |
| $V_{OB}$ | Output Voltage | | | | 0 | | $V_{CCB}$ | |
| $I_{OHA}$ | High-Level Output Current | | 4.5V | 3V | | | –24 | mA |
| $I_{OHB}$ | High-Level Output Current | | 4.5V | 2.7V to 4.5V | | | –24 | |
| $I_{OLA}$ | Low-Level Output Current | | 4.5V | 3V | | | 24 | |
| $I_{OLB}$ | Low-Level Output Current | | 4.5V | 2.7V to 4.5V | | | 24 | |
| $\Delta t/\Delta v$ | Input Transmition Rise or Fall Rate | | | | | | 10 | ns/v |
| $T_A$ | Operating Free-Air Temperature | | | | –40 | | 85 | °C |

**Notes:**
1. All unused inputs of the device must be held at the associated $V_{CC}$ or GND to ensure proper device operation.

**DC Electrical Characteristics** (Over Supply Voltage and Operating Temperature Ranges, unless otherwise specified).

| Parameters | Description | Test Conditions | $V_{CCA}$ | $V_{CCB}$ | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OHA}$ | Minimum High Level Output Voltage (Port A) | $I_{OH}$ = –100µA | 4.5V | 3V | 4.4 | 4.5 | | V |
| | | $I_{OH}$ = –24mA | 4.5V | 3V | 3.76 | 4.17 | | |
| $V_{OHB}$ | Minimum High Level Output Voltage (Port B) | $I_{OH}$ = –100µA | 4.5V | 3V | 2.9 | 3.0 | | |
| | | $I_{OH}$ = –12mA | 4.5V | 2.7V | 2.2 | 2.56 | | |
| | | | | 3V | 2.46 | 2.85 | | |
| | | $I_{OH}$ = –24mA | 4.5V | 2.7V | 2.1 | 2.42 | | |
| | | | | 3V | 2.25 | 2.70 | | |
| | | | | 4.5V | 3.76 | 4.21 | | |
| $V_{OLA}$ | Maximum Low Level Output Voltage (Port A) | $I_{OL}$ = 100µA | 4.5V | 3V | | | 0.1 | |
| | | $I_{OL}$ = 24mA | 4.5V | 3V | | 0.19 | 0.44 | |
| $V_{OLB}$ | Maximum Low Level Output Voltage (Port B) | $I_{OL}$ = 100µA | 4.5V | 3V | | | 0.1 | |
| | | $I_{OL}$ = 12mA | 4.5V | 2.7V | | 0.09 | 0.44 | |
| | | $I_{OL}$ = 24mA | 4.5V | 2.7V | | 0.18 | 0.5 | |
| | | | | 3V | | 0.18 | 0.44 | |
| | | | | 4.5V | | 0.18 | 0.44 | |
| $I_I$ | Maximum Input Leakage Current (Control Inputs) | $V_I = V_{CCA}$ or GND | 5.5V | 3.6V | | | ±1 | µA |
| | | | | 5.5V | | | ±1 | |
| $I_{OZ}$[1] | Maximum 3-state Output Leakage Current (A or B ports) | $V_I = V_{IL}$ or $V_{IH}$, $\overline{OE} = V_{CCA}$, $V_O = V_{CCA/B}$ or GND | 5.5V | 3.6V | | | ±5 | |
| $I_{CCA}$ | Quiescent $V_{CCA}$ Supply Current | A port = $V_{CCA}$ or GND, $I_O$= 0 | 5.5V | Open | | | 10 | |
| | | B to A, B-port = $V_{CCB}$ or GND, $I_O$ (A port) = 0 | 5.5V | 3.6V | | | 10 | |
| | | | | 5.5V | | | 10 | |
| $I_{CCB}$ | Quiescent $V_{CCB}$ Supply Current | A to B, A port = $V_{CCA}$ or GND, $I_O$ (B port) = 0 | 5.5V | 3.6V | | | 10 | |
| | | | | 5.5V | | | 10 | |
| $\Delta I_{CC}$[2] | $I_{CC}$ per input (A port) | One Input $V_I = V_{CCA}$ –2.1V, Other inputs = $V_{CCA}$ or GND, $\overline{OE}$ = GND and DIR = $V_{CCA}$ | 5.5V | 5.5V | | 0.65 | 1.5 | mA |
| | $I_{CC}$ per input ($\overline{OE}$) | $V_I = V_{CCA}$ –2.1V, Other inputs =$V_{CCA}$ or GND, DIR = $V_{CCA}$ or GND | 5.5V | 5.5V | | 0.65 | 1.5 | |
| | $I_{CC}$ per input (DIR) | $V_I = V_{CCA}$ –2.1V, Other inputs = $V_{CCA}$ or GND, $\overline{OE}$ = $V_{CCA}$ or GND | 5.5V | 3.6V | | 0.65 | 1.5 | |
| | $I_{CC}$ per input (B Port) | One Input $V_I = V_{CCB}$ –0.6V, Other inputs = $V_{CCB}$ or GND, $\overline{OE}$ = GND and DIR = GND | 5.5V | 3.6V | | | 50 | µA |

**Notes:**
1. For I/O ports, the parameter $I_{OZ}$ includes the input leakage current.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0V or the associated $V_{CC}$.

## Capacitance ($T_A$ = 25°C)

| Parameters | Description | Test Conditions | | Typ. | Units |
|---|---|---|---|---|---|
| $C_{IN}$ | Control Input Capacitance | $V_I = V_{CCA}$ or GND, $V_{CCA}$ = Open, $V_{CCB}$ =Open | | 2.4 | pF |
| $C_{I/O}$ | Input/Output Capacitance (A or B port) | $V_{I/O} = V_{CCA/B}$ or GND, $V_{CCA}$ = 5V, $V_{CCB}$ = 3.3V | | 9.5 | |
| $C_{PD}$ | Power Dissipation Capacitance (1) | Outputs Enabled | $V_{CCA}$ = 5V, $V_{CCB}$ = 3.3V $C_L$ = 0pF, f = 10 MHz | 20 | |
| | | Outputs Disabled | | 2.2 | |

**Notes:**
1. $C_{PD}$ is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption ($I_{CCD}$) at no output loading and operating at 50% duty cycle, $C_{PD}$ is related to $I_{CCD}$ dynamic operating current by the expression: $I_{CCD} = (C_{PD})(V_{CC})(f_{IN}) + (I_{CC}$ static)

## AC Electrical Characteristics (Over Operating Range, –40°C to +85°C)

| Parameters | From (Input) | To (Output) | $V_{CCA}$ = 5V ± 0.5V, $V_{CCB}$ = 5V ± 0.5V | | $V_{CCA}$ = 5V ± 0.5V, $V_{CCB}$ = 2.7V to 3.6V | | Units |
|---|---|---|---|---|---|---|---|
| | | | $C_L$ = 50pF, $R_L$ = 500Ω | | $C_L$ = 50pF, $R_L$ = 500Ω | | |
| | | | Min. | Max. | Min. | Max. | |
| $t_{PHL}$ | A | B | 1 | 6.1 | 1 | 6 | ns |
| $t_{PLH}$ | | | 1 | 5.8 | 1 | 5.8 | |
| $t_{PHL}$ | B | A | 1 | 6 | 1 | 6.1 | |
| $t_{PLH}$ | | | 1 | 6.2 | 1 | 6.2 | |
| $t_{PZL}$ | $\overline{OE}$ | A | 1 | 8 | 1 | 8 | |
| $t_{PZH}$ | | | 1 | 7.1 | 1 | 7.1 | |
| $t_{PZL}$ | $\overline{OE}$ | B | 1 | 8 | 1 | 8 | |
| $t_{PZH}$ | | | 1 | 8 | 1 | 7.8 | |
| $t_{PLZ}$ | $\overline{OE}$ | A | 1 | 5.2 | 1 | 5.2 | |
| $t_{PHZ}$ | | | 1 | 4.9 | 1 | 4.9 | |
| $t_{PLZ}$ | $\overline{OE}$ | B | 1 | 5.2 | 1 | 5.4 | |
| $t_{PHZ}$ | | | 1 | 4.9 | 1 | 5.4 | |
| $t_{SK(O)}$ | Output-to-Output Skew(1) | | | 1.5 | | 1.5 | |

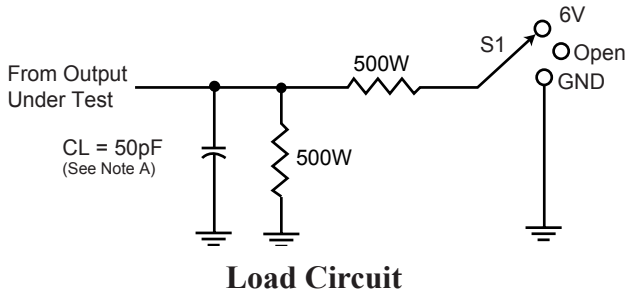
**Notes:**
1. Skew between any two outputs of the same device, switching in the same direction. Parameter guaranteed by design.

## Power- Up Considerations

To avoid excessive supply current, bus contention or oscillation during power-up, the following guidelines should be followed:

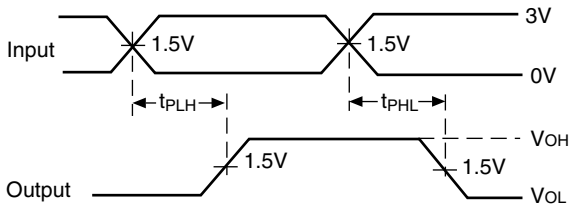
1. Connect ground first before any supply voltage is applied.
2. Then Power up $V_{CCA}$, which is the control side of the device.
3. Ramp $\overline{OE}$ ahead of or with $V_{CCA}$ to help prevent bus contention
4. Ramp DIR with $V_{CCA}$ if DIR high is needed (A bus to B bus). Otherwise keep DIR Low.

## PARAMETER MEASUREMENT INFORMATION FOR A TO B PORT
## $V_{CCA}$ =4.5V TO 5.5V and $V_{CCB}$ = 2.7V to 3.6V

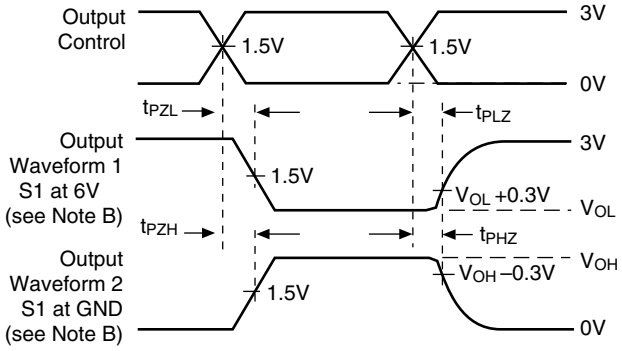



Load Circuit

| Test | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 6V |
| $t_{PHZ}/t_{PZH}$ | GND |




Voltage Waveforms
Propagation Delay Times




Voltage Waveforms
Enable and Disable Times

**Figure 1. Load Circuit and Voltage Waveforms**

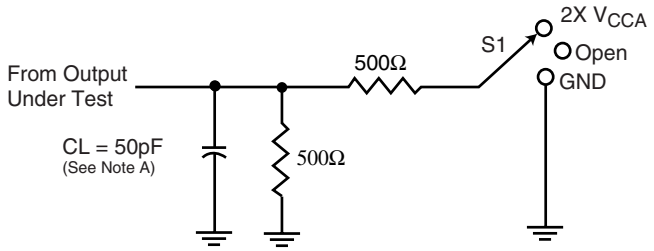
**Notes:**

A. $C_L$ includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

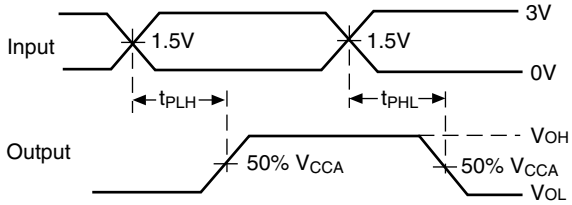
- All input impulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50Ω, $t_R$ ≤ 2.5ns, $t_F$ ≤ 2.5ns.
- The outputs are measured one at a time with one transition per measurement.

## PARAMETER MEASUREMENT INFORMATION FOR B TO A
## $V_{CCA}$ =4.5V TO 5.5V and $V_{CCB}$ = 2.7V to 3.6V

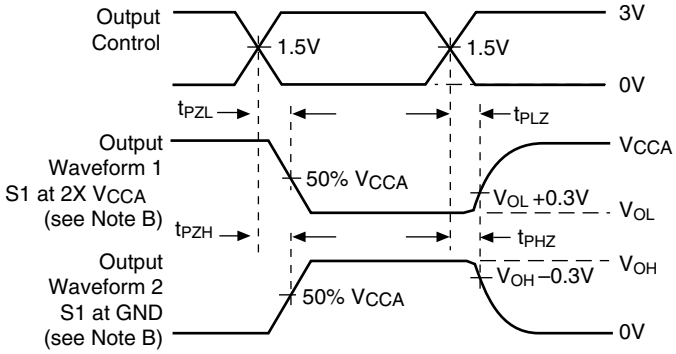



**Load Circuit**

| Test | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$<br>$t_{PLZ}/t_{PZL}$<br>$t_{PHZ}/t_{PZH}$ | Open<br>2X $V_{CCA}$GND |




**Voltage Waveforms**
**Propagation Delay Times**




**Voltage Waveforms**
**Enable and Disable Times**

**Figure 3. Load Circuit and Voltage Waveforms**

**Notes:**

A. $C_L$ includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

- All input impulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50Ω, $t_R$ ≤ 2.5ns, $t_F$ ≤ 2.5ns.
- The outputs are measured one at a time with one transition per measurement.

## PARAMETER MEASUREMENT INFORMATION FOR A TO B
## $V_{CCA}$ =4.5V TO 5.5V and $V_{CCB}$ = 4.5V to 5.5V

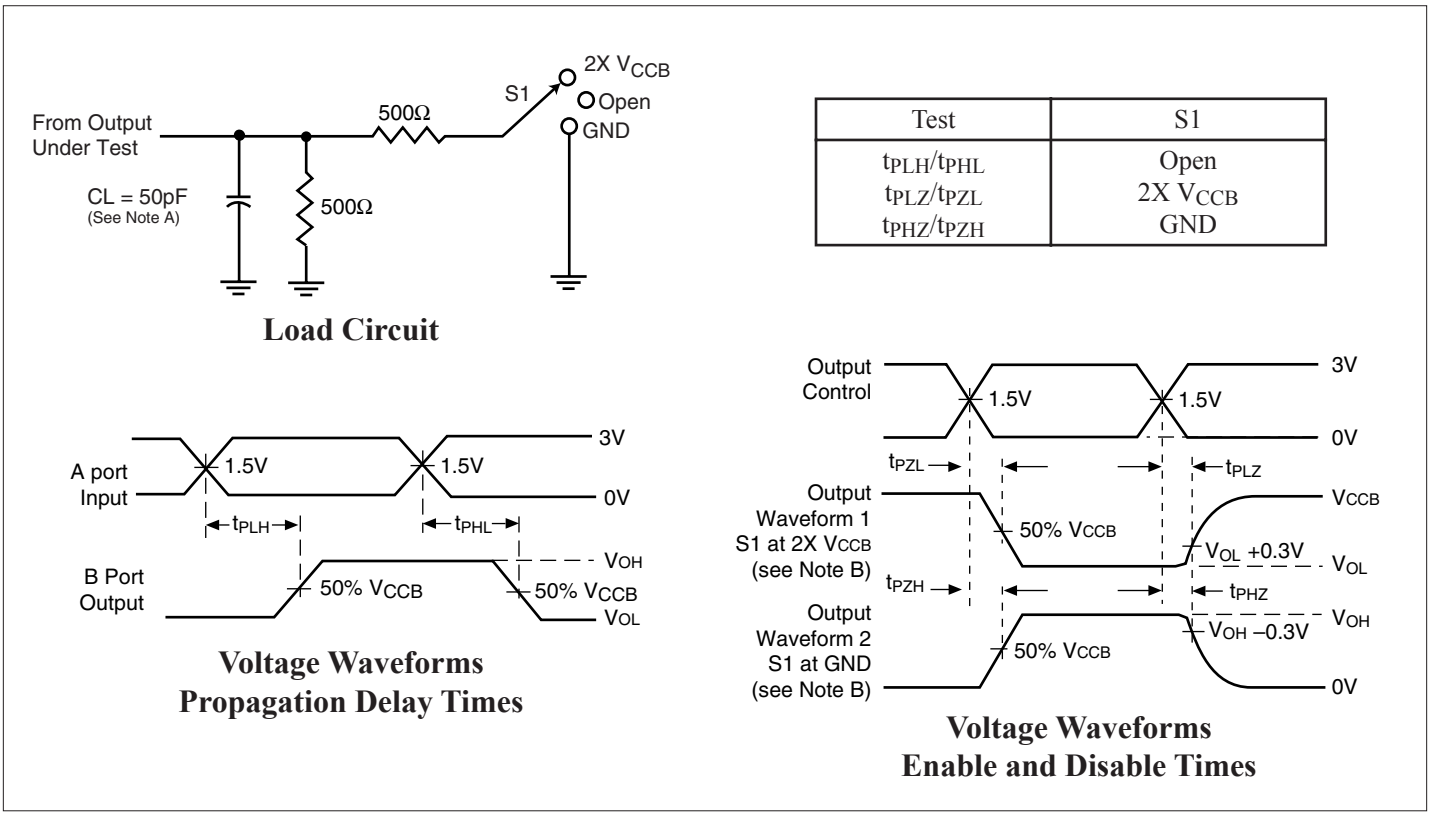



**Figure 2. Load Circuit and Voltage Waveforms**

**Notes:**

A. $C_L$ includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

- All input impulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50Ω, $t_R$ ≤ 2.5ns, $t_F$ ≤ 2.5ns.
- The outputs are measured one at a time with one transition per measurement.

## PARAMETER MEASUREMENT INFORMATION FOR B TO A
## $V_{CCA}$ =4.5V TO 5.5V and $V_{CCB}$ = 4.5V to 5.5V

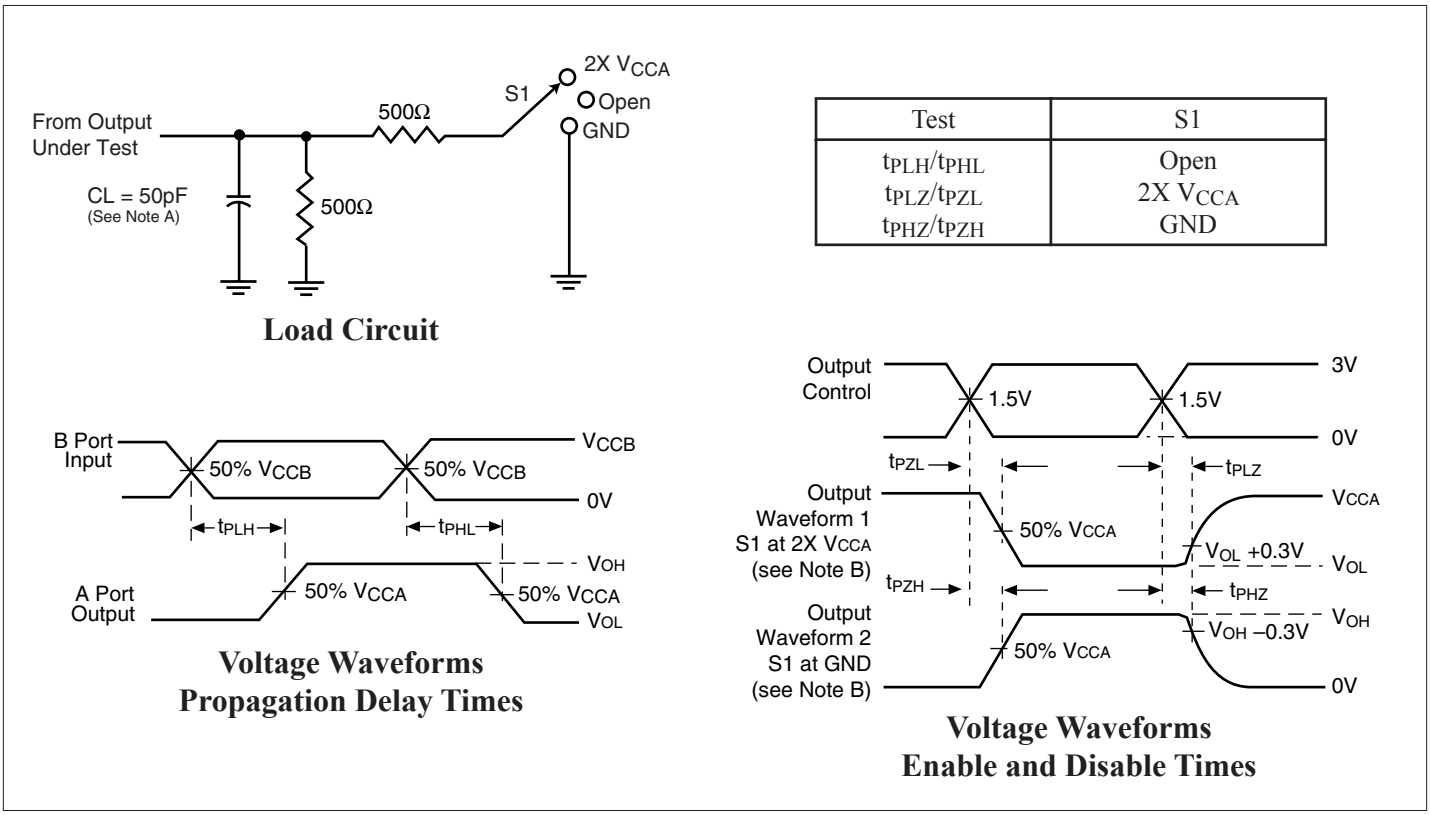



**Figure 2. Load Circuit and Voltage Waveforms**

**Notes:**

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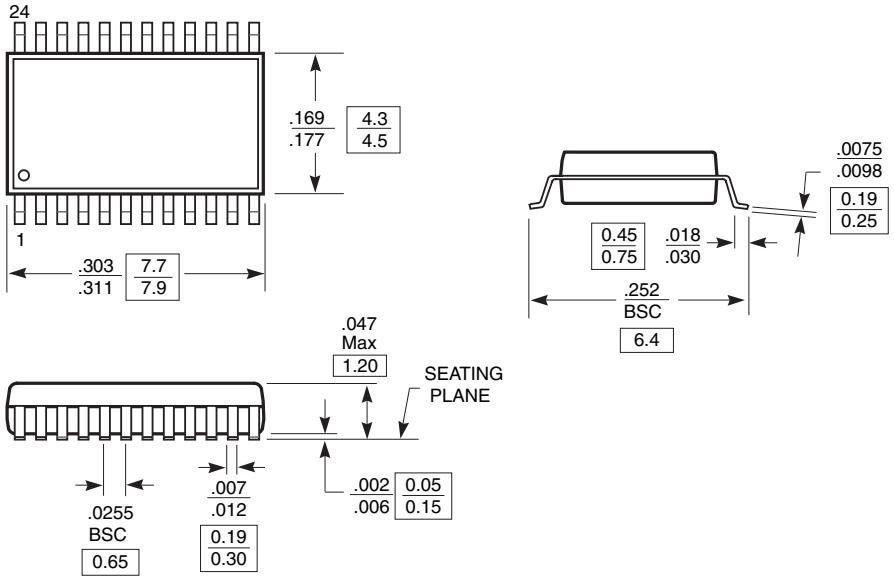
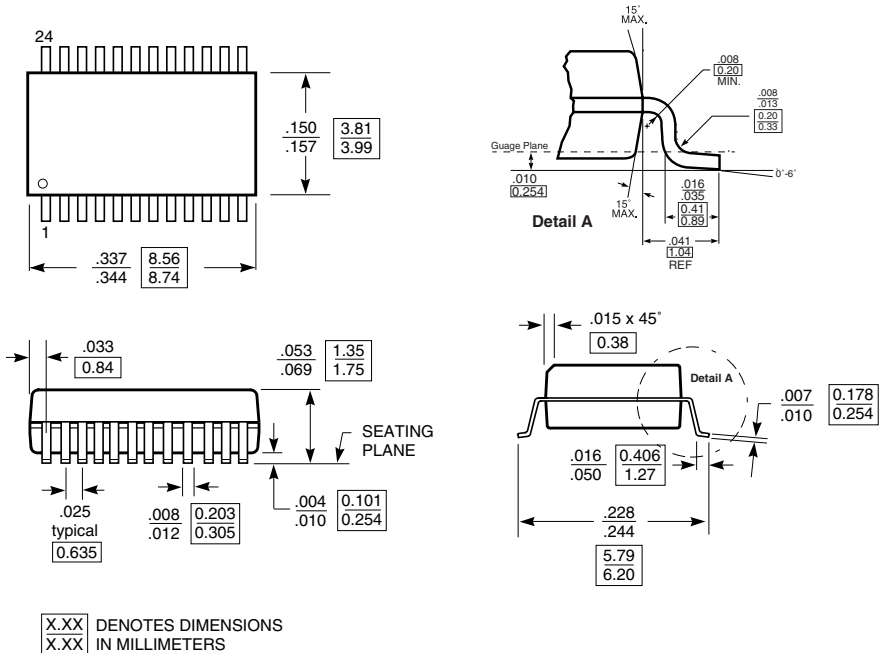
- All input impulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50Ω, $t_R$ ≤ 2.5ns, $t_F$ ≤ 2.5ns.
- The outputs are measured one at a time with one transition per measurement.

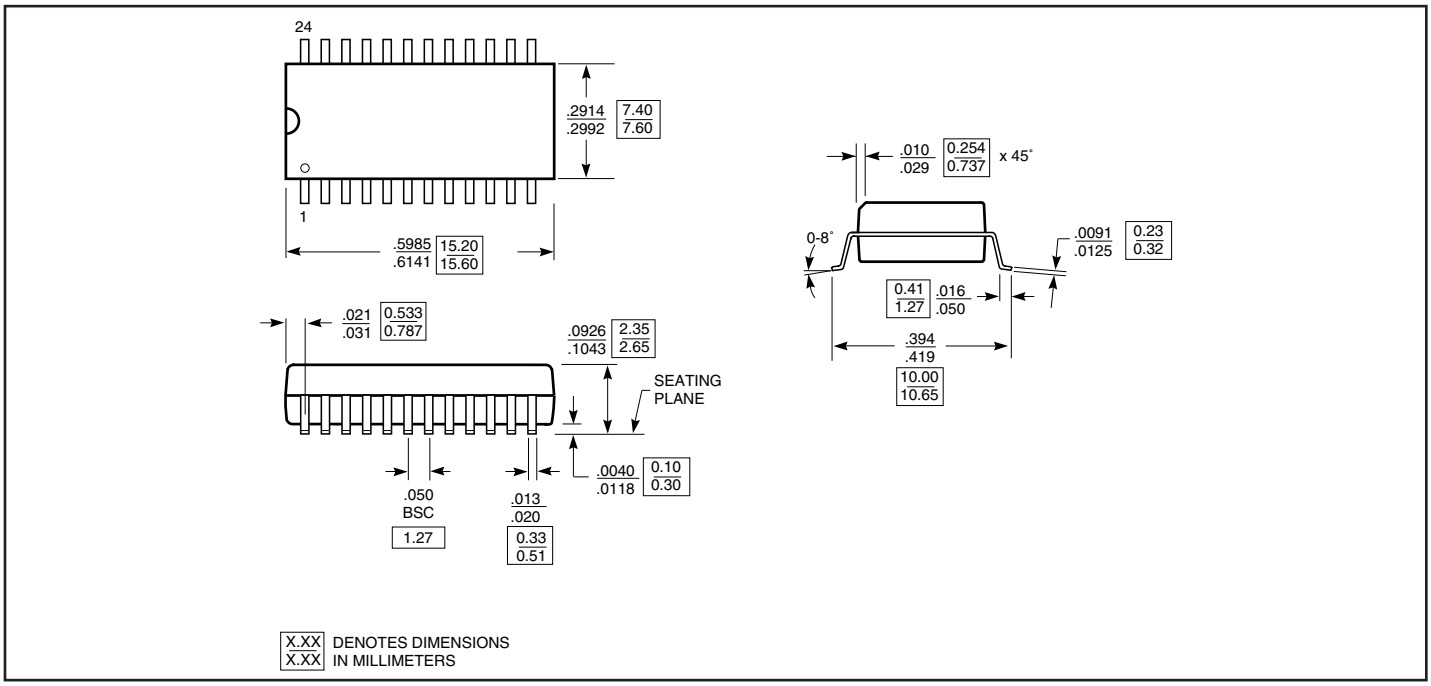
## Packaging Mechanical: 24-pin TSSOP (L)




## Packaging Mechanical: 24-pin QSOP (Q)



## Packaging Mechanical: 24-pin SOIC (S)




## Ordering Information

| Ordering Code | Package Code | Package Type |
|---|---|---|
| PI74LVCC4245AL | L | 24-pin, 173-mil wide plastic TSSOP |
| PI74LVCC4245ALE | L | Pb-free & Green, 24-pin, 173-mil wide plastic TSSOP |
| PI74LVCC4245AQ | Q | 24-pin, 150-mil wide plastic QSOP |
| PI74LVCC4245AS | S | 24-pin, 300-mil wide plastic SOI |
| PI74LVCC4245ASE | S | Pb-free & Green, 24-pin, 300-mil wide plastic SOI |

**Notes:**

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free & Green
- Adding an X suffix = Tape/Reel