National Semiconductor

August 1991

54AC/74AC112 • 54ACT/74ACT112
Dual JK Negative Edge-Triggered Flip-Flop

General Description

The 'AC/'ACT112 contain two independent, high-speed JK flip-flops with Direct Set and Clear inputs. Synchronous state changes are initiated by the falling edge of the clock. Triggering occurs at a voltage level of the clock and is not directly related to the transition time. The J and K inputs can change when the clock is in either state without affecting the flip-flop, provided that they are in the desired state during the recommended setup and hold times relative to the falling edge of the clock. A LOW signal on $\overline{S}_D$ or $\overline{C}_D$ prevents clocking and forces Q or $\overline{Q}$ HIGH, respectively. Simultaneous LOW signals on $\overline{S}_D$ and $\overline{C}_D$ force both Q and $\overline{Q}$ HIGH.

Asynchronous Inputs:

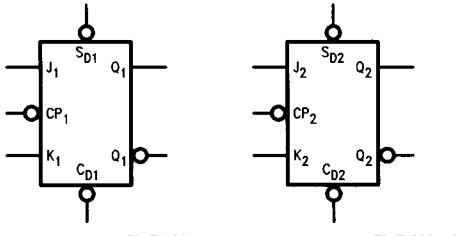
LOW input to $\overline{S}_D$ sets Q to HIGH level
LOW input to $\overline{C}_D$ sets Q to LOW level
Clear and Set are independent of clock
Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

Features

- 'ACT112 has TTL-compatible inputs
- Outputs source/sink 24 mA

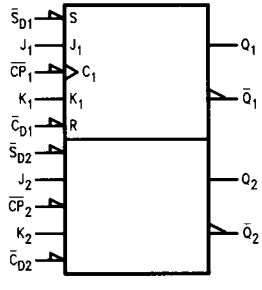
Information for 'AC112 and 54 Grade is ADVANCED INFORMATION.

Logic Symbols



TL/F/9924–1 TL/F/9924–2

IEEE/IEC

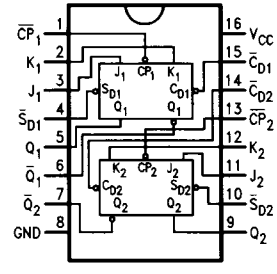


TL/F/9924–4

Pin Names	Description
J_1, J_2, K_1, K_2	Data Inputs
$\overline{CP}_1, \overline{CP}_2$	Clock Pulse Inputs (Active Falling Edge)
$\overline{C}_{D1}, \overline{C}_{D2}$	Direct Clear Inputs (Active LOW)
$\overline{S}_{D1}, \overline{S}_{D2}$	Direct Set Inputs (Active LOW)
$Q_1, Q_2, \overline{Q}_1, \overline{Q}_2$	Outputs

Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



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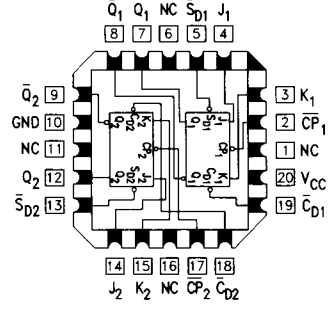
Pin Assigment for LCC



TL/F/9924–5

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RRD-B20M81/Printed in U. S. A.

Truth Table

Inputs					Outputs	
$\overline{S}_D$	$\overline{C}_D$	$\overline{CP}$	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H	H
H	H	↘	h	h	$\overline{Q}_0$	Q_0
H	H	↘	l	h	L	H
H	H	↘	h	l	H	L
H	H	↘	l	l	Q_0	$\overline{Q}_0$

H (h) = HIGH Voltage Level

L (l) = LOW Voltage Level

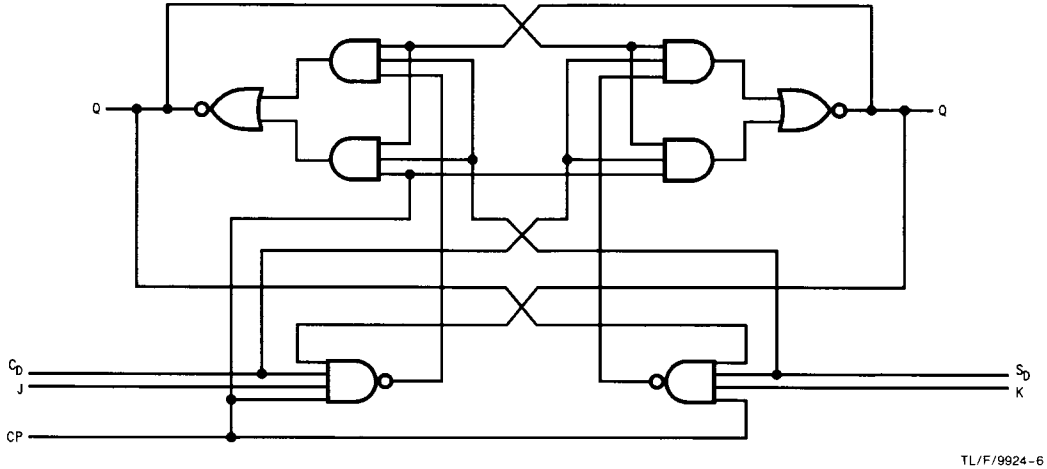
X = Immaterial

↘ = HIGH-to-LOW Clock Transition

Q_0 ($\overline{Q}_0$) = Before HIGH-to-LOW Transition of Clock

Lower case letters indicate the state of the referenced input or output one setup time prior to the HIGH-to-LOW clock transition.

Logic Diagram (One Half Shown)



TL/F/9924–6

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + O.5	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} +0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'ACT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.5	0.44	V	*V_{IN} = V_{IL} or V_{IH} 12 MA
		4.5		0.36	0.5	0.44		I_{OL} 24 mA
		5.5		0.36	0.5	0.44		24 mA

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}. I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$		54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditons
			Typ	Guaranteed Limits				
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}. I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$		54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 MA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC}$ − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics:

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency	3.3 5.0	125 150					100 125		MHz
t_{PLH}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	3.3 5.0	1.0 1.0	11.0 8.5	14.0 11.0			1.0 1.0	15.0 12.0	ns
t_{PHL}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	3.3 5.0	1.0 1.0	11.0 8.5	14.0 11.0			1.0 1.0	15.0 12.0	ns
t_{PLH}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	3.3 5.0	1.0 1.0	9.5 7.0	12.5 9.5			1.0 1.0	13.5 10.5	ns
t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	3.3 5.0	1.0 1.0	11.5 9.0	14.5 11.0			1.0 1.0	15.5 12.5	ns

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements:

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units
			Typ	Guaranted Minimum			
t_s	Setup Time, HIGH or LOW J_n or $\overline{K}_n$ to CP_n	3.3 5.0	3.0 2.0	5.5 4.5		6.0 4.6	ns
t_h	Hold Time, HIGH or LOW J_n or $\overline{K}_n$ to CP_n	3.3 5.0	−1.5 −0.5	0 0		0 0	ns
t_w	Pulse Width $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$	3.3 5.0	2.0 2.0	5.5 4.5		7.0 5.0	ns
t_{rec}	Recovery Time $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP_n	3.3 5.0	−1.0 −1.0	3.5 3.0		3.5 3.0	ns

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics:

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency	5.0	100					80		MHz
t_{PLH}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	5.0	1.0	9.5	13.0			1.0	14.0	ns
t_{PHL}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	5.0	1.0	9.5	13.0			1.0	14.0	ns
t_{PLH}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	5.0	1.0	7.0	10.0			1.0	11.0	ns
t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	5.0	1.0	9.5	12.5			1.0	13.5	ns

Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements:

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units
			Typ	Guaranted Minimum			
t_s	Setup Time, HIGH or LOW J_n or $\overline{K}_n$ to CP_n	5.0	2.5	7.0		8.0	ns
t_h	Hold Time, HIGH or LOW J_n or $\overline{K}_n$ to CP_n	5.0	0.5	1.5		1.5	ns
t_w	Pulse Width CP_n or $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$	5.0	4.0	7.0		8.0	ns
t_{rec}	Recovery Time $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP_n	5.0	1.0	3.0		3.0	ns

Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	35	pF	$V_{CC} = 5.0V$

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

74ACT 112 P C QR

Temperature Range Family
- 74ACTQ = Commercial TTL-Compatible
- 54ACTQ = Military TTL-Compatible

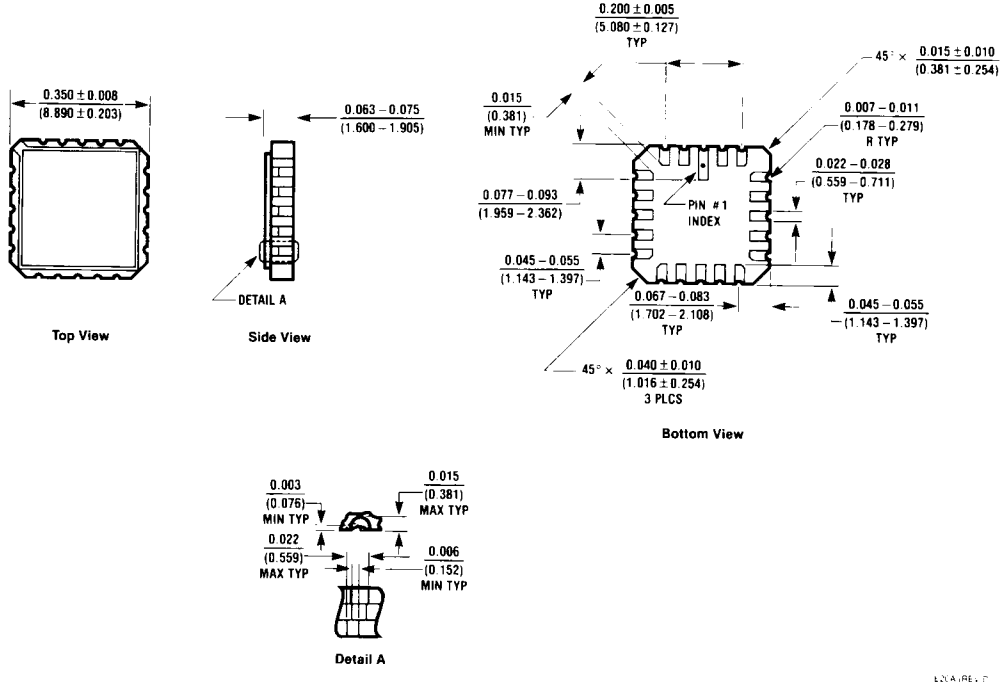
Device Type

Package Code
- P = Plastic DIP
- D = Ceramic DIP
- F = Flatpak
- L = Leadless Ceramic Chip Carrier (LCC)
- S = Small Outline (SOIC)

Special Variations
- X = Devices shipped in 13" reels
- QR = Commercial grade device with burn-in
- QB = Military grade device with environmental and burn-in processing shipped in tubes

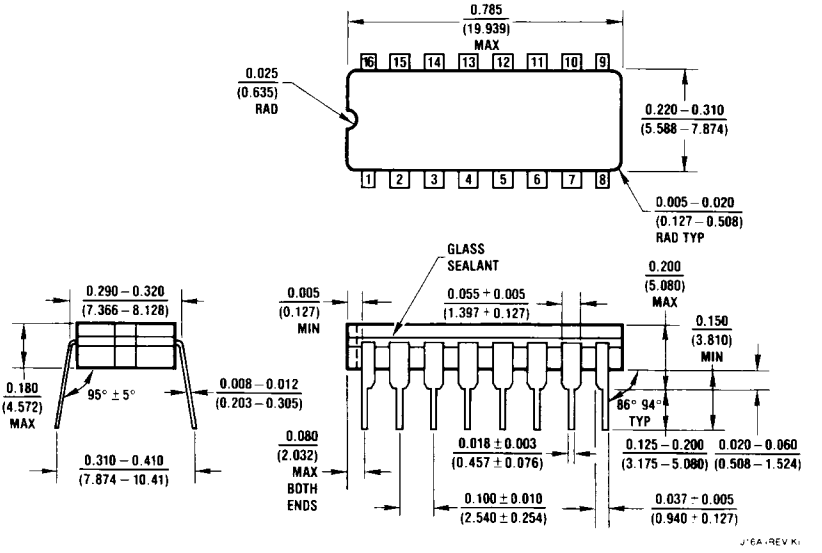
Temperature Range
- C = Commercial (−40°C to +85°C)
- M = Military (−55°C to +125°C)

Physical Dimensions inches (millimeters)

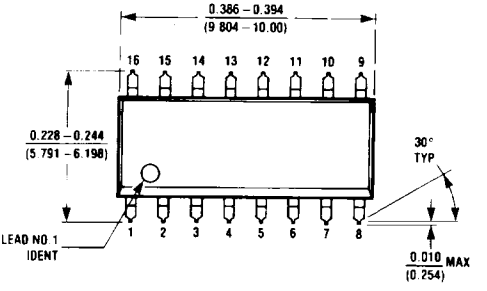


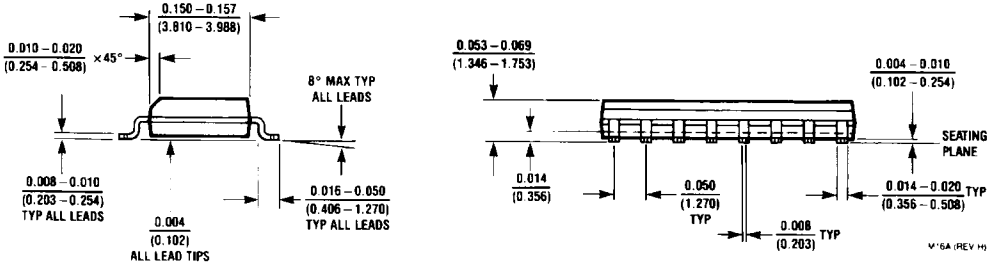
20-Lead Ceramic Leadless Chip Carrier (L)
NS Package Number E20A

Physical Dimensions inches (millimeters) (Continued)



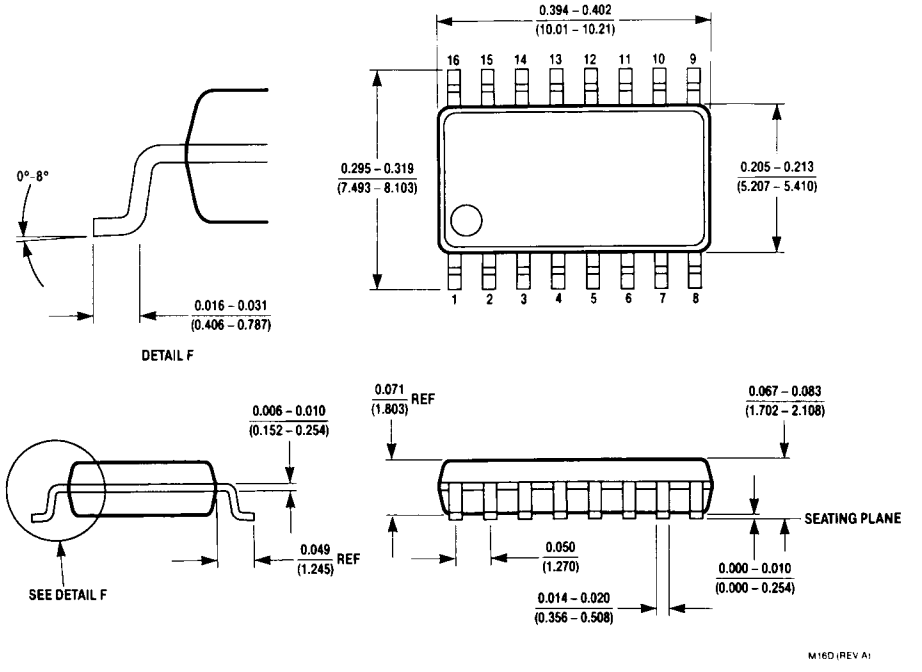
16-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J16A



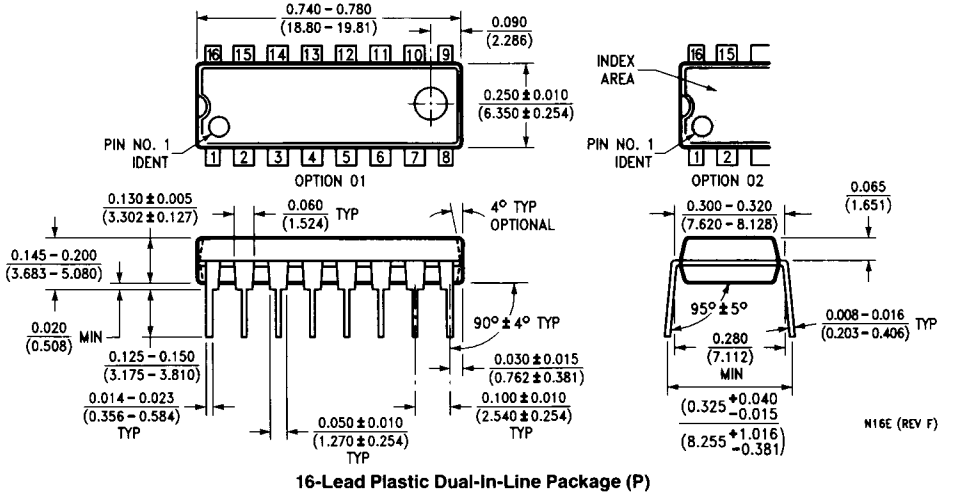


16-Lead Small Outline Integrated Circuit (S)
NS Package Number M16A

Physical Dimensions inches (millimeters) (Continued)

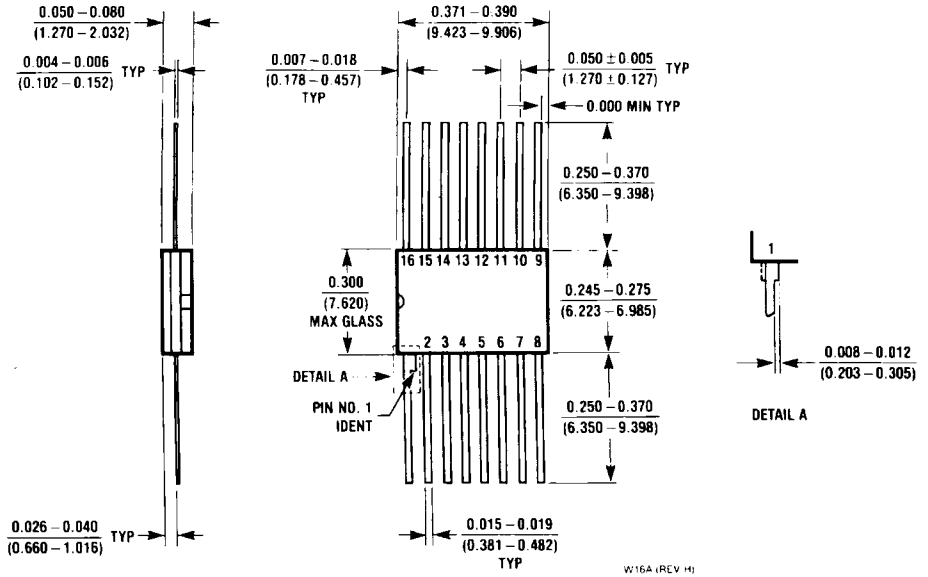


16-Lead Small Outlined Package—EIAJ (SJ)
NS Package Number M16D



16-Lead Plastic Dual-In-Line Package (P)
NS Package Number N16E

Physical Dimensions inches (millimeters) (Continued)



16-Lead Ceramic Flatpak (F)
NS Package Number W16A

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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