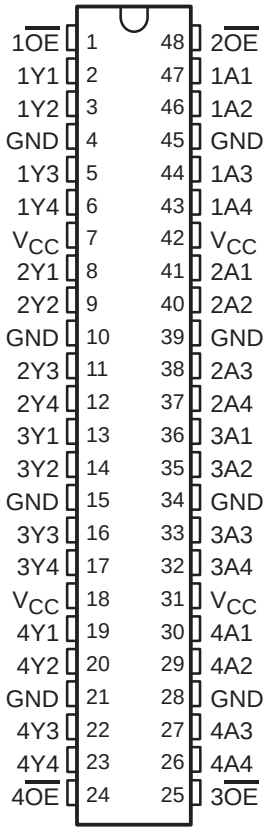
- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static-Power Dissipation**
- **5-V I/O Compatible**
- **High Drive Capability (–32 mA/64 mA)**
- **Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Support Unregulated Battery Operation Down to 2.3 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Auto3-State Eliminates Bus Current Loading When Voltage at the Output Exceeds V_{CC}**
- **I_{off} and Power-Up 3-State Support Hot Insertion**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV) Packages, and 380-mil Fine-Pitch Ceramic Flat (WD) Package**

NOTE: For tape and reel order entry:
The DGGR package is abbreviated to GR, and
the DGVR package is abbreviated to VR.

SN54ALVTH16244 . . . WD PACKAGE
SN74ALVTH16244 . . . DGG, DGV, OR DL PACKAGE
(TOP VIEW)



description

The ’ALVTH16244 devices are 16-bit buffers/line drivers designed for 2.5-V or 3.3-V V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

description (continued)

When V_{CC} is between 0 and 1.2 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.2 V, the output-enable ($\overline{OE}$) input should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

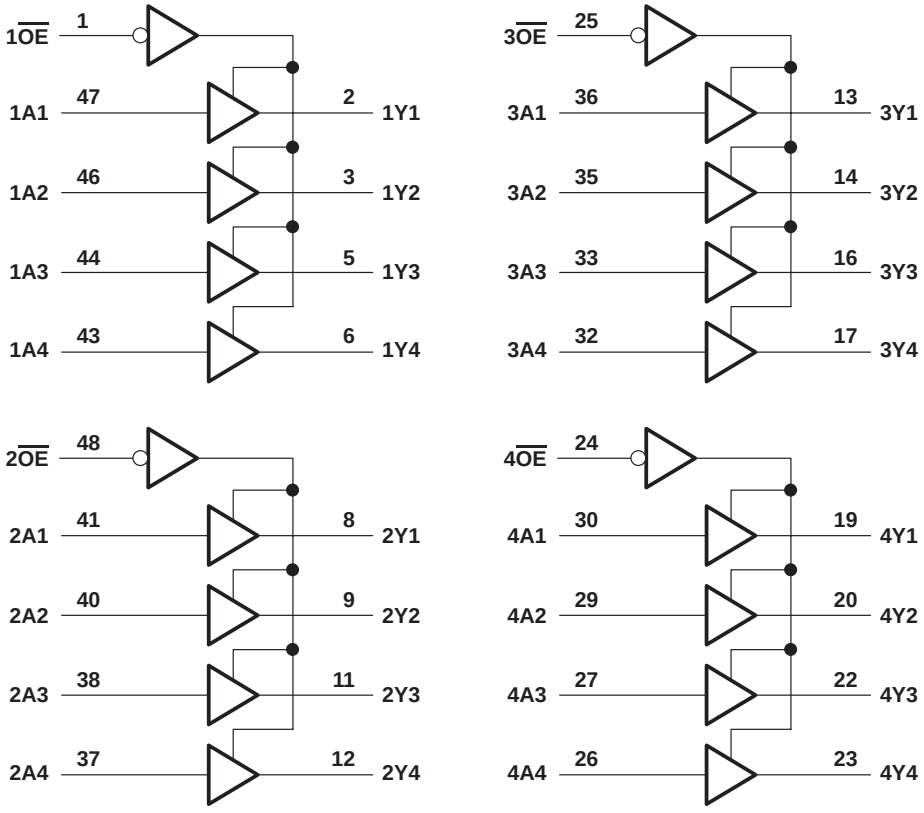
These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

The SN54ALVTH16244 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ALVTH16244 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1) . . . . . –0.5 V to V_{CC} to 7V
Output current in the low state, I_O: SN54ALVTH16244 . . . . . 96 mA
SN74ALVTH16244 . . . . . 128 mA
Output current in the high state, I_O: SN54ALVTH16244 . . . . . –48 mA
SN74ALVTH16244 . . . . . –64 mA
Input clamp current, I_{IK} ($V_I < 0$) . . . . . –50 mA
Output clamp current, I_{OK} ($V_O < 0$) . . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package . . . . . 89°C/W
DGV package . . . . . 93°C/W
DL package . . . . . 94°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions, V_{CC} = 2.5 V ± 0.2 V (see Note 3)

			SN54ALVTH16244		SN74ALVTH16244		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.3	2.7	2.3	2.7	V
V_{IH}	High-level input voltage		1.7		1.7		V
V_{IL}	Low-level input voltage			0.7		0.7	V
V_I	Input voltage		0	5.5	0	5.5	V
I_{OH}	High-level output current			–6		–8	mA
I_{OL}	Low-level output current			6		8	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1 kHz			18		24	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		200		μs/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

recommended operating conditions, V_{CC} = 3.3 V ± 0.3 V (see Note 3)

			SN54ALVTH16244		SN74ALVTH16244		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		3	3.6	3	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	5.5	0	5.5	V
I_{OH}	High-level output current			–24		–32	mA
I_{OL}	Low-level output current			24		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1 kHz			48		64	
Δt/Δv	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		200		μs/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALVTH16244			SN74ALVTH16244			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 2.3 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}		V_{CC} = 2.3 V to 2.7 V,	I_{OH} = –100 µA	V_{CC}–0.2			V_{CC}–0.2			V
		V_{CC} = 2.3 V	I_{OH} = –6 mA	1.8						
			I_{OH} = –8 mA				1.8			
V_{OL}		V_{CC} = 2.3 V to 2.7 V,	I_{OL} = 100 µA			0.2			0.2	V
		V_{CC} = 2.3 V	I_{OL} = 6 mA			0.4				
			I_{OL} = 8 mA						0.4	
			I_{OL} = 18 mA			0.5				
			I_{OL} = 24 mA						0.5	
I_I	Control inputs	V_{CC} = 2.7 V,	V_I = V_{CC} or GND			±1			±1	µA
		V_{CC} = 0 or 2.7 V,	V_I = 5.5 V			10			10	
	Data inputs	V_{CC} = 2.7 V	V_I = V_{CC}			1			1	
			V_I = 0			–5			–5	
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 4.5 V						±100	µA
$I_{I(hold)}$	Data inputs	V_{CC} = 2.3 V	V_I = 0.7 V		115			115		µA
			V_I = 1.7 V		–10			–10		
		V_{CC} = 2.7 V‡,	V_I = 0 to 2.7 V			±300			±300	
I_{EX}§		V_{CC} = 2.3 V,	V_O = 5.5 V			125			125	µA
$I_{OZ(PU/PD)}$¶		V_{CC} ≤ 1.2 V, V_O = 0.5 V to V_{CC}, V_I = GND or V_{CC}, $\overline{OE}$ = don't care				±100			±100	µA
I_{OZH}		V_{CC} = 2.7 V	V_O = 2.3 V, V_I = 0.7 V or 1.7 V			5			5	µA
I_{OZL}		V_{CC} = 2.7 V	V_O = 0.5 V, V_I = 0.7 V or 1.7 V			–5			–5	µA
I_{CC}		V_{CC} = 2.7 V, I_O = 0, V_I = V_{CC} or GND	Outputs high		0.04	0.1		0.04	0.1	mA
			Outputs low		2.3	4.5		2.3	4.5	
			Outputs disabled		0.04	0.1		0.04	0.1	
C_i		V_{CC} = 2.5 V,	V_I = 2.5 V or 0		3			3		pF
C_o		V_{CC} = 2.5 V,	V_O = 2.5 V or 0		6			6		pF

† All typical values are at V_{CC} = 2.5 V, T_A = 25°C.
‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.
§ Current into an output in the high state when V_O > V_{CC}
¶ High-impedance state during power up/power down

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALVTH16244			SN74ALVTH16244			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 3 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}		V_{CC} = 3 V to 3.6 V,	I_{OH} = –100 µA	V_{CC}–0.2			V_{CC}–0.2			V
		V_{CC} = 3 V	I_{OH} = –24 mA	2						
			I_{OH} = –32 mA				2			
V_{OL}		V_{CC} = 3 V to 3.6 V,	I_{OL} = 100 µA			0.2			0.2	V
		V_{CC} = 3 V	I_{OL} = 16 mA						0.4	
			I_{OL} = 24 mA			0.5				
			I_{OL} = 32 mA						0.5	
			I_{OL} = 48 mA			0.55				
			I_{OL} = 64 mA						0.55	
I_I	Control inputs	V_{CC} = 3.6 V,	V_I = V_{CC} or GND			±1			±1	µA
		V_{CC} = 0 or 3.6 V,	V_I = 5.5 V			10			10	
	Data inputs	V_{CC} = 3.6 V	V_I = 5.5 V			20			20	
			V_I = V_{CC}			1			1	
			V_I = 0			–5			–5	
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 4.5 V						±100	µA
$I_{I(hold)}$	Data inputs	V_{CC} = 3 V	V_I = 0.8 V	75			75			µA
			V_I = 2 V	–75			–75			
		V_{CC} = 3.6 V‡,	V_I = 0 to 3.6 V			±500			±500	
I_{EX}§		V_{CC} = 3 V,	V_O = 5.5 V			125			125	µA
$I_{OZ(PU/PD)}$¶		V_{CC} ≤ 1.2 V, V_O = 0.5 V to V_{CC}, V_I = GND or V_{CC}, $\overline{OE}$ = don't care				±100			±100	µA
I_{OZH}		V_{CC} = 3.6 V	V_O = 3 V, V_I = 0.8 V or 2 V			5			5	µA
I_{OZL}		V_{CC} = 3.6 V	V_O = 0.5 V, V_I = 0.8 V or 2 V			–5			–5	µA
I_{CC}		V_{CC} = 3.6 V, I_O = 0, V_I = V_{CC} or GND	Outputs high		0.07	0.1		0.07	0.1	mA
			Outputs low		3.2	5		3.2	5	
			Outputs disabled		0.07	0.1		0.07	0.1	
ΔI_{CC}#		V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND				0.4			0.4	mA
C_i		V_{CC} = 3.3 V,	V_I = 3.3 V or 0		3			3		pF
C_o		V_{CC} = 3.3 V,	V_O = 3.3 V or 0		6			6		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.
§ Current into an output in the high state when V_O > V_{CC}
¶ High-impedance state during power up/power down
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

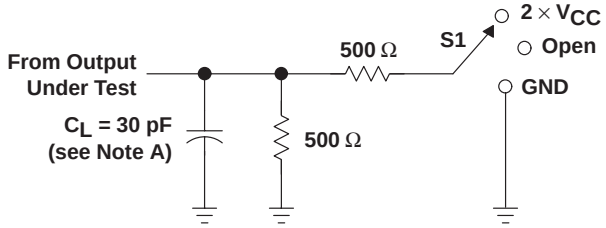
switching characteristics over recommended operating free-air temperature range, C_L = 30 pF, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ALVTH16244		SN74ALVTH16244		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1	3.1	1	3	ns
t_{PHL}			1	3.6	1	3.5	
t_{PZH}	$\overline{OE}$	Y	1.1	6	1.1	5.9	ns
t_{PZL}			1.1	4.8	1.1	4.7	
t_{PHZ}	$\overline{OE}$	Y	1.5	4.5	1.5	4.4	ns
t_{PLZ}			1	3.5	1	3.4	

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 2)

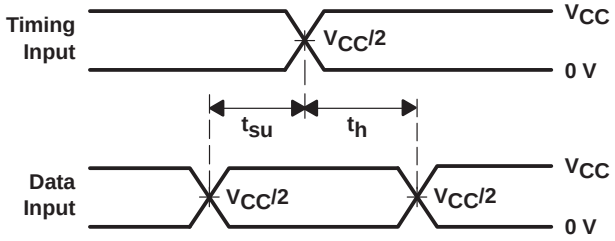
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ALVTH16244		SN74ALVTH16244		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1	2.6	1	2.4	ns
t_{PHL}			1	2.6	1	2.5	
t_{PZH}	$\overline{OE}$	Y	1	3.9	1	3.8	ns
t_{PZL}			1	3	1	2.9	
t_{PHZ}	$\overline{OE}$	Y	1.5	4.3	1.5	4.2	ns
t_{PLZ}			1.5	3.7	1.5	3.6	

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5 V ± 0.2 V

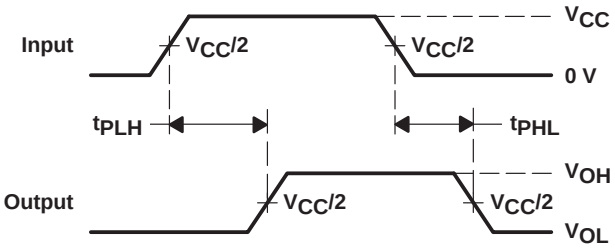


LOAD CIRCUIT

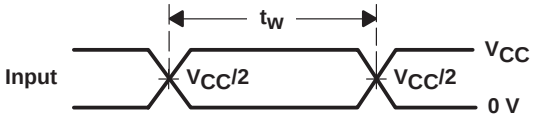
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



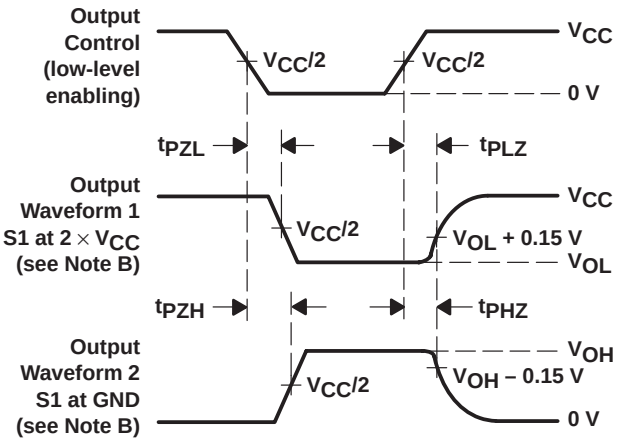
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION

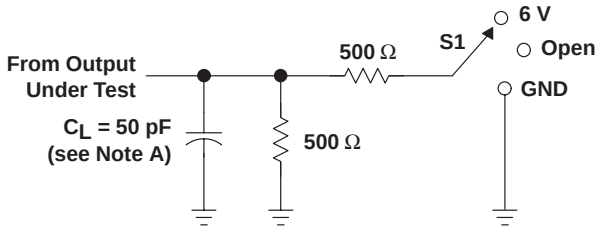


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.

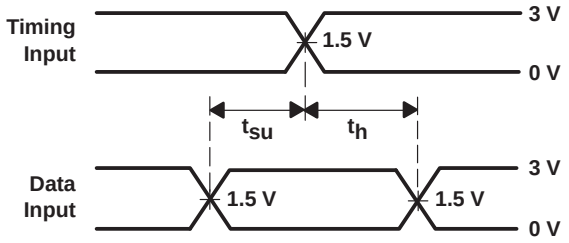
Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 3.3 V ± 0.3 V

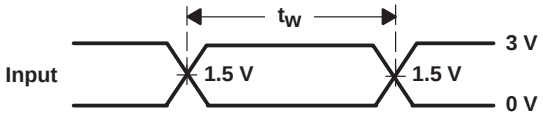


LOAD CIRCUIT

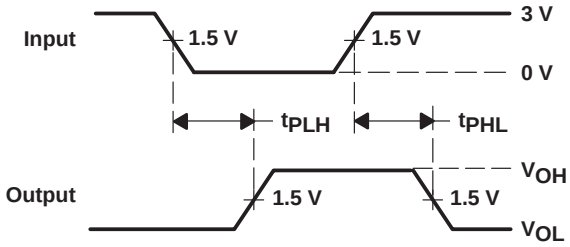
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



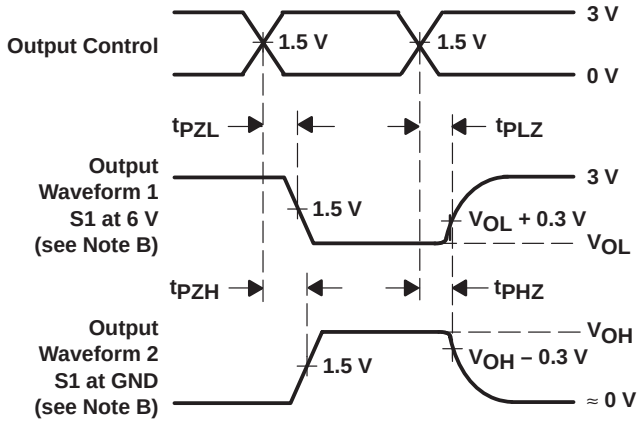
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

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SN74ALVTH16244, Status: ACTIVE

2.5-V/3.3-V 16-Bit Buffers/Drivers With 3-State Outputs

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Features	Samples	Technical Documents
Quality & Pb-Free Data	Pricing/Packaging	Applications Notes
Related Products	Inventory	Simulation Models
Development Tools	Symbols/Footprints	Reference Designs

Refine Your Selection

- Logic: Non-Inverting Buffers and Drivers

Support

- KnowledgeBase
- Contact Technical Support
- TI Cross Reference
- Training
- Part Marking Lookup
- Part Number Nomenclature

Datasheet

2.5-V/3.3-V 16-Bit Buffers/Drivers With 3-State Outputs (Rev. G) (sn74alvth16244.pdf, 157 KB)
21 May 1999 Download

	SN74ALVTH16244
Voltage Nodes (V)	3.3, 2.5
Vcc range (V)	2.3 to 3.6
Input Level	TTL/CMOS
Output Level	LVTTL
Output Drive (mA)	-8/24
tpd max (ns)	3.5
Static Current	4.5
	Samples
	Inventory

Product Information

Features

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- Members of the Texas Instruments *Widebus*™ Family
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static-Power Dissipation
- 5-V I/O Compatible
- High Drive Capability (-32 mA/64 mA)
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.3 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Auto3-State Eliminates Bus Current Loading When Voltage at the Output Exceeds V_{CC}
- I_{off} and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV) Packages, and 380-mil Fine-Pitch Ceramic Flat (WD) Package

NOTE: For tape and reel order entry:
The DGGR package is abbreviated to GR, and
the DGVR package is abbreviated to VR.

Description

The 'ALVTH16244 devices are 16-bit buffers/line drivers designed for 2.5-V or 3.3-V V_{CC} operation, but with

the capability to provide a TTL interface to a 5-V system environment. These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.2 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.2 V, the output-enable (OE\) input should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

The SN54ALVTH16244 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ALVTH16244 is characterized for operation from -40°C to 85°C.

Pricing/Packaging/Samples

			Price	Packaging			Samples
Device	**Status**	**Temp (°C)**	**Budget Price ($US) | QTY**	**Package Type | Pins**	**Footprints**	**STD Pack QTY**	**Samples**
74ALVTH16244ZQLR	ACTIVE	-40 to 85	0.97 | 1KU	VFBGA (ZQL) | 56		1000	Not Available
SN74ALVTH16244DL	ACTIVE	-40 to 85	0.88 | 1KU	SSOP (DL) | 48		25	Contact TI Distributor or Sales Office
SN74ALVTH16244DLR	ACTIVE	-40 to 85	0.88 | 1KU	SSOP (DL) | 48		1000	Contact TI Distributor or Sales Office
SN74ALVTH16244GR	ACTIVE	-40 to 85	0.88 | 1KU	TSSOP (DGG) | 48		2000	Contact TI Distributor or Sales Office
SN74ALVTH16244KR	ACTIVE	-40 to 85	0.88 | 1KU	VFBGA (GQL) | 56		1000	Contact TI Distributor or Sales Office
SN74ALVTH16244VR	ACTIVE	-40 to 85	0.88 | 1KU	TVSOP (DGV) | 48		2000	Contact TI Distributor or Sales Office

Inventory

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	TI Inventory Status			Reported Distributor Inventory		
74ALVTH16244ZQLR	As of 10:41 AM GMT, 2 Jan 2005			As of 10:41 AM GMT, 2 Jan 2005		
	In Stock	**In Progress QTY | Date**	**Lead Time**	**In Stock**	**Distributor: Region | Company**	**Purchase**
	0*	>10k | 2 Feb	4 Weeks		None Reported View Distributors	
SN74ALVTH16244DL	As of 10:41 AM GMT, 2 Jan 2005			As of 10:41 AM GMT, 2 Jan 2005		
	In Stock	**In Progress QTY | Date**	**Lead Time**	**In Stock**	**Distributor: Region | Company**	**Purchase**
	1891*	1455 | 31 Jan	4 Weeks	>1k	Americas | DigiKey	Buy Now
		>10k | 7 Feb		238	Europe | Spoerle	Buy Now
				75	Americas | Memec Insight	Buy Now
SN74ALVTH16244DLR	As of 10:41 AM GMT, 2 Jan 2005			As of 10:41 AM GMT, 2 Jan 2005		
	In Stock	**In Progress QTY | Date**	**Lead Time**	**In Stock**	**Distributor: Region | Company**	**Purchase**
	0*	1493 | 24 Jan	4 Weeks	347	Americas | DigiKey	Buy Now
		>10k | 2 Feb				
SN74ALVTH16244GR	As of 10:41 AM GMT, 2 Jan 2005			As of 10:41 AM GMT, 2 Jan 2005		
	In Stock	**In Progress QTY | Date**	**Lead Time**	**In Stock**	**Distributor: Region | Company**	**Purchase**
	0*	500 | 17 Jan	4 Weeks	>1k	Americas | DigiKey	Buy Now
		1500 | 26 Jan		>1k	Americas | Newark Electronics	Buy Now
		>10k | 3 Feb				
SN74ALVTH16244KR	As of 10:41 AM GMT, 2 Jan 2005			As of 10:41 AM GMT, 2 Jan 2005		
	In Stock	**In Progress QTY | Date**	**Lead Time**	**In Stock**	**Distributor: Region | Company**	**Purchase**
	0*	>10k | 2 Feb	4 Weeks	348	Americas | DigiKey	Buy Now
SN74ALVTH16244VR	As of 10:41 AM GMT, 2 Jan 2005			As of 10:41 AM GMT, 2 Jan 2005		
	In Stock	**In Progress QTY | Date**	**Lead Time**	**In Stock**	**Distributor: Region | Company**	**Purchase**
	0*	5820 | 14 Feb	7 Weeks	>1k	Americas | DigiKey	Buy Now
		355 | 21 Feb				
		2000 | 24 Feb				
		>10k | 14 Mar				

* Our information is updated daily, so please check back with us soon if this does not meet your needs. You may also contact your TI Authorized Distributor, including those listed above, for real time stock information.

** Lead time information is not available at this time. However, our information is updated daily so please check back with us soon. Please contact your preferred TI Authorized Distributor for additional information.

Quality & Lead (Pb)-Free Data

	Product Content				MTBF/FIT Rate
Device	Eco Plan*	Lead/Ball Finish	MSL Rating/Peak Reflow	Details	Details
74ALVTH16244ZQLR	Pb-Free (RoHS)	SNAGCU	Level-1-260C-UNLIM	View	View
SN74ALVTH16244DL	None	CU NIPDAU	Level-1-235C-UNLIM	View	View
SN74ALVTH16244DLR	None	CU NIPDAU	Level-1-235C-UNLIM	View	View
SN74ALVTH16244GR	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM	View	View
SN74ALVTH16244KR	None	SNPB	Level-1-240C-UNLIM	View	View
SN74ALVTH16244VR	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM	View	View

* May not be currently available - please click on the Product Content Details "View" link in the table above for the latest availability information and additional product content details.

If the information you are requesting is not available online at this time, contact one of our Product Information Centers regarding the availability of this information.

* TI Recommends

Technical Documents

Datasheets

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2.5-V/3.3-V 16-Bit Buffers/Drivers With 3-State Outputs (Rev. G) (sn74alvth16244.pdf,157 KB)

21 May 1999 Download

Application Notes

Semiconductor Packing Material Electrostatic Discharge (ESD) Protection (szza047.htm,12 KB)

08 Jul 2004 Abstract

Shelf-Life Evaluation of Lead-Free Component Finishes (szza046.htm,12 KB)

24 May 2004 Abstract

Understanding and Interpreting Standard-Logic Data Sheets (Rev. B) (szza036b.htm,11 KB)

28 May 2003 Abstract

TI IBIS File Creation, Validation, and Distribution Processes (szza034.htm,12 KB)

29 Aug 2002 Abstract

16-Bit Widebus Logic Families in 56-Ball, 0.65-mm Pitch Very Thin Fine-Pitch BGA (Rev. B) (szza029b.htm,12 KB)

22 May 2002 Abstract

Power-Up 3-State (PU3S) Circuits in TI Standard Logic Devices (szza033.htm,12 KB)

10 May 2002 Abstract

Benefits & Issues of Migrating 5-V and 3.3-V Logic to Lower-Voltage Supplies (Rev. A) (sdaa011a.htm,12 KB)

08 Sep 1999 Abstract

Advanced Low-Voltage Technology (scea015.htm,11 KB)

27 Jul 1999 Abstract

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User Guides

LOGIC Pocket Data Book (scyd013.pdf,4835 KB)

05 Dec 2002 Download

Simulation Models

IBIS Model

IBIS Model of SN74ALVTH16244 (scem326.ibs,172 KB)

06 Feb 2003 ibis / zip

More Literature

Logic Selection Guide Second Half 2004 (Rev. V) (sdyu001v.pdf,5770 KB)

21 Sep 2004 Download

Logic Cross-Reference (Rev. A) (scyb017a.pdf,2938 KB)

07 Oct 2003 Download

Advanced Bus Interface Logic Selection Guide (scyt126.pdf,453 KB)

09 Jan 2001 Download

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