

P29FCT52A/B/C (P29PCT52A/B/C) P29FCT53A/B/C (P29PCT53A/B/C) OCTAL REGISTERED TRANSCEIVER

FEATURES

- Function, Pinout, and Drive Compatible with the FCT, F Logic, and Am2952/53
- FCT-C speed at 6.3ns max. (Com'I)
FCT-A speed at 7.5ns max. (Com'I)
- CMOS for Low Power Consumption
- Edge-rate Control Circuitry for Significantly Improved Noise Characteristics
- ESD protection exceeds 2000V
- Inputs and Outputs Interface Directly with TTL, NMOS, and CMOS Devices
- Outputs Meet Levels Required for CMOS Static RAM Low Power Standby Mode
- 64 mA Sink Current (Com'I), 48 mA (MII)
24 mA Source Current (Com'I), 15 mA (MII)
- Manufactured in 0.8 micron PACE Technology™

DESCRIPTION

The '29FCT52 AND '29FCT53 have two 8-bit back-to-back registers that store data flowing in both directions between two bidirectional buses. Separate clock, clock enable and 3-state output enable signals are provided for each register. Both A outputs and B outputs are guaranteed to sink 64mA.

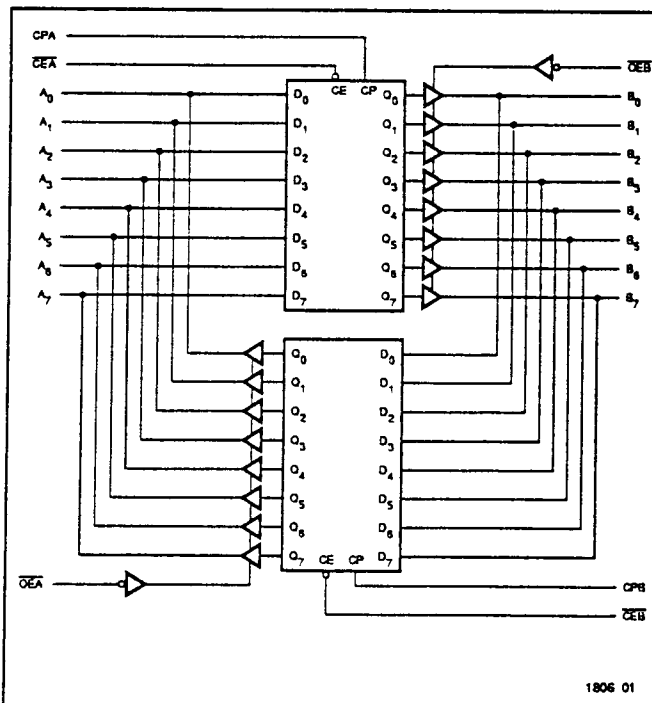
The '29FCT52 is an inverting option of the '29FCT53.

The '29FCT52 and '29FCT53 are manufactured using PACE Technology™ which is Performance Advanced

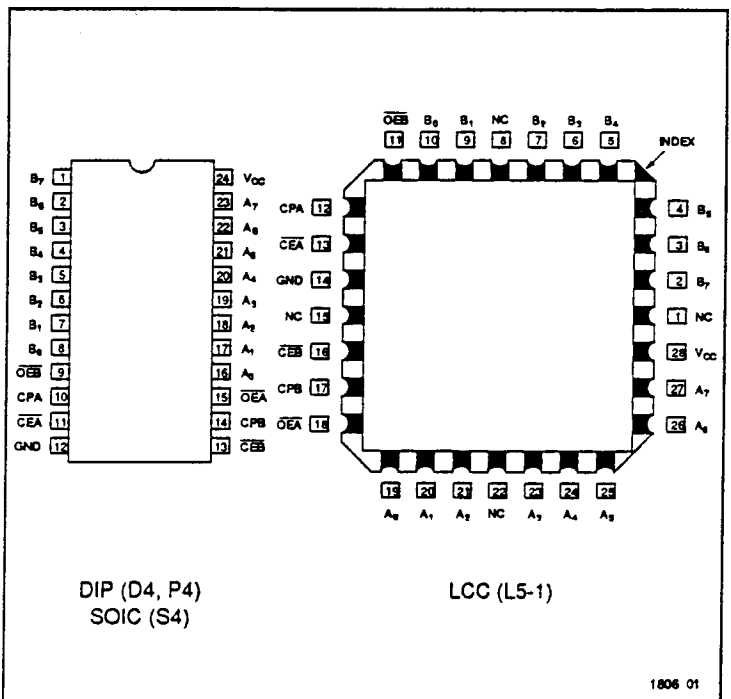
CMOS Engineered to use 0.8 micron effective channel lengths resulting in 500 picoseconds loaded* internal gate delays. PACE Technology includes two-level metal and epitaxial substrates. In addition to very high performance and very high density, the technology features latch-up protection and single event upset protection, and is supported by a Class 1 environment volume production facility.

* For a fan-in/fan-out of 4 at 85°C junction temperature and 5.0 V supply. For a fan-in/fan-out of 1, the internal gate delay is 200 picosecond at room temperature.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



REGISTERED FUNCTION TABLE

Inputs			Internal Q	Function
D	CP	\overline{CE}		
X	X	H	NC	Hold Data
L	\downarrow	L	L	Load Data
H	\uparrow	L	H	

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OUTPUT CONTROL

\overline{OE}	Internal Q	Y-Outputs		Function
		'29FCT52	'29FCT53	
H	X	Z	Z	Disable Outputs
L	L	L	H	Enable Outputs
L	H	H	L	

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PIN DESCRIPTION

Name	I/O	Description
A ₀₋₇	I/O	Eight bidirectional lines carrying the A Register inputs or B Register outputs.
B ₀₋₇	I/O	Eight bidirectional lines carrying the B Register inputs or A Register outputs.
CPA	I	Clock for the A Register. When \overline{CEA} is LOW, data is entered into the A Register on the LOW-to-HIGH transition of the CPA signal.
\overline{CEA}	I	Clock Enable for the A Register. When \overline{CEA} is LOW, data is entered into the A Register on the LOW-to-HIGH transition of the CPA signal. When \overline{CEA} is HIGH, the A Register holds its contents regardless of CPA signal transitions.
\overline{OEB}	I	Output Enable for the A Register. When \overline{OEB} is LOW, the A Register outputs are enabled onto the B ₀₋₇ lines. When \overline{OEB} is HIGH, the B ₀₋₇ outputs are in the high impedance state.
CPB	I	Clock for the B Register. When \overline{CEB} is LOW, data is entered into the B Register on the LOW-to-HIGH transition of the CPB signal.
\overline{CEB}	I	Clock Enable for the B Register. When \overline{CEB} is LOW, data is entered into the B Register on the LOW-to-HIGH transition of the CPB signal. When \overline{CEB} is HIGH, the B Register holds its contents regardless of CPB signal transitions.
\overline{OEA}	I	Output Enable for the B Register. When \overline{OEA} is LOW, the B Register outputs are enabled onto the A ₀₋₇ lines. When \overline{OEA} is HIGH, the A ₀₋₇ outputs are in the high impedance state.

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ABSOLUTE MAXIMUM RATINGS^{1,2}

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	-65 to +150	°C
T_A	Ambient Temperature Under Bias	-65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	-0.5 to +7.0	V
I_{IN}	Input Current	-30 to +5.0	mA

Notes:

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1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	-55°C	+125°C
Commercial	0°C	+70°C

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Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	-0.5 to $V_{CC} + 0.5$	V
V_{OUT}	Voltage Applied to Output	-0.5 to $V_{CC} + 0.5$	V

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2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

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DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter	Min	Typ ¹	Max	Units	V_{CC}	Conditions	
V_{IH}	Input HIGH Voltage	2.0			V			
V_{IL}	Input LOW Voltage			0.8	V			
V_H	Hysteresis		0.35		V		All inputs	
V_{CD}	Input Clamp Diode Voltage		-0.7	-1.2	V	MIN	$I_{IN} = -18\text{mA}$	
V_{OH}	Output HIGH Voltage	$V_{CC} = 3\text{V}, V_{IN} = 0.2\text{V}, \text{ or } V_{CC} - 0.2\text{V}$	$V_{CC} - 0.2$	V_{CC}	V		$I_{OH} = -32\mu\text{A}$	
		Military/Commercial (CMOS)	$V_{CC} - 0.2$	V_{CC}	V	MIN	$I_{OH} = -300\mu\text{A}$	
		Military (TTL)	2.4	4.3	V	MIN	$I_{OH} = -15\text{mA}$	
		Commercial (TTL)	2.7	4.3	V	MIN	$I_{OH} = -24\text{mA}$	
V_{OL}	Output LOW Voltage	$V_{CC} = 3\text{V}, V_{IN} = 0.2\text{V}, \text{ or } V_{CC} - 0.2\text{V}$		0.2	V		$I_{OL} = 300\mu\text{A}$	
		Military/Commercial (CMOS)		GND	V	MIN	$I_{OL} = 300\mu\text{A}$	
		Military (TTL)		0.3	0.55	V	MIN	$I_{OL} = 48\text{mA}$
		Commercial (TTL)		0.3	0.55	V	MIN	$I_{OL} = 64\text{mA}$
I_{IH}	Input HIGH Current (Except I/O Pins)			5	μA	MAX	$V_{IN} = V_{CC}$	
I_{IL}	Input LOW Current (Except I/O Pins)			-5	μA	MAX	$V_{IN} = \text{GND}$	
I_{IH}	Input HIGH Current ³ (Except I/O Pins)			5	μA	MAX	$V_{IN} = 2.7\text{V}$	
I_{IL}	Input LOW Current ³ (Except I/O Pins)			-5	μA	MAX	$V_{IN} = 0.5\text{V}$	
I_{IH}	Input HIGH Current (I/O Pins only)			15	μA	MAX	$V_{IN} = V_{CC}$	
I_{IL}	Input LOW Current (I/O Pins only)			-15	μA	MAX	$V_{IN} = \text{GND}$	
I_{IH}	Input HIGH Current ³ (I/O Pins only)			15	μA	MAX	$V_{IN} = 2.7\text{V}$	
I_{IL}	Input LOW Current ³ (I/O Pins only)			-15	μA	MAX	$V_{IN} = 0.5\text{V}$	
I_{OS}	Output Short Circuit Current ²	-60			mA	MAX	$V_{OUT} = 0.0\text{V}$	
C_{IN}	Input Capacitance ³		5	10	pF		All inputs	
C_{OUT}	Output Capacitance ³		9	12	pF		All outputs	

Notes:

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1. Typical limits are at $V_{CC} = 5.0\text{V}$, $T_A = +25^\circ\text{C}$ ambient.

2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect

operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

3. This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ ¹	Max	Units	Conditions
I_{CC}	Quiescent Power Supply Current (CMOS inputs)	0.5	1.5	mA	$V_{CC} = \text{MAX}$, $f_1 = 0$, Outputs Open, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	0.5	2.0	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 3.4V^2$, $f_1 = 0$, Outputs Open
I_{CCD}	Dynamic Power Supply Current ³	0.15	0.25	mA/ mHz	$V_{CC} = \text{MAX}$, One Input Toggling, 50% Duty Cycle, OEA or OEB = GND Outputs Open, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
I_C	Total Power Supply Current ⁵	2.0	4.0	mA	$V_{CC} = \text{MAX}$, $f_0 = 10 \text{ MHz}$, 50% Duty Cycle, Outputs Open, One Bit Toggling at $f_1 = 5 \text{ MHz}$, OEA or OEB = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		2.5	6.0	mA	$V_{CC} = \text{MAX}$, $f_0 = 10 \text{ MHz}$, 50% Duty Cycle, Outputs Open, One Bit Toggling at $f_1 = 5 \text{ MHz}$, OEA or OEB = GND, $V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$
		4.3	7.8 ⁴	mA	$V_{CC} = \text{MAX}$, $f_0 = 10 \text{ MHz}$, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at $f_1 = 2.5 \text{ MHz}$, OEA or OEB = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		6.5	16.8 ⁴	mA	$V_{CC} = \text{MAX}$, $f_0 = 10 \text{ MHz}$, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at $f_1 = 2.5 \text{ MHz}$, OEA or OEB = GND, $V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$

Notes:

- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient and maximum loading.
- Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $$I_{CC} = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$$

$$I_{CC} = I_{\text{CCOC}} + I_{\text{CCOT}} D_H N_T + I_{\text{CCD}} (f_0/2 + f_1 N_1)$$

$$I_{\text{CCOC}} = \text{Quiescent Current with CMOS input levels}$$

- I_{CCOT} = Power Supply Current for a TTL High Input ($V_{IN} = 3.4V$)
 - D_H = Duty Cycle for TTL Inputs High
 - N_T = Number of TTL Inputs at D_H
 - I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 - f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 - f_1 = Input Frequency
 - N_1 = Number of Inputs at f_1
- All currents are in milliamps and all frequencies are in megahertz.

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AC CHARACTERISTICS

Symbol	Parameter	P29FCT52A/53A				P29FCT52B/53B				P29FCT52C/53C				Units	Fig. No.
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min. ¹	Max.	Min. ¹	Max.	Min. ¹	Max.	Min. ¹	Max.	Min. ¹	Max.	Min. ¹	Max.		
t_{PLH} t_{PHL}	Propagation Delay CPA, CPB to B_n, A_n	2.0	11.0	2.0	10.0	2.0	8.0	2.0	7.5	2.0	7.3	2.0	6.3	ns	1,5
t_{PZH} t_{PZL}	Output Enable Time \overline{OEA} or \overline{OEB} to A_n or B_n	1.5	13.0	1.5	10.5	1.5	8.5	1.5	8.0	1.5	8.0	1.5	7.0	ns	1,7,8
t_{PHZ} t_{PLZ}	Output Enable Time \overline{OEA} or \overline{OEB} to A_n or B_n	1.5	10.0	1.5	10.0	1.5	8.0	1.5	7.5	1.5	7.5	1.5	6.5	ns	1,7,8

Notes:

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1. Minimum limits are guaranteed but not tested on Propagation Delays.
2. AC Characteristics guaranteed with $C_L = 50pF$ as shown in Figure 1.

AC OPERATING REQUIREMENTS

Symbol	Parameter	P29FCT52A/53A				P29FCT52B/53B				P29FCT52C/53C				Units	Fig. No.
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW, A_n, B_n to CPA, CPB	2.5	—	2.5	—	2.5	—	2.5	—	2.5	—	2.5	—	ns	4
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW, A_n, B_n to CPA, CPB	2.0	—	2.0	—	1.5	—	1.5	—	1.5	—	1.5	—	ns	4
$t_s(H)$ $t_s(L)$	Set-up Time, HIGH or LOW, $\overline{CEA}, \overline{CEB}$ to CPA, CPB	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns	4
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW, $\overline{CEA}, \overline{CEB}$ to CPA, CPB	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns	4
$t_w(H)$ $t_w(L)$	Pulse Width, HIGH or LOW, CPA or CPB	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns	5

Note:

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1. Minimum limits are guaranteed but not tested on Propagation Delays.

ORDERING INFORMATION

$\frac{P29FCTxxx}{\text{Device}}$ $\frac{xx}{\text{Package}}$ $\frac{x}{\text{Processing}}$

